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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	61
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc4010l-5pc84c

XC4000E and XC4000EX Families Compared to the XC4000

For readers already familiar with the XC4000 family of Xilinx Field Programmable Gate Arrays, the major new features in the XC4000-Series devices are listed in this section. The biggest advantages of XC4000E and XC4000EX devices are significantly increased system speed, greater capacity, and new architectural features, particularly Select-RAM memory. The XC4000EX devices also offer many new routing features, including special high-speed clock buffers that can be used to capture input data with minimal delay.

Any XC4000E device is pinout- and bitstream-compatible with the corresponding XC4000 device. An existing XC4000 bitstream can be used to program an XC4000E device. However, since the XC4000E includes many new features, an XC4000E bitstream cannot be loaded into an XC4000 device.

Most XC4000EX devices have no corresponding XC4000 devices, because of the larger CLB arrays. The XC4028EX has the same array size as the XC4025 and XC4025E, but is not bitstream-compatible. However, the XC4025, XC4025E, and XC4028EX are all pinout-compatible.

Improvements in XC4000E and XC4000EX

Increased System Speed

Delays in FPGA-based designs are layout dependent. There is a rule of thumb designers can consider—the system clock rate should not exceed one third to one half of the specified toggle rate. Critical portions of a design, such as shift registers and simple counters, can run faster—approximately two thirds of the specified toggle rate.

XC4000E and XC4000EX devices can run at synchronous system clock rates of up to 66 MHz, and internal performance can exceed 150 MHz. This increase in performance over the previous families stems from improvements in both device processing and system architecture. XC4000-Series devices use a sub-micron triple-layer metal process. In addition, many architectural improvements have been made, as described below.

PCI Compliance

XC4000-Series -3 and faster speed grades are fully PCI compliant. XC4000E and XC4000EX devices can be used to implement a one-chip PCI solution.

Carry Logic

The speed of the carry logic chain has increased dramatically. Some parameters, such as the delay on the carry chain through a single CLB (T_{BYP}), have improved by as much as 50% from XC4000 values. See "Fast Carry Logic" on page 21 for more information.

Select-RAM Memory: Edge-Triggered, Synchronous RAM Modes

The RAM in any CLB can be configured for synchronous, edge-triggered, write operation. The read operation is not affected by this change to an edge-triggered write.

Dual-Port RAM

A separate option converts the 16x2 RAM in any CLB into a 16x1 dual-port RAM with simultaneous Read/Write.

The function generators in each CLB can be configured as either level-sensitive (asynchronous) single-port RAM, edge-triggered (synchronous) single-port RAM, edge-triggered (synchronous) dual-port RAM, or as combinatorial logic.

Configurable RAM Content

The RAM content can now be loaded at configuration time, so that the RAM starts up with user-defined data.

H Function Generator

In XC4000-Series devices, the H function generator is more versatile than in the XC4000. Its inputs can come not only from the F and G function generators but also from up to three of the four control input lines. The H function generator can thus be totally or partially independent of the other two function generators, increasing the maximum capacity of the device.

IOB Clock Enable

The two flip-flops in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000 CLB. This new feature makes the IOBs more versatile, and avoids the need for clock gating.

Output Drivers

The output pull-up structure defaults to a TTL-like totem-pole. This driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc, just like the XC4000 outputs. Alternatively, XC4000-Series devices can be globally configured with CMOS outputs, with p-channel pull-up transistors pulling to Vcc. Also, the configurable pull-up resistor in the XC4000 Series is a p-channel transistor that pulls to Vcc, whereas in the XC4000 it is an n-channel transistor that pulls to a voltage one transistor threshold below Vcc.

Input Thresholds

The input thresholds can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other.

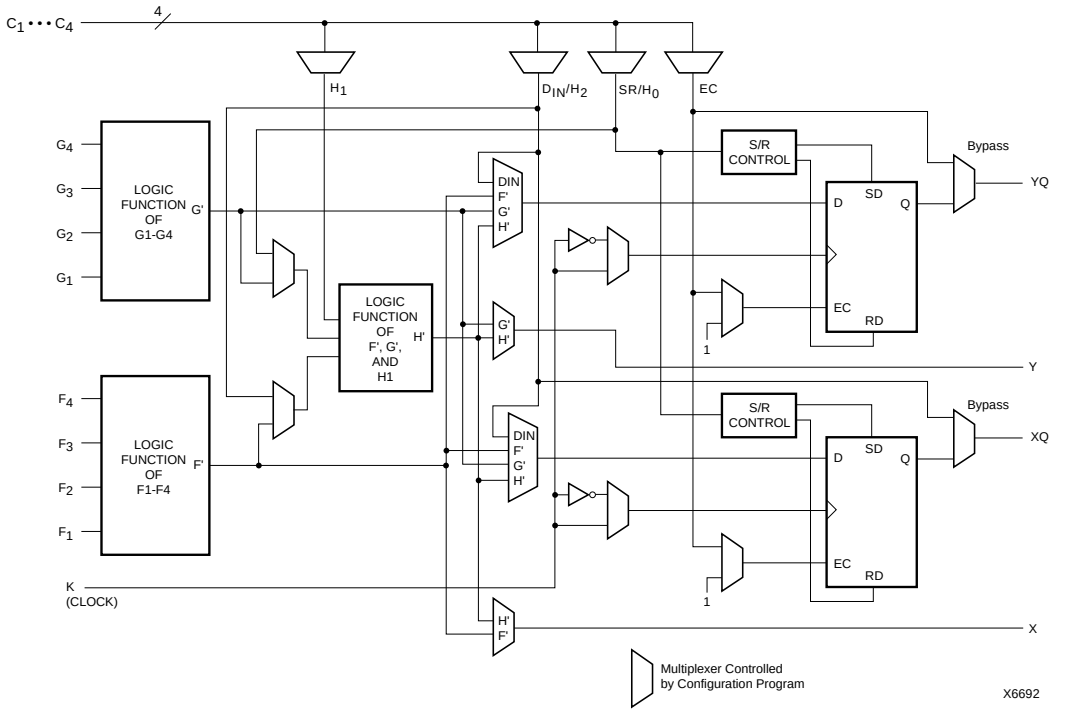


Figure 1: Simplified Block Diagram of XC4000-Series CLB (RAM and Carry Logic functions not shown)

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in Table 4.

Latches (XC4000EX only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in Table 4.

Table 4: CLB Storage Element Functionality (active rising edge is shown)

Mode	K	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop	X	X	1	X	SR
	⎍/‾	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
⎍/‾	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

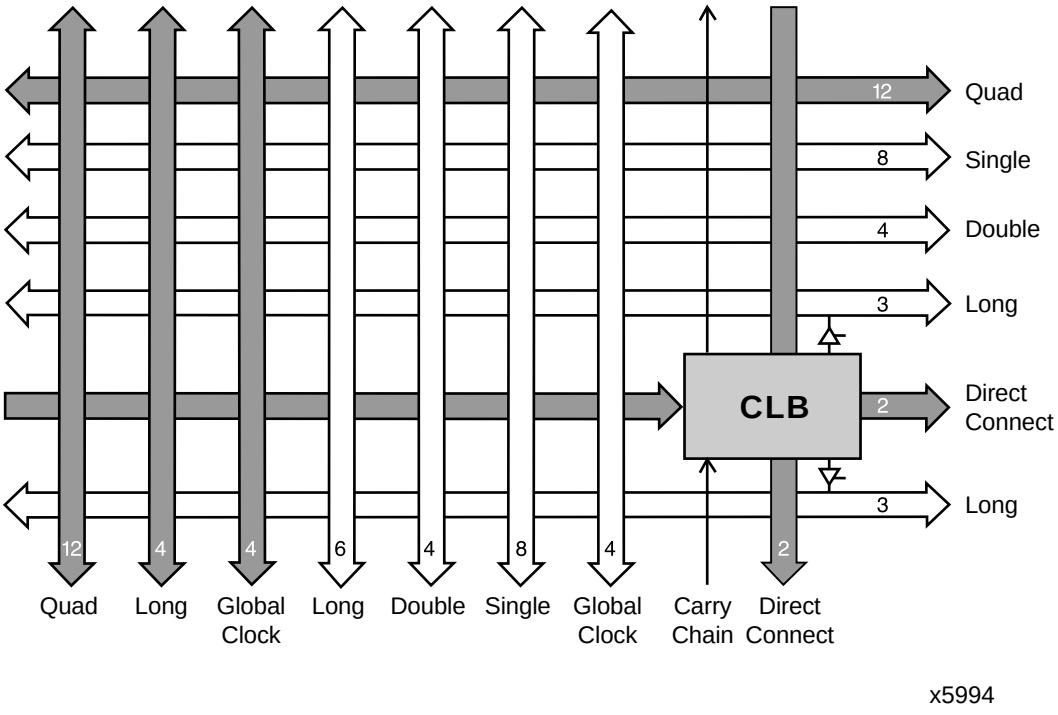


Figure 26: High-Level Routing Diagram of XC4000-Series CLB (shaded arrows indicate XC4000EX only)

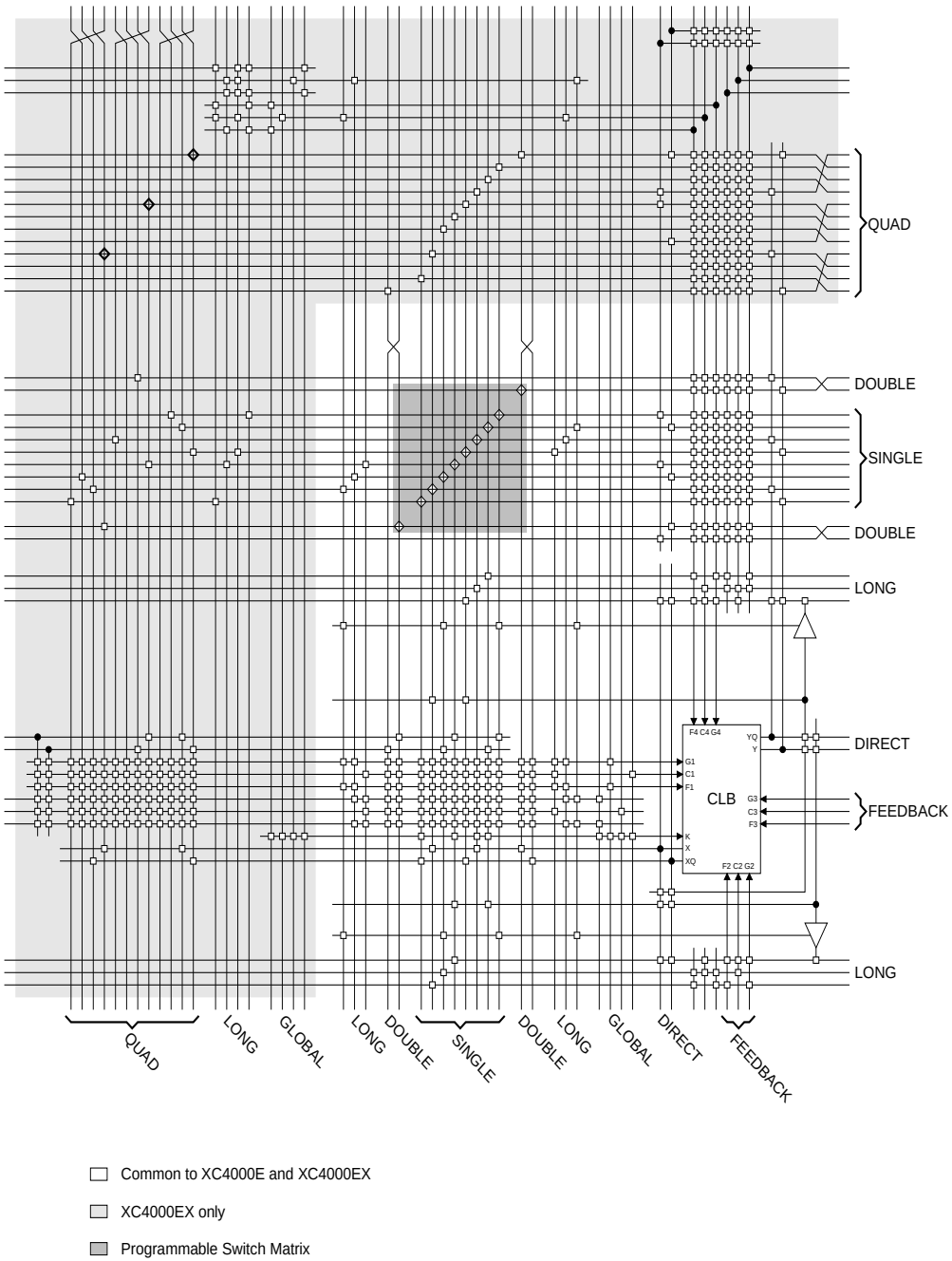


Figure 27: Detail of Programmable Interconnect Associated with XC4000-Series CLB

Configuration Through the Boundary Scan Pins

XC4000-Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 Devices*." This application note also applies to XC4000E and XC4000EX devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000-Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

Readback of Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

XC4000-Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 51.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

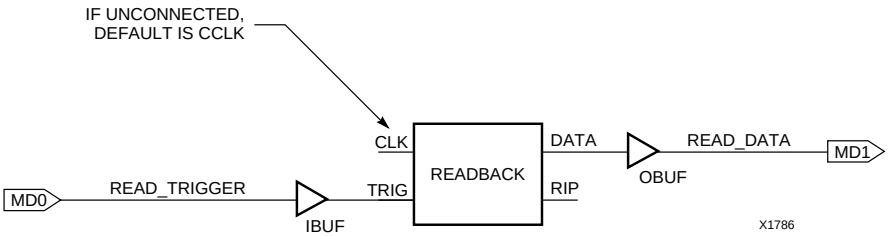
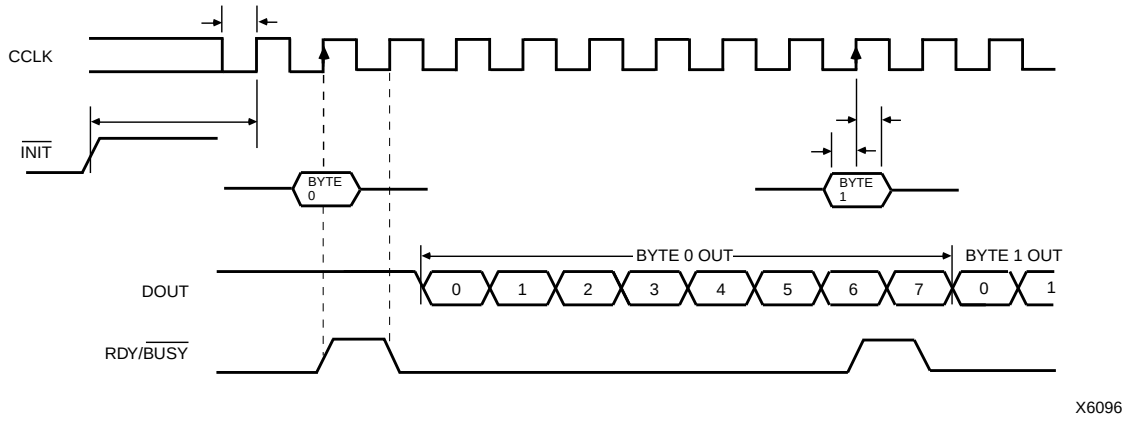


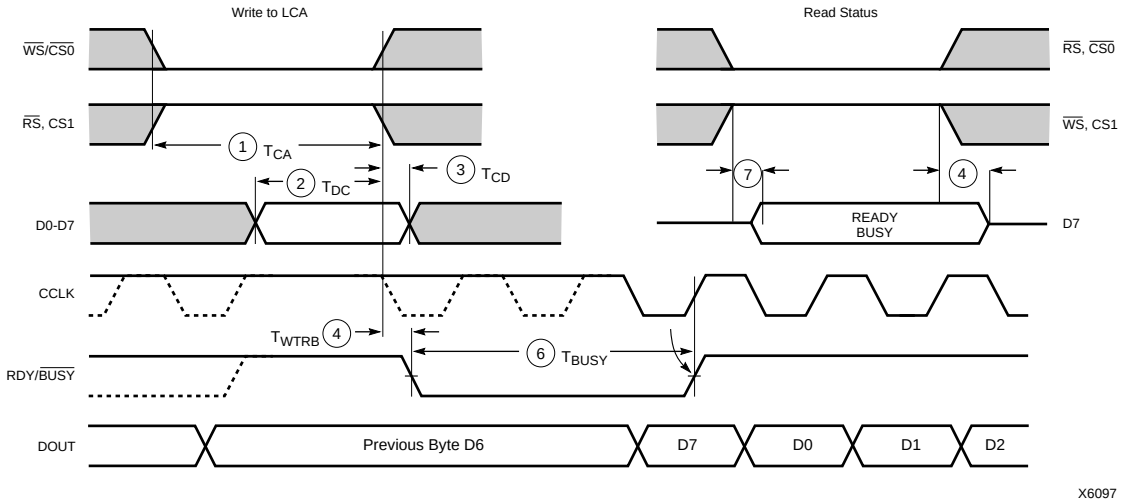
Figure 51: Readback Schematic Example



	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	60		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	50		ns
	CCLK Low time	T_{CCL}	60		ns
	CCLK Frequency	F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after $\overline{INIT}$ goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/$\overline{BUSY}$ line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/$\overline{BUSY}$ is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 60: Synchronous Peripheral Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
Write	Effective Write time ($\overline{CS0}$, $\overline{WS}$=Low; $\overline{RS}$, CS1=High)	1	T_{CA}	100		ns
	DIN setup time	2	T_{DC}	60		ns
	DIN hold time	3	T_{CD}	0		ns
RDY	RDY/$\overline{BUSY}$ delay after end of Write or Read	4	T_{WTRB}		60	ns
	RDY/$\overline{BUSY}$ active after beginning of Read	7			60	ns
	RDY/$\overline{BUSY}$ Low output (Note 4)	6	T_{BUSY}	2	9	CCLK periods

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.
2. The time from the end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of $\overline{WS}$. RDY/$\overline{BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. A new write may be asserted immediately after RDY/$\overline{BUSY}$ goes Low, but write may not be terminated until RDY/$\overline{BUSY}$ has been High for one CCLK period.

Figure 62: Asynchronous Peripheral Mode Programming Switching Characteristics

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4		ns
		XC4005E	5.0	5.0	4.0		ns
		XC4006E	6.0	5.9	4.7		ns
		XC4008E	7.0	6.3	5.0		ns
		XC4010E	8.0	6.4	5.1		ns
		XC4013E	9.0	7.2	5.7		ns
		XC4020E	10.0	8.2	7.3		ns
		XC4025E	11.0	9.1	7.3		ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6		ns
		XC4005E	6.0	5.3	4.5		ns
		XC4006E	7.8	6.4	5.4		ns
		XC4008E	8.1	6.8	5.8		ns
		XC4010E	10.5	6.9	5.9		ns
		XC4013E	11.0	7.7	6.5		ns
		XC4020E	12.0	8.7	8.7		ns
		XC4025E	12.0	9.6	9.6		ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9		ns
		XC4005E	7.0	6.0	5.7		ns
		XC4006E	7.5	6.7	5.7		ns
		XC4008E	8.0	7.1	6.0		ns
		XC4010E	8.5	7.3	6.2		ns
		XC4013E	8.7	7.5	7.0		ns
		XC4020E	11.0	8.4	7.1		ns
		XC4025E	11.0	8.4	7.1		ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3		ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T_{PUS}	XC4003E	20.0	14.0	14.0		ns
		XC4005E	23.0	16.0	16.0		ns
		XC4006E	25.0	18.0	18.0		ns
		XC4008E	27.0	20.0	20.0		ns
		XC4010E	29.0	22.0	22.0		ns
		XC4013E	32.0	26.0	26.0		ns
		XC4020E	35.0	32.5	32.5		ns
		XC4025E	42.0	39.1	39.1		ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0		ns
		XC4005E	10.0	8.0	6.8		ns
		XC4006E	11.5	9.0	7.7		ns
		XC4008E	12.5	10.0	8.5		ns
		XC4010E	13.5	11.0	9.4		ns
		XC4013E	15.0	13.0	11.7		ns
		XC4020E	16.0	14.8	14.8		ns
		XC4025E	18.0	16.5	16.5		ns
					Preliminary		

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

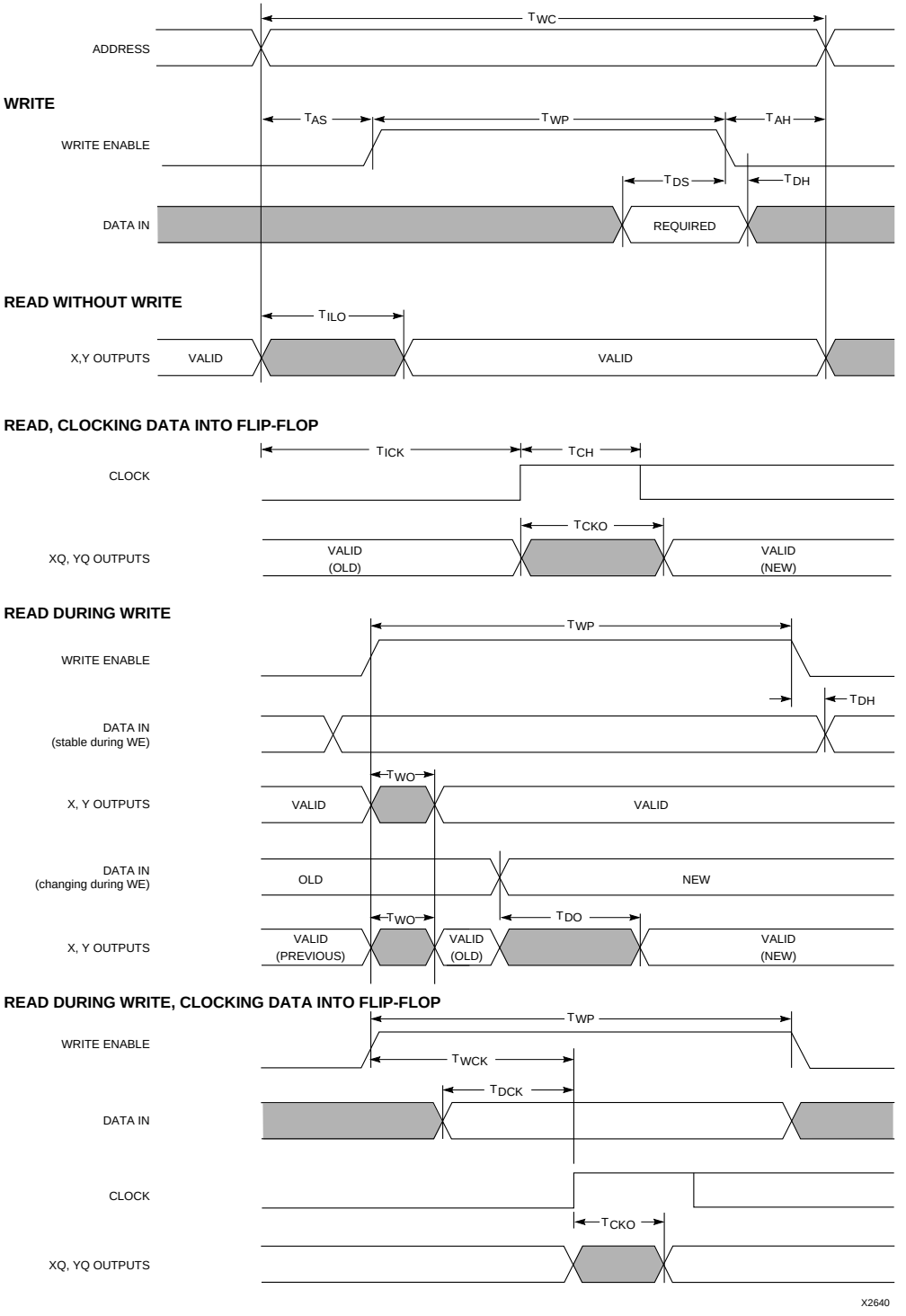
XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Combinatorial Delays									
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		
F/G inputs via H' to X/Y outputs	T_{IHO}		4.7		4.3		2.7		
C inputs via SR through H' to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		
C inputs via H' to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		
C inputs via DIN through H' to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		
CLB Fast Carry Logic									
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		
Sequential Delays									
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		
Setup Time before Clock K									
F/G inputs	T_{ICK}	4.0		3.0		2.4			
F/G inputs via H'	T_{IHCK}	6.1		4.6		3.9			
C inputs via H0 through H'	T_{HH0CK}	4.5		3.6		3.5			
C inputs via H1 through H'	T_{HH1CK}	5.0		4.1		3.3			
C inputs via H2 through H'	T_{HH2CK}	4.8		3.8		3.7			
C inputs via DIN	T_{DICK}	3.0		2.4		2.0			
C inputs via EC	T_{ECCK}	4.0		3.0		2.6			
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0			
C_{IN} input via F'/G'	T_{CCK}								
C_{IN} input via F'/G' and H'	T_{CHCK}								
						Preliminary			

XC4000E CLB Level-Sensitive RAM Timing Characteristics



XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
GND	P52	P71	P14	P79	P101	-
DONE	P53	P72	R15	P80	P103	-
VCC	P54	P73	P13	P81	P106	-
$\overline{\text{PROGRAM}}$	P55	P74	R14	P82	P108	-
I/O (D7)	P56	P75	T16	P83	P109	295
I/O, PGCK3	P57	P76	T15	P84	P110	298
I/O	-	P77	R13	P85	P111	301
I/O	-	P78	P12	P86	P112	304
I/O (D6)	P58	P79	T14	P87	P113	307
I/O	-	P80	T13	P88	P114	310
I/O	-	-	R12	P89	P115	313
I/O	-	-	T12	P90	P116	316
GND	-	P81	P11	P91	P119	-
I/O	-	P82	R11	P92	P120	319
I/O	-	P83	T11	P93	P121	322
I/O (D5)	P59	P84	T10	P94	P122	325
I/O ($\overline{\text{CS0}}$)	P60	P85	P10	P95	P123	328
I/O	-	P86	R10	P96	P126	331
I/O	-	P87	T9	P97	P127	334
I/O (D4)	P61	P88	R9	P98	P128	337
I/O	P62	P89	P9	P99	P129	340
VCC	P63	P90	R8	P100	P130	-
GND	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P92	T8	P102	P132	343
I/O ($\overline{\text{RS}}$)	P66	P93	T7	P103	P133	346
I/O	-	P94	T6	P104	P134	349
I/O	-	P95	R7	P105	P135	352
I/O (D2)	P67	P96	P7	P106	P138	355
I/O	P68	P97	T5	P107	P139	358
I/O	-	P98	R6	P108	P140	361
I/O	-	P99	T4	P109	P141	364
GND	-	P100	P6	P110	P142	-
I/O	-	-	R5	P111	P145	367
I/O	-	-	-	P112	P146	370
I/O (D1)	P69	P101	T3	P113	P147	373
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P102	P5	P114	P148	376
I/O	-	P103	R4	P115	P149	379
I/O	-	P104	R3	P116	P150	382
I/O (D0, DIN)	P71	P105	P4	P117	P151	385
I/O, SGCK4 (DOUT)	P72	P106	T2	P118	P152	388
CCLK	P73	P107	R2	P119	P153	-
VCC	P74	P108	P3	P120	P154	-
O, TDO	P75	P109	T1	P121	P159	0
GND	P76	P110	N3	P122	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P112	P2	P124	P162	5
I/O	-	P113	N2	P125	P163	8
I/O	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P115	P1	P127	P165	14
I/O (A3)	P80	P116	N1	P128	P166	17
I/O	-	P117	M2	P129	P167	20
I/O	-	-	M1	P130	P168	23
GND	-	P118	L3	P131	P171	-
I/O	-	P119	L2	P132	P172	26
I/O	-	P120	L1	P133	P173	29
I/O (A4)	P81	P121	K3	P134	P174	32
I/O (A5)	P82	P122	K2	P135	P175	35
I/O	-	P123	K1	P137	P178	38
I/O	-	P124	J1	P138	P179	41
I/O (A6)	P83	P125	J2	P139	P180	44
I/O (A7)	P84	P126	J3	P140	P181	47
GND	P1	P127	H2	P141	P182	-

4/2/96

Additional No Connect (N.C.) Connections on PQ160 & PQ208 Packages

PQ160	PQ208
P136	P1
	P3
	P12-P13
	P19-20
	P31-P32
	P38-P39
	P51-P54
	P65-P66
	P72-P73
	P84-P85
	P91-P92
	P102
	P104-P105
	P107
	P117-P118
	P124-P125
	P136-P137
	P143-P144
	P155-P158
	P169-P170
	P176-P177
	P188-P189
	P195-P196
	P206-P208

2/28/96

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
GND	-	P70	M16	P90	-
I/O	-	P71	T18	P93	307
I/O	-	P72	P17	P94	310
I/O	P48	P73	N16	P95	313
I/O	P49	P74	T17	P96	316
I/O	-	P75	R17	P97	319
I/O	-	P76	P16	P98	322
I/O	P50	P77	U18	P99	325
I/O, SGCK3	P51	P78	T16	P100	328
GND	P52	P79	R16	P101	-
DONE	P53	P80	U17	P103	-
VCC	P54	P81	R15	P106	-
$\overline{\text{PROGRAM}}$	P55	P82	V18	P108	-
I/O (D7)	P56	P83	T15	P109	331
I/O, PGCK3	P57	P84	U16	P110	334
I/O	-	P85	T14	P111	337
I/O	-	P86	U15	P112	340
I/O (D6)	P58	P87	V17	P113	343
I/O	-	P88	V16	P114	346
I/O	-	P89	T13	P115	349
I/O	-	P90	U14	P116	352
GND	-	P91	T12	P119	-
I/O	-	P92	U13	P120	355
I/O	-	P93	V13	P121	358
I/O (D5)	P59	P94	U12	P122	361
I/O ($\overline{\text{CS0}}$)	P60	P95	V12	P123	364
I/O	-	-	T11	P124	367
I/O	-	-	U11	P125	370
I/O	-	P96	V11	P126	373
I/O	-	P97	V10	P127	376
I/O (D4)	P61	P98	U10	P128	379
I/O	P62	P99	T10	P129	382
VCC	P63	P100	R10	P130	-
GND	P64	P101	R9	P131	-
I/O (D3)	P65	P102	T9	P132	385
I/O ($\overline{\text{RS}}$)	P66	P103	U9	P133	388
I/O	-	P104	V9	P134	391
I/O	-	P105	V8	P135	394
I/O	-	-	U8	P136	397
I/O	-	-	T8	P137	400
I/O (D2)	P67	P106	V7	P138	403
I/O	P68	P107	U7	P139	406
I/O	-	P108	V6	P140	409
I/O	-	P109	U6	P141	412
GND	-	P110	T7	P142	-
I/O	-	P111	U5	P145	415
I/O	-	P112	T6	P146	418
I/O (D1)	P69	P113	V3	P147	421
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P114	V2	P148	424
I/O	-	P115	U4	P149	427
I/O	-	P116	T5	P150	430
I/O (D0, DIN)	P71	P117	U3	P151	433
I/O, SGCK4 (DOUT)	P72	P118	T4	P152	436
CCLK	P73	P119	V1	P153	-
VCC	P74	P120	R4	P154	-
O, TDO	P75	P121	U2	P159	0
GND	P76	P122	R3	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P123	T3	P161	2
I/O, PGCK4 (A1)	P78	P124	U1	P162	5
I/O	-	P125	P3	P163	8
I/O	-	P126	R2	P164	11
I/O (CS1, A2)	P79	P127	T2	P165	14
I/O (A3)	P80	P128	N3	P166	17
I/O	-	P129	P2	P167	20
I/O	-	P130	T1	P168	23
GND	-	P131	M3	P171	-
I/O	-	P132	P1	P172	26
I/O	-	P133	N1	P173	29
I/O (A4)	P81	P134	M2	P174	32
I/O (A5)	P82	P135	M1	P175	35
I/O	-	-	L3	P176	38
I/O	-	P136	L2	P177	41
I/O	-	P137	L1	P178	44
I/O	-	P138	K1	P179	47
I/O (A6)	P83	P139	K2	P180	50
I/O (A7)	P84	P140	K3	P181	53
GND	P1	P141	K4	P182	-

4/2/96

Additional No Connect (N.C.) Connections on PG191 & PQ208 Packages

PG191	PQ208	PQ208
A14	P1	P107
B5	P3	P117
B6	P12	P118
B13	P13	P143
D1	P38	P144
D18	P39	P155
F2	P51	P156
F17	P52	P157
N2	P53	P158
N17	P54	P169
R1	P65	P170
R18	P66	P195
V4	P91	P196
V5	P92	P206
V14	P102	P207
V15	P104	P208
	P105	

2/28/96

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	P136	U8	P156	607
I/O	P137	T8	P157	610
I/O	-	-	-	613
I/O	-	-	-	616
I/O (D2)	P138	V7	P159	619
I/O	P139	U7	P160	622
VCC	-	-	P161	-
I/O	P140	V6	P162	625
I/O	P141	U6	P163	628
I/O	-	R8	P164	631
I/O	-	R7	P165	634
GND	P142	T7	P166	-
I/O	-	R6	P167	637
I/O	-	R5	P168	640
I/O	P143	V5	P169	643
I/O	P144	V4	P170	646
I/O	P145	U5	P171	649
I/O	P146	T6	P172	652
I/O (D1)	P147	V3	P173	655
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P148	V2	P174	658
I/O	-	-	-	661
I/O	-	-	-	664
I/O	P149	U4	P175	667
I/O	P150	T5	P176	670
I/O (D0, DIN)	P151	U3	P177	673
I/O, SGCK4 (DOUT)	P152	T4	P178	676
CCLK	P153	V1	P179	-
VCC	P154	R4	P180	-
O, TDO	P159	U2	P181	0
GND	P160	R3	P182	-
I/O (A0, $\overline{WS}$)	P161	T3	P183	2
I/O, PGCK4 (A1)	P162	U1	P184	5
I/O	P163	P3	P185	8
I/O	P164	R2	P186	11
I/O (CS1, A2)	P165	T2	P187	14
I/O (A3)	P166	N3	P188	17
I/O	-	-	-	20
I/O	-	-	-	23
I/O	-	P4	P189	26
I/O	-	N4	P190	29
I/O	P167	P2	P191	32
I/O	P168	T1	P192	35
I/O	P169	R1	P193	38
I/O	P170	N2	P194	41
GND	P171	M3	P196	-
I/O	P172	P1	P197	44
I/O	P173	N1	P198	47
I/O	-	M4	P199	50
I/O	-	L4	P200	53
VCC	-	-	P201	-
I/O	-	-	-	56
I/O	-	-	-	59
I/O (A4)	P174	M2	P202	62
I/O (A5)	P175	M1	P203	65
I/O	P176	L3	P205	68
I/O	P177	L2	P206	71
I/O	P178	L1	P207	74
I/O	P179	K1	P208	77
I/O (A6)	P180	K2	P209	80
I/O (A7)	P181	K3	P210	83
GND	P182	K4	P211	-

4/2/96

Additional No Connect (N.C.) Connections on HQ208 & HQ240 Packages

HQ208	HQ240
P1	P22 ‡
P3	P37 ‡
P51	P83 ‡
P52	P98 ‡
P53	P143 ‡
P54	P158 ‡
P102	P195
P104	P204 ‡
P105	P219 ‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

3/20/96

‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

Pin Locations for XC4025E, XC4028EX, & XC4028XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
VCC	P183	J4	P212	K1	P38	VCC*	-
I/O (A8)	P184	J3	P213	K2	P37	D14	98
I/O (A9)	P185	J2	P214	K3	P36	C14	101
I/O (A19)	P186	J1	P215	K5	P35	A15	104
I/O (A18)	P187	H1	P216	K4	P34	B15	107
I/O	P188	H2	P217	J1	P33	C15	110
I/O	P189	H3	P218	J2	P32	D15	113
I/O (A10)	P190	G1	P220	H1	P31	A16	116
I/O (A11)	P191	G2	P221	J3	P30	B16	119
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	J4	P29	C16	122
I/O	-	-	-	J5	P28	B17	125
I/O	-	-	-	H2	P27	C17	128
I/O	-	-	-	G1	P26	B18	131
VCC	-	-	P222	E1	P25	VCC*	-
I/O	-	H4	P223	H3	P23	C18	134
I/O	-	G4	P224	G2	P22	D17	137
I/O	P192	F1	P225	H4	P21	A20	140
I/O	P193	E1	P226	F2	P20	B19	143
GND	P194	G3	P227	F1	P19	GND*	-
I/O	-	-	-	H5	P18	C19	146
I/O	-	-	-	G3	P17	D18	149
I/O	P195	F2	P228	D1	P16	A21	152
I/O	P196	D1	P229	G4	P15	B20	155
I/O	P197	C1	P230	E2	P14	C20	158
I/O	P198	E2	P231	F3	P13	B21	161
I/O (A12)	P199	F3	P232	G5	P12	B22	164
I/O (A13)	P200	D2	P233	C1	P10	C21	167
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	F4	P9	D20	170
I/O	-	-	-	E3	P8	A23	173
I/O	-	F4	P234	D2	P7	D21	176
I/O	-	E4	P235	C2	P6	C22	179
I/O	P201	B1	P236	F5	P5	B24	182
I/O	P202	E3	P237	E4	P4	C23	185
I/O (A14)	P203	C2	P238	D3	P3	D22	188
I/O, SGCK1, GCK8 (A15)	P204	B2	P239	C3	P2	C24	191
VCC	P205	D3	P240	A2	P1	VCC*	-
GND	P2	D4	P1	B1	P304	GND*	-
I/O, PGCK1, GCK1 (A16)	P4	C3	P2	D4	P303	D23	194
I/O (A17)	P5	C4	P3	B2	P302	C25	197

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	P6	B3	P4	B3	P301	D24	200
I/O	P7	C5	P5	E6	P300	E23	203
I/O, TDI	P8	A2	P6	D5	P299	C26	206
I/O, TCK	P9	B4	P7	C4	P298	E24	209
I/O	-	-	-	A3	P297	F24	212
I/O	-	-	-	D6	P296	E25	215
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P10	C6	P8	E7	P295	D26	218
I/O	P11	A3	P9	B4	P294	G24	221
I/O	P12	B5	P10	C5	P293	F25	224
I/O	P13	B6	P11	A4	P292	F26	227
I/O	-	D5	P12	D7	P291	H23	230
I/O	-	D6	P13	C6	P290	H24	233
I/O	-	-	-	E8	P289	G25	236
I/O	-	-	-	B5	P288	G26	239
GND	P14	C7	P14	A5	P287	GND*	-
I/O, FCLK1	P15	A4	P15	B6	P286	J23	242
I/O	P16	A5	P16	D8	P285	J24	245
I/O, TMS	P17	B7	P17	C7	P284	H25	248
I/O	P18	A6	P18	B7	P283	K23	251
VCC	-	-	P19	A6	P282	VCC*	-
I/O	-	D7	P20	C8	P280	K24	254
I/O	-	D8	P21	E9	P279	J25	257
I/O	-	-	-	A7	P278	L24	260
I/O	-	-	-	D9	P277	K25	263
GND‡	-	-	P22	-	-	GND*	-
I/O	-	-	-	B8	P276	L25	266
I/O	-	-	-	A8	P275	L26	269
I/O	P19	C8	P23	C9	P274	M23	272
I/O	P20	A7	P24	B9	P273	M24	275
I/O	P21	B8	P25	E10	P272	M25	278
I/O	P22	A8	P26	A9	P271	M26	281
I/O	P23	B9	P27	D10	P270	N24	284
I/O	P24	C9	P28	C10	P269	N25	287
GND	P25	D9	P29	A10	P268	GND*	-
VCC	P26	D10	P30	A11	P267	VCC*	-
I/O	P27	C10	P31	B10	P266	N26	290
I/O	P28	B10	P32	B11	P265	P25	293
I/O	P29	A9	P33	C11	P264	P23	296
I/O	P30	A10	P34	E11	P263	P24	299
I/O	P31	A11	P35	D11	P262	R26	302
I/O	P32	C11	P36	A12	P261	R25	305
I/O	-	-	-	B12	P260	R24	308
I/O	-	-	-	A13	P259	R23	311
GND‡	-	-	P37	-	-	GND*	-
I/O	-	-	-	C12	P258	T26	314
I/O	-	-	-	D12	P257	T25	317
I/O	-	D11	P38	E12	P256	T23	320
I/O	-	D12	P39	B13	P255	V26	323
VCC	-	-	P40	A16	P253	VCC*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AM6	B6	26
I/O	AM2	A6	29
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	AL3	D8	32
I/O	AH6	C7	35
I/O	AP2	B7	38
I/O	AK4	D9	41
I/O	AN1	B8	44
I/O	AK2	A8	47
I/O	AG5	D10	50
I/O	AF6	C9	53
I/O	AL5	B9	56
I/O	AJ3	C10	59
GND	GND*	GND*	-
I/O	AH2	B10	62
I/O	AE5	A10	65
I/O	AM4	C11	68
I/O	AD6	D12	71
VCC	VCC*	VCC*	-
I/O	AG3	B11	74
I/O	AG1	C12	77
I/O	AC5	C13	80
I/O	AE1	A12	83
I/O	AH4	D14	86
I/O	AB6	B13	89
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A4)	AD2	C14	92
I/O (A5)	AB4	A13	95
I/O	AE3	B14	98
I/O	AC1	D15	101
I/O (A21)	AD4	C15	104
I/O (A20)	AA5	B15	107
I/O	AB2	A15	110
I/O	AC3	C16	113
I/O (A6)	AA3	B16	116
I/O (A7)	Y6	A16	119
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A8)	W3	D17	122
I/O (A9)	Y2	A17	125
I/O	V2	C17	128
I/O	W5	B17	131
I/O (A19)	V4	C18	134
I/O (A18)	T2	D18	137
I/O	U1	B18	140
I/O	V6	A19	143
I/O (A10)	U3	B19	146
I/O (A11)	R1	C19	149
VCC	VCC*	VCC*	-
GND	GND*	GND*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	U5	D19	152
I/O	T4	A20	155
I/O	P2	B20	158
I/O	N1	C20	161
I/O	R5	C21	164
I/O	M2	A22	167
VCC	VCC*	VCC*	-
I/O	L3	B22	170
I/O	T6	C22	173
I/O	N5	B23	176
I/O	M4	A24	179
GND	GND*	GND*	-
I/O	K2	D22	182
I/O	K4	C23	185
I/O	P6	B24	188
I/O	M6	C24	191
I/O	L5	D23	194
I/O	J5	B25	197
I/O	J3	A26	200
I/O	H2	C25	203
I/O (A12)	H4	D24	206
I/O (A13)	G3	B26	209
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	K6	A27	212
I/O	G1	D25	215
I/O	E1	C26	218
I/O	E3	B27	221
I/O	J7	C27	224
I/O	H6	B28	227
I/O	C3	D27	230
I/O	D2	B29	233
I/O (A14)	E5	C28	236
I/O, GCK8 (A15)	G7	D28	239
VCC	VCC*	VCC*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any specific package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any specific package pin.

XC4052XL Pad Name	PG411	BG432	Bndry Scan
I/O	AE39	AH13	703
I/O	AM36	AL12	706
I/O	AC35	AK12	709
I/O	AL35	AJ12	712
I/O	AF38	AK11	715
GND	GND*	GND*	-
I/O	AG39	AH12	718
I/O	AG37	AJ11	721
VCC	VCC*	VCC*	-
I/O	AD34	AL10	724
I/O	AN39	AK10	727
I/O	AE35	AJ10	730
I/O	AH38	AK9	733
GND	GND*	GND*	-
I/O	AJ37	AL8	736
I/O	AG35	AH10	739
I/O	AF34	AJ9	742
I/O	AH36	AK8	745
GND	GND*	GND*	-
I/O	AK38	AJ8	748
I/O	AP38	AH9	751
I/O	AK36	AK7	754
I/O	AM34	AL6	757
I/O	AH34	AJ7	760
I/O	AJ35	AH8	763
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AL37	AK6	766
I/O	AT38	AL5	769
I/O	AM38	AH7	772
I/O	AN37	AJ6	775
I/O	AK34	AK5	778
I/O	AR39	AL4	781
GND	GND*	GND*	-
I/O	AR37	AH6	784
I/O	AU37	AJ5	787
I/O	AN35	AK4	790
I/O	AL33	AH5	793
I/O	AV38	AK3	796
I/O, GCK4	AT36	AJ4	799
GND	GND*	GND*	-
DONE	AR35	AH4	-
VCC	VCC*	VCC*	-
$\overline{\text{PROGRAM}}$	AN33	AH3	-
I/O (D7)	AM32	AJ2	802
I/O, GCK5	AP34	AG4	805
I/O	AW39	AG3	808
I/O	AN31	AH2	811

XC4052XL Pad Name	PG411	BG432	Bndry Scan
I/O	AV36	AH1	814
I/O	AR33	AF4	817
GND	GND*	GND*	-
I/O	AP32	AF3	820
I/O	AU35	AG2	823
I/O	AV34	AG1	826
I/O	AW35	AE4	829
I/O	AW33	AE3	832
I/O	AU33	AF2	835
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D6)	AV32	AF1	838
I/O	AU31	AD4	841
I/O	AR31	AD3	844
I/O	AP28	AE2	847
I/O	AP30	AD2	850
I/O	AT30	AC4	853
GND	GND*	GND*	-
I/O	AT32	AC3	856
I/O	AV30	AD1	859
I/O	AR29	AC2	862
I/O	AP26	AB4	865
GND	GND*	GND*	-
I/O	AU29	AB3	868
I/O	AV28	AB2	871
I/O, FCLK3	AT28	AB1	874
I/O	AR25	AA3	877
VCC	VCC*	VCC*	-
I/O (D5)	AP24	AA2	880
I/O ($\overline{\text{CS0}}$)	AU27	Y2	883
GND	GND*	GND*	-
I/O	AR27	Y4	886
I/O	AW27	Y3	889
I/O	AU25	Y1	892
I/O	AV26	W1	895
I/O	AT24	W4	898
I/O	AR23	W3	901
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AW25	W2	904
I/O	AW23	V2	907
I/O	AP22	V4	910
I/O	AV24	V3	913
I/O	AU23	U1	916
I/O	AT22	U2	919
GND	GND*	GND*	-
I/O	AR21	U4	922
I/O	AV22	U3	925

PG299 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PG299 Pin	XC4025E	XC4028EX/XL
X1	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
X2	GND	GND
X3	I/O	I/O
X4	I/O	I/O
X5	VCC	VCC
X6	GND	GND
X7	I/O	I/O
X8	I/O	I/O
X9	I/O	I/O
X10	VCC	VCC
X11	GND	GND
X12	I/O	I/O
X13	I/O	I/O
X14	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
X15	VCC	VCC
X16	GND	GND
X17	I/O	I/O
X18	I/O	I/O
X19	VCC	VCC
X20	I/O, SGCK3	I/O, GCK4
W1	VCC	VCC
W2	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O, FCLK4
W8	I/O (D2)	I/O (D2)
W9	I/O	I/O
W10	I/O (D3)	I/O (D3)
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O, FCLK3
W15	I/O	I/O
W16	I/O	I/O
W17	I/O (D6)	I/O (D6)
W18	I/O, PGCK3	I/O, GCK5
W19	I/O (D7)	I/O (D7)
W20	GND	GND
V1	I/O (A3)	I/O (A3)
V2	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
V3	CCLK	CCLK
V4	I/O (D0, DIN)	I/O (D0, DIN)
V5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
V11	I/O (D4)	I/O (D4)
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	I/O	I/O
V18	DONE	DONE
V19	I/O	I/O
V20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O (CS1, A2)	I/O (CS1, A2)
U4	O, TDO	O, TDO
U5	I/O	I/O
U6	I/O (D1)	I/O (D1)
U7	I/O	I/O
U8	I/O	I/O
U9	I/O	I/O
U10	I/O	I/O
U11	I/O	I/O
U12	I/O	I/O
U13	I/O	I/O
U14	I/O	I/O
U15	I/O	I/O
U16	I/O	I/O
U17	$\overline{PROGRAM}$	$\overline{PROGRAM}$
U18	I/O	I/O
U19	I/O	I/O
U20	I/O	I/O
T1	GND	GND
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	GND	GND
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	I/O	I/O
T11	I/O	I/O
T12	I/O (D5)	I/O (D5)
T13	I/O	I/O
T14	I/O	I/O
T15	I/O	I/O
T16	VCC	VCC
T17	I/O	I/O
T18	I/O	I/O
T19	I/O	I/O
T20	VCC	VCC

PG299 Pin	XC4025E	XC4028EX/XL
R1	VCC	VCC
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R16	I/O	I/O
R17	I/O	I/O
R18	I/O	I/O
R19	I/O	I/O
R20	GND	GND
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
N1	I/O (A4)	I/O (A4)
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N16	I/O	I/O
N17	I/O	I/O
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
M1	I/O	I/O (A21)
M2	I/O	I/O
M3	I/O (A5)	I/O (A5)
M4	I/O	I/O
M5	I/O	I/O
M16	I/O	I/O
M17	I/O	I/O
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
L1	GND	GND
L2	I/O (A7)	I/O (A7)
L3	I/O (A6)	I/O (A6)
L4	I/O	I/O (A20)
L5	I/O	I/O
L16	I/O	I/O
L17	I/O	I/O
L18	I/O	I/O
L19	I/O	I/O
L20	VCC	VCC
K1	VCC	VCC
K2	I/O (A8)	I/O (A8)
K3	I/O (A9)	I/O (A9)

PG299 Pin	XC4025E	XC4028EX/XL
K4	I/O	I/O (A18)
K5	I/O	I/O (A19)
K16	I/O	I/O
K17	I/O	I/O
K18	I/O	I/O
K19	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
K20	GND	GND
J1	I/O	I/O
J2	I/O	I/O
J3	I/O (A11)	I/O (A11)
J4	I/O	I/O
J5	I/O	I/O
J16	I/O	I/O
J17	I/O	I/O
J18	I/O	I/O
J19	I/O	I/O
J20	I/O	I/O
H1	I/O (A10)	I/O (A10)
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H16	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O (A12)	I/O (A12)
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
F1	GND	GND
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	VCC	VCC
E1	VCC	VCC
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	VCC	VCC
E6	I/O	I/O

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P99	I/O	I/O	I/O
P100	N.C.	N.C.	N.C.
P101	VCC	VCC	VCC
P102	I/O	I/O	I/O
P103	I/O (D2)	I/O (D2)	I/O (D2)
P104	I/O	I/O	I/O
P105	I/O	I/O	I/O
P106	I/O	I/O	I/O
P107	I/O	I/O	I/O
P108	I/O	I/O	I/O
P109	I/O	I/O	I/O
P110	I/O	I/O	I/O
P111	I/O	I/O	I/O
P112	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P113	I/O (D3)	I/O (D3)	I/O (D3)
P114	GND	GND	GND
P115	VCC	VCC	VCC
P116	I/O	I/O	I/O
P117	I/O (D4)	I/O (D4)	I/O (D4)
P118	I/O	I/O	I/O
P119	I/O	I/O	I/O
P120	I/O	I/O	I/O
P121	I/O	I/O	I/O
P122	I/O	I/O	I/O
P123	I/O	I/O	I/O
P124	I/O	I/O	I/O
P125	I/O	I/O	I/O
P126	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P127	I/O (D5)	I/O (D5)	I/O (D5)
P128	N.C.	N.C.	N.C.
P129	VCC	VCC	VCC
P130	I/O	I/O	I/O
P131	I/O	I/O, FCLK3	I/O, FCLK3
P132	I/O	I/O	I/O
P133	I/O	I/O	I/O
P134	GND	GND	GND
P135	I/O	I/O	I/O
P136	I/O	I/O	I/O
P137	I/O	I/O	I/O
P138	I/O	I/O	I/O
P139	I/O	I/O	I/O
P140	I/O	I/O	I/O
P141	I/O	I/O	I/O
P142	I/O (D6)	I/O (D6)	I/O (D6)
P143	I/O	I/O	I/O
P144	I/O	I/O	I/O
P145	I/O	I/O	I/O
P146	I/O	I/O	I/O
P147	I/O	I/O	I/O
P148	I/O	I/O	I/O
P149	I/O, PGCK3	I/O, GCK5	I/O, GCK5
P150	I/O (D7)	I/O (D7)	I/O (D7)
P151	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P152	VCC	VCC	VCC
P153	DONE	DONE	DONE
P154	GND	GND	GND
P155	I/O, SGCK3	I/O, GCK4	I/O, GCK4
P156	I/O	I/O	I/O
P157	I/O	I/O	I/O
P158	I/O	I/O	I/O
P159	I/O	I/O	I/O
P160	I/O	I/O	I/O
P161	I/O	I/O	I/O
P162	I/O	I/O	I/O
P163	I/O	I/O	I/O
P164	I/O	I/O	I/O
P165	I/O	I/O	I/O
P166	I/O	I/O	I/O
P167	I/O	I/O	I/O
P168	I/O	I/O	I/O
P169	I/O	I/O	I/O
P170	I/O	I/O	I/O
P171	GND	GND	GND
P172	I/O	I/O	I/O
P173	I/O	I/O	I/O
P174	I/O	I/O	I/O
P175	I/O	I/O	I/O
P176	N.C.	N.C.	N.C.
P177	VCC	VCC	VCC
P178	I/O	I/O	I/O
P179	I/O	I/O	I/O
P180	I/O	I/O	I/O
P181	I/O	I/O	I/O
P182	I/O	I/O	I/O
P183	I/O	I/O	I/O
P184	I/O	I/O	I/O
P185	I/O	I/O	I/O
P186	I/O	I/O	I/O
P187	I/O	I/O	I/O
P188	I/O	I/O	I/O
P189	I/O	I/O	I/O
P190	GND	GND	GND
P191	VCC	VCC	VCC
P192	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P193	I/O	I/O	I/O
P194	I/O	I/O	I/O
P195	I/O	I/O	I/O
P196	I/O	I/O	I/O
P197	I/O	I/O	I/O
P198	I/O	I/O	I/O
P199	I/O	I/O	I/O
P200	I/O	I/O	I/O
P201	I/O	I/O	I/O
P202	I/O	I/O	I/O
P203	I/O	I/O	I/O
P204	VCC	VCC	VCC

PG411 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PG411 Pin	XC4036EX/XL	XC4044EX/XL	XC4052XL
AW1	I/O	I/O	I/O
AW3	GND	GND	GND
AW5	I/O	I/O	I/O
AW7	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
AW9	VCC	VCC	VCC
AW11	GND	GND	GND
AW13	I/O	I/O	I/O
AW15	N.C.	I/O	I/O
AW17	I/O	I/O	I/O
AW19	VCC	VCC	VCC
AW21	GND	GND	GND
AW23	N.C.	I/O	I/O
AW25	N.C.	I/O	I/O
AW27	I/O	I/O	I/O
AW29	VCC	VCC	VCC
AW31	GND	GND	GND
AW33	I/O	I/O	I/O
AW35	N.C.	N.C.	I/O
AW37	VCC	VCC	VCC
AW39	I/O	I/O	I/O
AV2	I/O, GCK7 (A1)	I/O, GCK7 (A1)	I/O, GCK7 (A1)
AV4	I/O	I/O	I/O
AV6	I/O	I/O	I/O
AV8	N.C.	I/O	I/O
AV10	I/O	I/O	I/O
AV12	I/O	I/O	I/O
AV14	I/O	I/O	I/O
AV16	I/O	I/O	I/O
AV18	I/O	I/O	I/O
AV20	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
AV22	I/O	I/O	I/O
AV24	I/O	I/O	I/O
AV26	N.C.	N.C.	I/O
AV28	I/O	I/O	I/O
AV30	I/O	I/O	I/O
AV32	I/O (D6)	I/O (D6)	I/O (D6)
AV34	N.C.	N.C.	I/O
AV36	I/O	I/O	I/O
AV38	I/O	I/O	I/O
AU1	VCC	VCC	VCC
AU3	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
AU5	N.C.	N.C.	I/O
AU7	I/O (D1)	I/O (D1)	I/O (D1)
AU9	N.C.	I/O	I/O
AU11	I/O	I/O	I/O
AU13	N.C.	N.C.	I/O
AU15	N.C.	N.C.	I/O
AU17	N.C.	I/O	I/O
AU19	I/O (D3)	I/O (D3)	I/O (D3)
AU21	I/O	I/O	I/O
AU23	I/O	I/O	I/O
AU25	N.C.	N.C.	I/O
AU27	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
AU29	I/O	I/O	I/O
AU31	I/O	I/O	I/O
AU33	I/O	I/O	I/O
AU35	I/O	I/O	I/O
AU37	N.C.	N.C.	I/O
AU39	GND	GND	GND
AT2	N.C.	N.C.	I/O
AT4	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
AT6	GND	GND	GND
AT8	I/O	I/O	I/O
AT10	I/O	I/O	I/O
AT12	I/O	I/O	I/O
AT14	GND	GND	GND
AT16	I/O	I/O	I/O
AT18	I/O	I/O	I/O
AT20	GND	GND	GND
AT22	I/O	I/O	I/O
AT24	I/O	I/O	I/O
AT26	GND	GND	GND
AT28	I/O, FCLK3	I/O, FCLK3	I/O, FCLK3
AT30	N.C.	I/O	I/O
AT32	I/O	I/O	I/O
AT34	VCC	VCC	VCC
AT36	I/O, GCK4	I/O, GCK4	I/O, GCK4
AT38	I/O	I/O	I/O
AR1	I/O	I/O	I/O
AR3	I/O	I/O	I/O
AR5	CCLK	CCLK	CCLK
AR7	I/O	I/O	I/O
AR9	I/O	I/O	I/O
AR11	I/O	I/O	I/O
AR13	I/O, FCLK4	I/O, FCLK4	I/O, FCLK4
AR15	I/O (D2)	I/O (D2)	I/O (D2)
AR17	I/O	I/O	I/O
AR19	I/O	I/O	I/O
AR21	I/O	I/O	I/O
AR23	I/O	I/O	I/O
AR25	I/O	I/O	I/O
AR27	I/O	I/O	I/O
AR29	I/O	I/O	I/O
AR31	I/O	I/O	I/O
AR33	I/O	I/O	I/O
AR35	DONE	DONE	DONE
AR37	N.C.	N.C.	I/O
AR39	I/O	I/O	I/O
AP2	I/O	I/O	I/O
AP4	VCC	VCC	VCC