AMD Xilinx - XC4013L-5PQ208C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	160
Number of Gates	13000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc4013l-5pq208c

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 15.

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See Figure 33 on page 39.)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in "Wide Edge Decoders" on page 31.

Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

Three-State Buffer Examples

Figure 22 shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

Figure 23 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 15.

Table 15: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

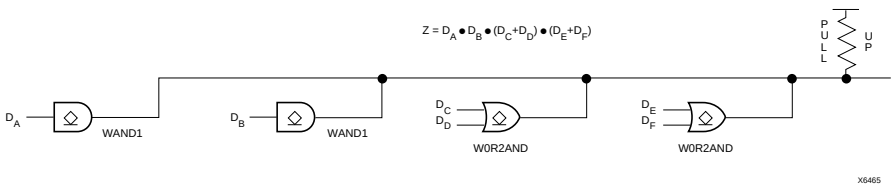


Figure 22: Open-Drain Buffers Implement a Wired-AND Function

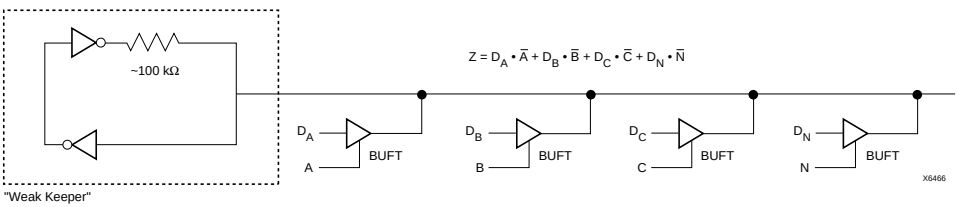


Figure 23: 3-State Buffers Implement a Multiplexer

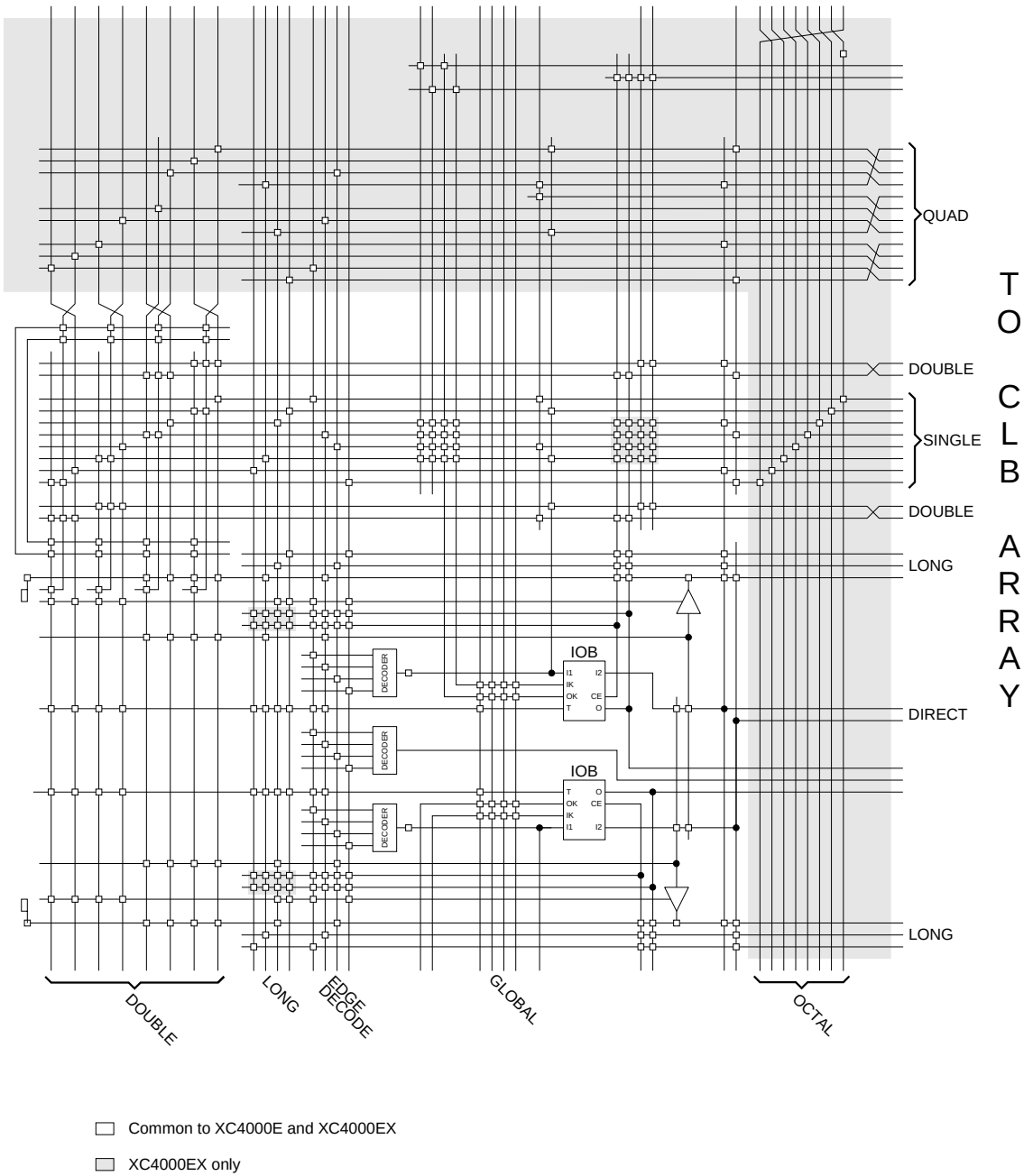


Figure 33: Detail of Programmable Interconnect Associated with XC4000-Series IOB (Left Edge)

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	I	I	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode, Synchronous Peripheral mode, and Express mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC4000-Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 65 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in MakeBits, the XACT*step* program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
User I/O Pins That Can Have Special Functions			
RDY/$\overline{\text{BUSY}}$	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/$\overline{\text{BUSY}}$ is a user-programmable I/O pin. RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High.
$\overline{\text{RCLK}}$	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000EX) is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 kΩ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000EX only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
FCLK1 - FCLK4 (XC4000EX only)	Weak Pull-up	I or I/O	Four FCLK inputs can each drive a FastCLK buffer. The FastCLK buffers cannot be driven from internal logic. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFFCLK symbol is automatically placed on one of these pins.

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT*step* development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC4000E devices have six configuration modes. XC4000EX devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC4000EX devices. The coding for mode selection is shown in Table 20.

Table 20: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express (XC4000EX only)	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 24 on page 78.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz (up to 10% lower for low-voltage devices). Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/$\overline{\text{BUSY}}$ status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the syn-

Table 22: XC4000E Program Data

Device	XC4003E	XC4005E/L	XC4006E	XC4008E	XC4010E/L	XC4013E/L	XC4020E	XC4025E
Max Logic Gates	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLBs (Row x Col.)	100 (10 x 10)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)
IOBs	80	112	128	144	160	192	224	256
Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Horizontal Longlines	20	28	32	36	40	48	56	64
TBUFs per Longline	12	16	18	20	22	26	30	34
Bits per Frame	126	166	186	206	226	266	306	346
Frames	428	572	644	716	788	932	1,076	1,220
Program Data	53,936	94,960	119,792	147,504	178,096	247,920	329,264	422,128
PROM Size (bits)	53,984	95,008	119,840	147,552	178,144	247,968	329,312	422,176

Notes:
1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
   Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
   Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
   PROM Size = Program Data + 40
2. The user can add more “one” bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra “one” bits, even for extra leading ones at the beginning of the header.

The MakeBits software creates the configuration bitstream. In Express mode, only non-CRC error checking is supported. In all other modes, MakeBits allows a selection of CRC or non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, MakeBits calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 21. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 47. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture MakeBits option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Configuration

The 0010 preamble code, included for all modes except Express mode, indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device. In Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 48 on page 59.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The XC4000-Series $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 49 describes start-up timing for the three Xilinx families in detail. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, the other configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events — DONE going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in MakeBits, the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 49, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

The XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{\text{INIT}}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 50. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called “Start-up Timing Synchronous to Done In” and is selected by the CCLK_SYNC and UCLK_SYNC MakeBits options.

When DONE is not used as an input, the operation is called “Start-up Timing Not Synchronous to DONE In,” and is selected by the CCLK_NOSYNC and UCLK_NOSYNC MakeBits options.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 49 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

In all configuration modes except Express mode, XC4000-Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly.*

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [$2^{24} * $ CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

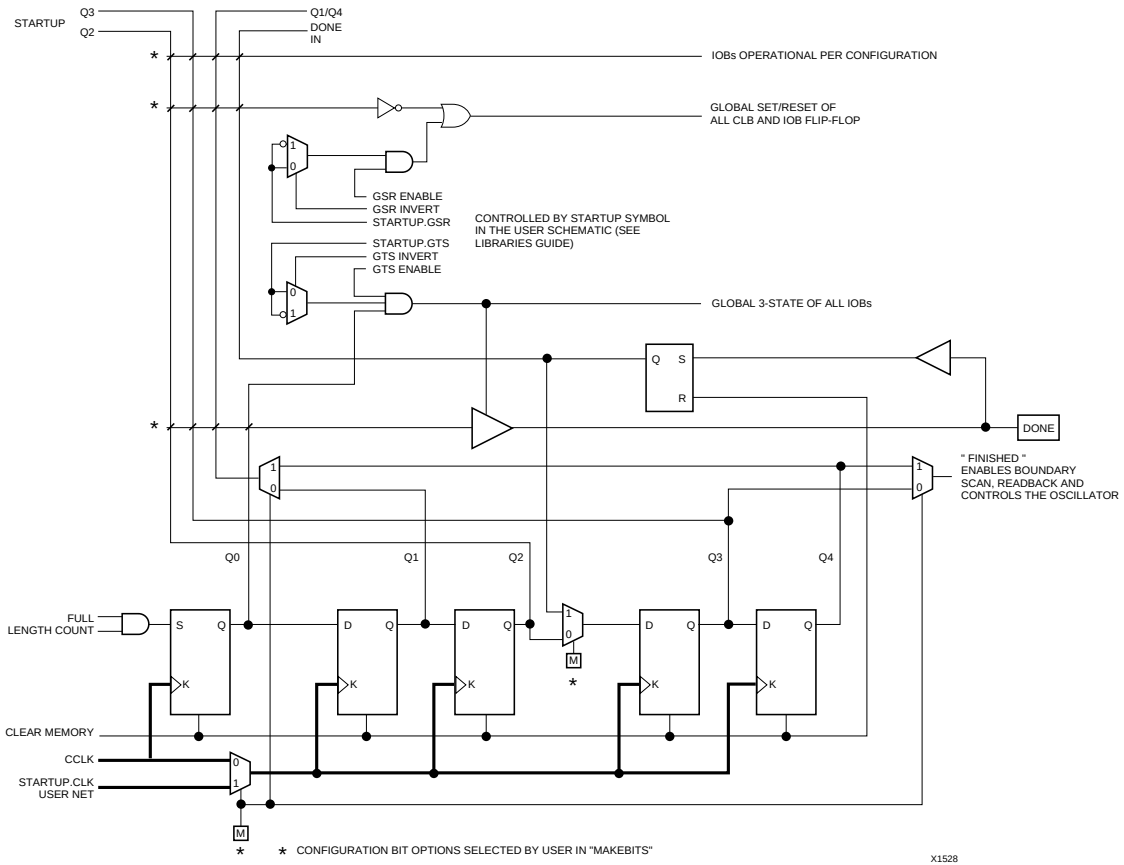


Figure 50: Start-up Logic

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by MakeBits, the bitstream generation software.

Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 kΩ - 100 kΩ pull-up. The delay from DONE High to active user I/O is controlled by a MakeBits option.

Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by a MakeBits option.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 49 on page 61. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC4000-Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 Devices*." This application note also applies to XC4000E and XC4000EX devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000-Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

Readback of Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

XC4000-Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 51.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

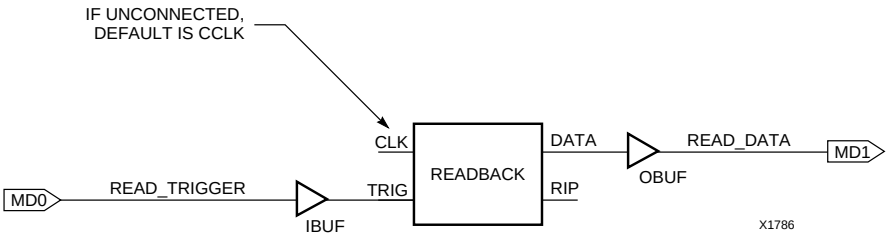


Figure 51: Readback Schematic Example

Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

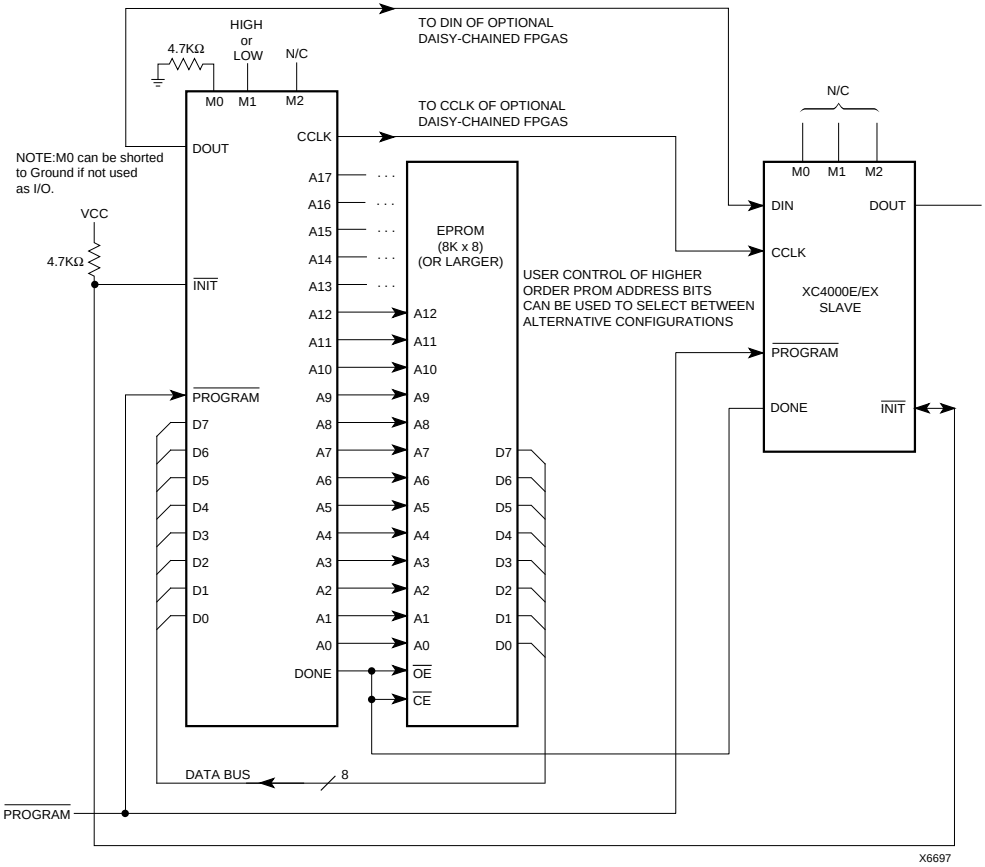


Figure 57: Master Parallel Mode Circuit Diagram

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.
Note 3: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	TTL input levels		10	mA
		CMOS input levels		1	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4		ns
		XC4005E	5.0	5.0	4.0		ns
		XC4006E	6.0	5.9	4.7		ns
		XC4008E	7.0	6.3	5.0		ns
		XC4010E	8.0	6.4	5.1		ns
		XC4013E	9.0	7.2	5.7		ns
		XC4020E	10.0	8.2	7.3		ns
		XC4025E	11.0	9.1	7.3		ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6		ns
		XC4005E	6.0	5.3	4.5		ns
		XC4006E	7.8	6.4	5.4		ns
		XC4008E	8.1	6.8	5.8		ns
		XC4010E	10.5	6.9	5.9		ns
		XC4013E	11.0	7.7	6.5		ns
		XC4020E	12.0	8.7	8.7		ns
		XC4025E	12.0	9.6	9.6		ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9		ns
		XC4005E	7.0	6.0	5.7		ns
		XC4006E	7.5	6.7	5.7		ns
		XC4008E	8.0	7.1	6.0		ns
		XC4010E	8.5	7.3	6.2		ns
		XC4013E	8.7	7.5	7.0		ns
		XC4020E	11.0	8.4	7.1		ns
		XC4025E	11.0	8.4	7.1		ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3		ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T_{PUS}	XC4003E	20.0	14.0	14.0		ns
		XC4005E	23.0	16.0	16.0		ns
		XC4006E	25.0	18.0	18.0		ns
		XC4008E	27.0	20.0	20.0		ns
		XC4010E	29.0	22.0	22.0		ns
		XC4013E	32.0	26.0	26.0		ns
		XC4020E	35.0	32.5	32.5		ns
		XC4025E	42.0	39.1	39.1		ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0		ns
		XC4005E	10.0	8.0	6.8		ns
		XC4006E	11.5	9.0	7.7		ns
		XC4008E	12.5	10.0	8.5		ns
		XC4010E	13.5	11.0	9.4		ns
		XC4013E	15.0	13.0	11.7		ns
		XC4020E	16.0	14.8	14.8		ns
		XC4025E	18.0	16.5	16.5		ns
					Preliminary		

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

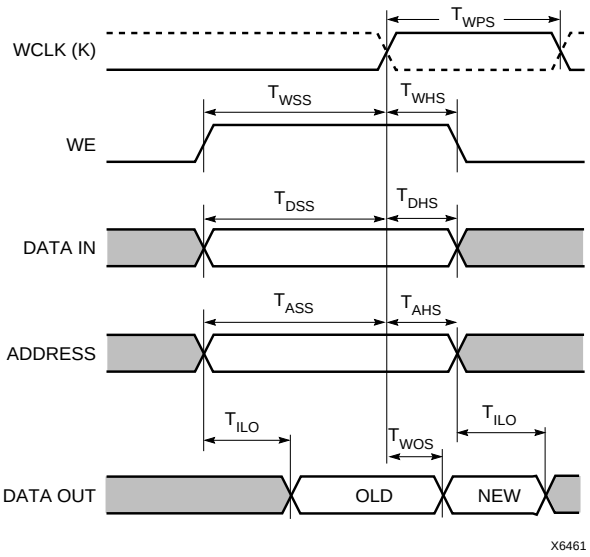
XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Operation										
Address write cycle time	16x2	T_{WCS}	15.0		14.4		11.6			
(clock K period)	32x1	T_{WCTS}	15.0		14.4		11.6			
Clock K pulse width	16x2	T_{WPS}	7.5	1 ms	7.2	1 ms	5.8	1 ms		
(active edge)	32x1	T_{WPTS}	7.5	1 ms	7.2	1 ms	5.8	1 ms		
Address setup time	16x2	T_{ASS}	2.8		2.4		2.0			
before clock K	32x1	T_{ASTS}	2.8		2.4		2.0			
Address hold time	16x2	T_{AHS}	0		0		0			
after clock K	32x1	T_{AHTS}	0		0		0			
DIN setup time	16x2	T_{DSS}	3.5		3.2		2.7			
before clock K	32x1	T_{DSTS}	2.5		1.9		1.7			
DIN hold time	16x2	T_{DHS}	0		0		0			
after clock K	32x1	T_{DHTS}	0		0		0			
WE setup time	16x2	T_{WSS}	2.2		2.0		1.6			
before clock K	32x1	T_{WSTS}	2.2		2.0		1.6			
WE hold time	16x2	T_{WHS}	0		0		0			
after clock K	32x1	T_{WHTS}	0		0		0			
Data valid	16x2	T_{WOS}		10.3		8.8		7.9		
after clock K	32x1	T_{WOTS}		11.6		10.3		9.3		
							Preliminary			

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.



XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	R4	P68	B5	20
I/O	-	-	-	P5	P67	A4	23
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	-	P4	P189	U2	P66	C7	26
I/O	-	N4	P190	T3	P65	B6	29
I/O	P167	P2	P191	U1	P64	A6	32
I/O	P168	T1	P192	P4	P63	D8	35
I/O	P169	R1	P193	R3	P62	B7	38
I/O	P170	N2	P194	N5	P61	A7	41
I/O	-	-	P195	T2	P60	D9	44
I/O	-	-	-	R2	P59	C9	47
GND	P171	M3	P196	T1	P58	GND*	-
I/O	P172	P1	P197	N4	P57	B8	50
I/O	P173	N1	P198	P3	P56	D10	53
I/O	-	M4	P199	P2	P55	C10	56
I/O	-	L4	P200	N3	P54	B9	59
VCC	-	-	P201	R1	P52	VCC*	-
I/O	-	-	-	M5	P51	A9	62
I/O	-	-	-	P1	P50	D11	65
I/O	-	-	-	M4	P49	B11	68
I/O	-	-	-	N2	P48	A11	71
GND	-	-	-	-	-	GND*	-
I/O (A4)	P174	M2	P202	N1	P47	D12	74
I/O (A5)	P175	M1	P203	M3	P46	C12	77
I/O	P176	L3	P205	M2	P45	B12	80
I/O	P177	L2	P206	L5	P44	A12	83
I/O (A21)	P178	L1	P207	M1	P43	C13	86
I/O (A20)	P179	K1	P208	L4	P42	B13	89
I/O (A6)	P180	K2	P209	L3	P41	A13	92
I/O (A7)	P181	K3	P210	L2	P40	B14	95
GND	P182	K4	P211	L1	P39	GND*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the BG352 package. They have no direct connection to any specific package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the BG352 package. They have no direct connection to any specific package pin.

Pads labelled GND‡ should be connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ208 Package

N.C.	N.C.
P1	P107
P3	P155
P51	P156
P52	P157
P53	P158
P54	P206
P102	P207
P104	P208
P105	

3/15/96

Additional Ground (GND) Connections on HQ240 Package

GND
P204
P219

3/21/96

The Ground (GND) package pins in the above table should be externally connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ304 Package

N.C.
P11
P24
P53
P100
P128
P176
P205
P254
P281

3/21/96

Note: In XC4025 (no extension) devices in the HQ304 package, P101 is a No Connect (N.C.) pin. P101 is Vcc in XC4025E/L and XC4028EX/XL devices. Where necessary for compatibility, this pin can be left unconnected.

Package-Specific Pinout Tables

PC84 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

Pin	XC4003E	XC4005E XC4005L	XC4006E	XC4008E	XC4010E XC4010L
P1	GND	GND	GND	GND	GND
P2	VCC	VCC	VCC	VCC	VCC
P3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P4	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P5	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P6	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P7	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P8	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P9	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P10	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P11	VCC	VCC	VCC	VCC	VCC
P12	GND	GND	GND	GND	GND
P13	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P14	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P15	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P16	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O
P19	I/O	I/O	I/O	I/O	I/O
P20	I/O	I/O	I/O	I/O	I/O
P21	GND	GND	GND	GND	GND
P22	VCC	VCC	VCC	VCC	VCC
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P30	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P31	GND	GND	GND	GND	GND
P32	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P33	VCC	VCC	VCC	VCC	VCC
P34	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P35	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P36	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P37	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P38	I/O	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O	I/O
P40	I/O	I/O	I/O	I/O	I/O
P41	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P42	VCC	VCC	VCC	VCC	VCC
P43	GND	GND	GND	GND	GND
P44	I/O	I/O	I/O	I/O	I/O
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P52	GND	GND	GND	GND	GND
P53	DONE	DONE	DONE	DONE	DONE
P54	VCC	VCC	VCC	VCC	VCC
P55	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P56	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P59	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P60	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P61	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P62	I/O	I/O	I/O	I/O	I/O
P63	VCC	VCC	VCC	VCC	VCC
P64	GND	GND	GND	GND	GND
P65	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P66	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P67	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P70	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P71	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P72	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P73	CCLK	CCLK	CCLK	CCLK	CCLK
P74	VCC	VCC	VCC	VCC	VCC
P75	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P76	GND	GND	GND	GND	GND
P77	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P78	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P79	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P80	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P81	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P82	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P83	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P84	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)

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BG225 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

BG225 Pin	XC4010E	XC4013E/L
R1	VCC	VCC
R2	I/O, PGCK2	I/O, PGCK2
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	VCC
R9	I/O	I/O
R10	N.C.	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	VCC	VCC
P1	I/O, SCGK2	I/O, SCGK2
P2	I (M0)	I (M0)
P3	I/O (HDC)	I/O (HDC)
P4	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P5	N.C.	I/O
P6	I/O	I/O
P7	N.C.	I/O
P8	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P9	I/O	I/O
P10	N.C.	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	DONE	DONE
P15	I/O (D7)	I/O (D7)
N1	I/O	I/O
N2	I/O	I/O
N3	O (M1)	O (M1)
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	N.C.	I/O
N8	I/O	I/O
N9	I/O	I/O
N10	I/O	I/O
N11	N.C.	I/O
N12	I/O	I/O
N13	I/O, SGCK3	I/O, SGCK3
N14	I/O, PGCK3	I/O, PGCK3
N15	N.C.	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I (M2)	I (M2)
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	N.C.	I/O
M11	I/O	I/O
M12	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
M13	I/O	I/O
M14	N.C.	I/O
M15	I/O	I/O
L1	I/O	I/O
L2	N.C.	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	N.C.	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	N.C.	I/O
K1	N.C.	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	N.C.	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	GND	GND
K9	I/O	I/O
K10	I/O	I/O
K11	I/O	I/O
K12	N.C.	I/O
K13	I/O	I/O
K14	I/O	I/O
K15	I/O (D5)	I/O (D5)
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	N.C.	I/O
J6	I/O	I/O
J7	GND	GND
J8	GND	GND
J9	GND	GND
J10	I/O (D6)	I/O (D6)
J11	I/O	I/O
J12	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
J13	I/O	I/O
J14	I/O	I/O
J15	I/O	I/O
H1	VCC	VCC
H2	GND	GND
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	GND	GND
H7	GND	GND
H8	GND	GND
H9	GND	GND
H10	GND	GND

BG225 Pin	XC4010E	XC4013E/L
H11	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
H12	I/O (D3)	I/O (D3)
H13	I/O (D4)	I/O (D4)
H14	I/O	I/O
H15	VCC	VCC
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	GND	GND
G8	GND	GND
G9	GND	GND
G10	N.C.	I/O
G11	I/O (D2)	I/O (D2)
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
F1	N.C.	I/O
F2	N.C.	I/O
F3	I/O	I/O
F4	I/O, TMS	I/O, TMS
F5	I/O	I/O
F6	I/O	I/O
F7	N.C.	I/O
F8	GND	GND
F9	N.C.	I/O
F10	I/O (D0, DIN)	I/O (D0, DIN)
F11	I/O	I/O
F12	N.C.	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
E1	I/O	I/O
E2	N.C.	I/O
E3	N.C.	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O (A8)	I/O (A8)
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O (D1)	I/O (D1)
E13	I/O	I/O
E14	N.C.	I/O
E15	N.C.	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O, TDI	I/O, TDI
D4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
D5	I/O (A13)	I/O (A13)
D6	I/O	I/O
D7	I/O	I/O
D8	VCC	VCC
D9	I/O (A5)	I/O (A5)
D10	I/O	I/O
D11	N.C.	I/O

BG225 Pin	XC4010E	XC4013E/L
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
C1	I/O, TCK	I/O, TCK
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
C4	N.C.	I/O
C5	I/O	I/O
C6	N.C.	I/O
C7	I/O	I/O
C8	I/O (A6)	I/O (A6)
C9	I/O	I/O
C10	N.C.	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	CCLK	CCLK
C14	I/O	I/O
C15	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
B1	I/O (A17)	I/O (A17)
B2	VCC	VCC
B3	I/O	I/O
B4	I/O (A12)	I/O (A12)
B5	I/O	I/O
B6	I/O (A11)	I/O (A11)
B7	I/O (A9)	I/O (A9)
B8	I/O (A7)	I/O (A7)
B9	I/O	I/O
B10	N.C.	I/O
B11	I/O	I/O
B12	I/O (A3)	I/O (A3)
B13	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
B14	VCC	VCC
B15	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
A1	GND	GND
A2	I/O (A14)	I/O (A14)
A3	N.C.	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O (A10)	I/O (A10)
A7	I/O	I/O
A8	GND	GND
A9	I/O	I/O
A10	I/O (A4)	I/O (A4)
A11	I/O	I/O
A12	I/O	I/O
A13	I/O (CS1, A2)	I/O (CS1, A2)
A14	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
A15	O, TDO	O, TDO

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PQ240, HQ240 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P1	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	I/O	I/O	I/O	I/O
P9	I/O	I/O	I/O	I/O
P10	I/O	I/O	I/O	I/O
P11	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O
P13	I/O	I/O	I/O	I/O
P14	GND	GND	GND	GND
P15	I/O	I/O	I/O	I/O, FCLK1
P16	I/O	I/O	I/O	I/O
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O
P19	VCC	VCC	VCC	VCC
P20	I/O	I/O	I/O	I/O
P21	I/O	I/O	I/O	I/O
P22	N.C.‡	N.C.‡	N.C.‡	GND‡
P23	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND
P30	VCC	VCC	VCC	VCC
P31	I/O	I/O	I/O	I/O
P32	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O
P37	N.C.‡	N.C.‡	N.C.‡	GND‡
P38	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O
P40	VCC	VCC	VCC	VCC
P41	I/O	I/O	I/O	I/O
P42	I/O	I/O	I/O	I/O
P43	I/O	I/O	I/O	I/O
P44	I/O	I/O	I/O	I/O, FCLK2
P45	GND	GND	GND	GND
P46	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O
P51	I/O	I/O	I/O	I/O
P52	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O
P57	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, GCK2
P58	O (M1)	O (M1)	O (M1)	O (M1)
P59	GND	GND	GND	GND
P60	I (M0)	I (M0)	I (M0)	I (M0)
P61	VCC	VCC	VCC	VCC
P62	I (M2)	I (M2)	I (M2)	I (M2)
P63	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, GCK3
P64	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P65	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O
P68	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P69	I/O	I/O	I/O	I/O
P70	I/O	I/O	I/O	I/O
P71	I/O	I/O	I/O	I/O
P72	I/O	I/O	I/O	I/O
P73	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O
P75	GND	GND	GND	GND
P76	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O
P78	I/O	I/O	I/O	I/O
P79	I/O	I/O	I/O	I/O
P80	VCC	VCC	VCC	VCC
P81	I/O	I/O	I/O	I/O
P82	I/O	I/O	I/O	I/O
P83	N.C.‡	N.C.‡	N.C.‡	GND‡
P84	I/O	I/O	I/O	I/O
P85	I/O	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
D27	I/O	I/O	I/O
D28	I/O, GCK8 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
D29	I/O, GCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
D30	I/O, TDI	I/O, TDI	I/O, TDI
D31	I/O, TCK	I/O, TCK	I/O, TCK
C1	GND	GND	GND
C2	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
C3	VCC	VCC	VCC
C4	O, TDO	O, TDO	O, TDO
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	N.C.	N.C.	N.C.
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O (A4)	I/O (A4)	I/O (A4)
C15	I/O (A21)	I/O (A21)	I/O (A21)
C16	N.C.	I/O	I/O
C17	N.C.	I/O	I/O
C18	I/O (A19)	I/O (A19)	I/O (A19)
C19	I/O (A11)	I/O (A11)	I/O (A11)
C20	I/O	I/O	I/O
C21	I/O	I/O	I/O
C22	I/O	I/O	I/O
C23	I/O	I/O	I/O
C24	I/O	I/O	I/O
C25	I/O	I/O	I/O
C26	I/O	I/O	I/O
C27	I/O	I/O	I/O
C28	I/O (A14)	I/O (A14)	I/O (A14)
C29	VCC	VCC	VCC
C30	I/O (A17)	I/O (A17)	I/O (A17)
C31	GND	GND	GND
B1	GND	GND	GND
B2	GND	GND	GND
B3	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	N.C.	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	I/O	I/O	I/O
B12	N.C.	N.C.	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	I/O (A20)	I/O (A20)	I/O (A20)
B16	I/O (A6)	I/O (A6)	I/O (A6)
B17	N.C.	I/O	I/O
B18	I/O	I/O	I/O
B19	I/O (A10)	I/O (A10)	I/O (A10)

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
B20	I/O	I/O	I/O
B21	N.C.	N.C.	I/O
B22	I/O	I/O	I/O
B23	I/O	I/O	I/O
B24	I/O	I/O	I/O
B25	N.C.	I/O	I/O
B26	I/O (A13)	I/O (A13)	I/O (A13)
B27	I/O	I/O	I/O
B28	I/O	I/O	I/O
B29	I/O	I/O	I/O
B30	GND	GND	GND
B31	GND	GND	GND
A1	VCC	VCC	VCC
A2	GND	GND	GND
A3	GND	GND	GND
A4	N.C.	N.C.	I/O
A5	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
A6	I/O	I/O	I/O
A7	GND	GND	GND
A8	N.C.	I/O	I/O
A9	GND	GND	GND
A10	I/O	I/O	I/O
A11	VCC	VCC	VCC
A12	I/O	I/O	I/O
A13	I/O (A5)	I/O (A5)	I/O (A5)
A14	GND	GND	GND
A15	N.C.	I/O	I/O
A16	I/O (A7)	I/O (A7)	I/O (A7)
A17	I/O (A9)	I/O (A9)	I/O (A9)
A18	GND	GND	GND
A19	I/O	I/O	I/O
A20	I/O	I/O	I/O
A21	VCC	VCC	VCC
A22	I/O	I/O	I/O
A23	GND	GND	GND
A24	I/O	I/O	I/O
A25	GND	GND	GND
A26	I/O	I/O	I/O
A27	I/O	I/O	I/O
A28	N.C.	N.C.	I/O
A29	GND	GND	GND
A30	GND	GND	GND
A31	VCC	VCC	VCC

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.