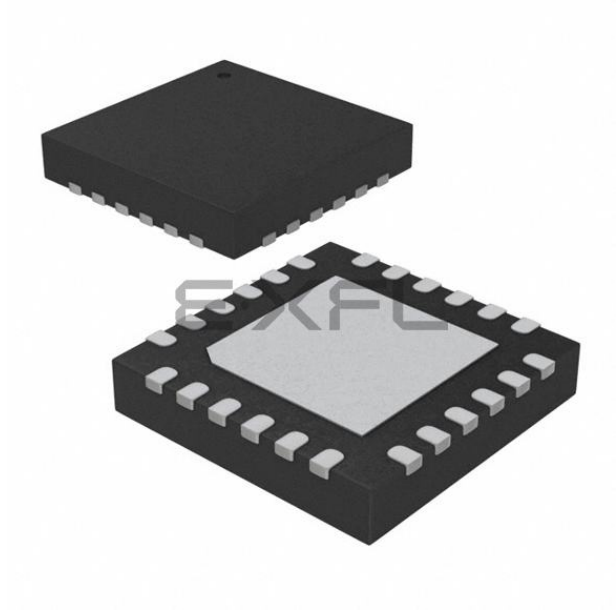

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-VQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny1607-mfr

6.10.1 Signature Row Summary (SIGROW)

Offset	Name	Bit Pos.									
0x00	DEVICEID0	7:0	DEVICEID[7:0]								
0x01	DEVICEID1	7:0	DEVICEID[7:0]								
0x02	DEVICEID2	7:0	DEVICEID[7:0]								
0x03	SERNUM0	7:0	SERNUM[7:0]								
0x04	SERNUM1	7:0	SERNUM[7:0]								
0x05	SERNUM2	7:0	SERNUM[7:0]								
0x06	SERNUM3	7:0	SERNUM[7:0]								
0x07	SERNUM4	7:0	SERNUM[7:0]								
0x08	SERNUM5	7:0	SERNUM[7:0]								
0x09	SERNUM6	7:0	SERNUM[7:0]								
0x0A	SERNUM7	7:0	SERNUM[7:0]								
0x0B	SERNUM8	7:0	SERNUM[7:0]								
0x0C	SERNUM9	7:0	SERNUM[7:0]								
0x0D ... 0x1F	Reserved										
0x20	TEMPSENSE0	7:0	TEMPSENSE[7:0]								
0x21	TEMPSENSE1	7:0	TEMPSENSE[7:0]								
0x22	OSC16ERR3V	7:0	OSC16ERR3V[7:0]								
0x23	OSC16ERR5V	7:0	OSC16ERR5V[7:0]								
0x24	OSC20ERR3V	7:0	OSC20ERR3V[7:0]								
0x25	OSC20ERR5V	7:0	OSC20ERR5V[7:0]								

6.10.2 Signature Row Description

12.5.1 Reset Flag Register

Name: RSTFR
Offset: 0x00
Reset: 0xXX
Property: -

All flags are cleared by writing a '1' to them. They are also cleared by a Power-on Reset, with the exception of the Power-On Reset Flag (PORF).

Bit	7	6	5	4	3	2	1	0
			UPDIRF	SWRF	WDRF	EXTRF	BORF	PORF
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	x	x	x	x	x	x

Bit 5 – UPDIRF UPDI Reset Flag
This bit is set if a UPDI Reset occurs.

Bit 4 – SWRF Software Reset Flag
This bit is set if a Software Reset occurs.

Bit 3 – WDRF Watchdog Reset Flag
This bit is set if a Watchdog Reset occurs.

Bit 2 – EXTRF External Reset Flag
This bit is set if an External Reset occurs.

Bit 1 – BORF Brown-Out Reset Flag
This bit is set if a Brown-out Reset occurs.

Bit 0 – PORF Power-On Reset Flag
This bit is set if a Power-on Reset occurs.

This flag is only cleared by writing a '1' to it.

After a POR, only the POR flag is set and all other flags are cleared. No other flags can be set before a full system boot is run after the POR.

13.5.3 Interrupt Priority Level 0

Name: LVL0PRI
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	LVL0PRI[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – LVL0PRI[7:0] Interrupt Priority Level 0
When Round Robin is enabled (LVL0RR bit in CPUINT.CTRLA is '1'), this bit field stores the vector of the last acknowledged priority level 0 (LVL0) interrupt. The stored vector will have the lowest priority next time one or more LVL0 interrupts are pending.

If Round Robin is disabled (LVL0RR in CPUINT.CTRLA is '0'), the vector address-based priority scheme (lowest address has the highest priority) is governing the priorities of LVL0 interrupt requests.

If a system Reset is asserted, the lowest interrupt vector address will have the highest priority within the LVL0.

16.4 Register Summary - PORT

Offset	Name	Bit Pos.								
0x00	DIR	7:0	DIR[7:0]							
0x01	DIRSET	7:0	DIRSET[7:0]							
0x02	DIRCLR	7:0	DIRCLR[7:0]							
0x03	DIRTGL	7:0	DIRTGL[7:0]							
0x04	OUT	7:0	OUT[7:0]							
0x05	OUTSET	7:0	OUTSET[7:0]							
0x06	OUTCLR	7:0	OUTCLR[7:0]							
0x07	OUTTGL	7:0	OUTTGL[7:0]							
0x08	IN	7:0	IN[7:0]							
0x09	INTFLAGS	7:0	INT[7:0]							
0x0A ... 0x0F	Reserved									
0x10	PIN0CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x11	PIN1CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x12	PIN2CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x13	PIN3CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x14	PIN4CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x15	PIN5CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x16	PIN6CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		
0x17	PIN7CTRL	7:0	INVEN				PULLUPEN	ISC[2:0]		

16.5 Register Description - Ports

16.5.10 Interrupt Flags

Name: INTFLAGS
Offset: 0x09
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	INT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – INT[7:0] Interrupt Pin Flag
The INT Flag is set when a pin change/state matches the pin's input sense configuration. Writing a '1' to a flag's bit location will clear the flag.

For enabling and executing the interrupt, refer to ISC bit description in PORT.PINnCTRL.

17.4 Register Summary - BOD

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0				SAMPFREQ	ACTIVE[1:0]		SLEEP[1:0]	
0x01	CTRLB	7:0						LVL[2:0]		
0x02 ... 0x07	Reserved									
0x08	VLMCTRLA	7:0							VLMLVL[1:0]	
0x09	INTCTRL	7:0						VLMCFG[1:0]		VLMIE
0x0A	INTFLAGS	7:0								VLMIF
0x0B	STATUS	7:0								VLMS

17.5 Register Description

20.5.18 Compare n Buffer Register

Name: CMPnBUF
Offset: 0x38 + n*0x02 [n=0..2]
Reset: 0x00
Property: -

This register serves as the buffer for the associated compare registers (TCAn.CMPn). Accessing any of these registers using the CPU or UPDI will affect the corresponding CMPnBV status bit.

The TCAn.CMPnBUFL and TCAn.CMPnBUFH register pair represents the 16-bit value, TCAn.CMPnBUF. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

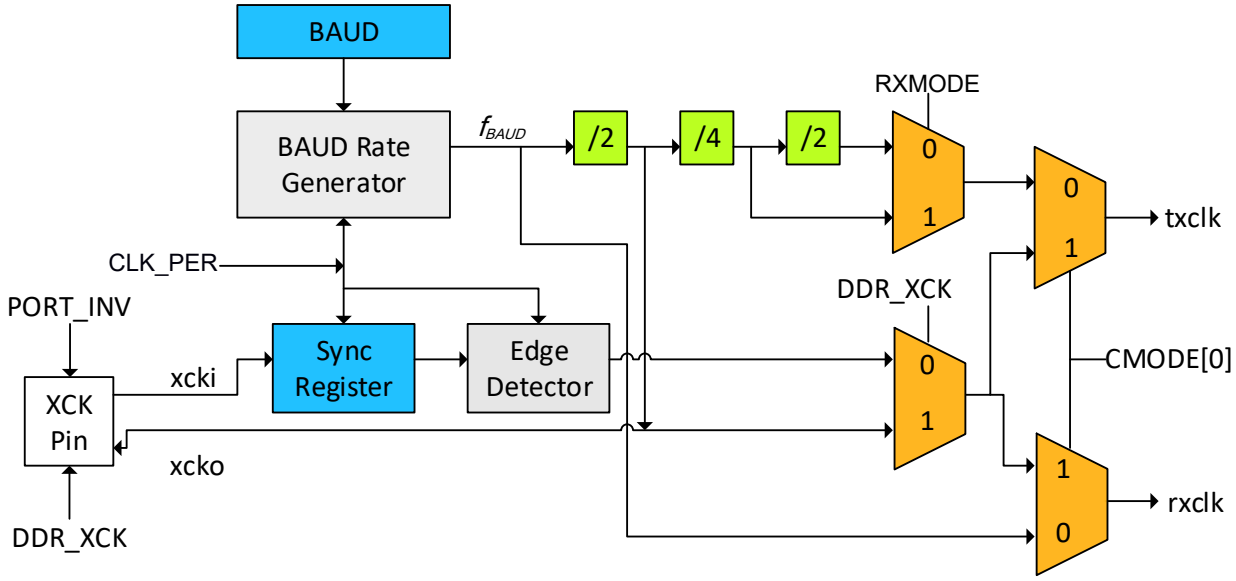
Bit	15	14	13	12	11	10	9	8
	CMPBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CMPBUF[15:8] Compare High Byte
These bits hold the MSB of the 16-bit compare buffer register.

Bits 7:0 – CMPBUF[7:0] Compare Low Byte
These bits hold the LSB of the 16-bit compare buffer register.

Figure 23-2. Clock Generation Logic Block Diagram



23.3.2.1.1 Internal Clock Generation - The Fractional Baud Rate Generator

The Baud Rate Generator is used for internal clock generation for Asynchronous modes, Synchronous master mode, and Master SPI mode operation. The output frequency generated (f_{BAUD}) is determined by the baud register value (BAUD) and the peripheral clock frequency (f_{CLK_PER}).

In Asynchronous mode, the BAUD register value uses all 16 bits. The 10 MSBs (BAUD[15:6]) hold the integer part, while the 6 LSBs (BAUD[5:0]) hold the fractional part. The fractional part is used to dynamically adjust the sampling timing for each individual bit in the frame and in that way compensate for the inaccuracy of the integer part of the BAUD register setting. BAUD register values below 64 are not supported, as the integer part need to be at least 1. The integer part valid range is therefore 64 to 65535.

In Synchronous mode, only the 10-bit integer part of the BAUD register, i.e. BAUD[15:6], determine the baud rate, and the fractional part must therefore be written to zero.

The following table lists equations for translating between BAUD register values and baud rates. The equations takes BAUD register bit width and fractional interpretation into consideration, and the BAUD register values calculated with these equations can be written directly to the BAUD register without any additional scaling. Resulting rounding errors will contribute to baud rate frequency errors.

Table 23-2. Equations for Calculating Baud Rate Register Setting

Operating Mode	Conditions	Baud Rate (f_{BAUD}, Bits Per Seconds)	USART.BAUD Register Value Calculation
Asynchronous	$f_{BAUD} \leq \frac{f_{CLK\_PER}}{S}$ $USART.BAUD \geq 64$	$\frac{f_{CLK\_PER}}{S \times BAUD} \times 2^6$	$round\left(\frac{f_{CLK\_PER}}{S \times f_{BAUD}} \times 2^6\right)$
Synchronous	$f_{BAUD} \leq \frac{f_{CLK\_PER}}{2}$	$\frac{f_{CLK\_PER}}{2 \times BAUD} \times 2^6$	$round\left(\frac{f_{CLK\_PER}}{2 \times f_{BAUD}}\right) \times 2^6$

S = 16 if in Receiver mode (USART.CTRLB, RXMODE) is configured as NORMAL, and S = 8 if configured as CLK2X. S determines the number of samples taken for each USART symbol.

23.5.6 Control A

Name: CTRLA
Offset: 0x05
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXCIE	TXCIE	DREIE	RXSIE	LBME	ABEIE	RS485[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – RXCIE Receive Complete Interrupt Enable
The bit enables the Receive Complete Interrupt (interrupt vector RXC). The enabled interrupt will be triggered when RXCIF in the USARTn.STATUS register is set.

Bit 6 – TXCIE Transmit Complete Interrupt Enable
This bit enables the Transmit Complete Interrupt (interrupt vector TXC). The enabled interrupt will be triggered when the TXCIF in the USARTn.STATUS register is set.

Bit 5 – DREIE Data Register Empty Interrupt Enable
This bit enables the Data Register Empty Interrupt (interrupt vector DRE). The enabled interrupt will be triggered when the DREIF in the USART.STATUS register is set.

Bit 4 – RXSIE Receiver Start Frame Interrupt Enable
Writing a '1' to this bit enables the Start Frame Detector to generate an interrupt on interrupt vector RXC when a start-of-frame condition is detected.

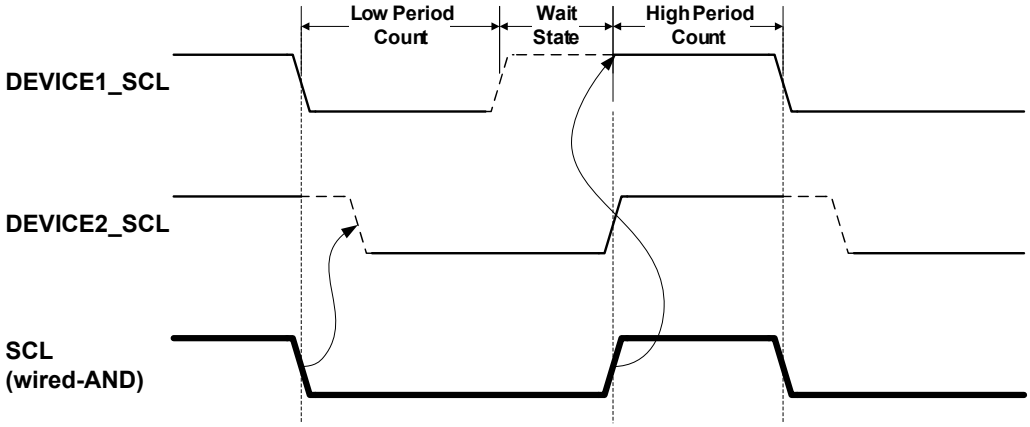
Bit 3 – LBME Loop-back Mode Enable
Writing this bit to '1' enables an internal connection between the TxD and RxD pin.

Bit 2 – ABEIE Auto-baud Error Interrupt Enable
Writing this bit to '1' enables the auto-baud error interrupt on interrupt vector RXC. The enabled interrupt will trigger for conditions where the ISFIF flag is set.

Bits 1:0 – RS485[1:0] RS-485 Mode
These bits enable the RS-485 and select the operation mode.

Value	Name	Description
0x0	OFF	Disabled.
0x1	EXT	Enables RS-485 mode with control of an external line driver through a dedicated Transmit Enable (TE) pin.
0x2	INT	Enables RS-485 mode with control of the internal USART transmitter.
0x3	-	Reserved.

Figure 25-11. Clock Synchronization



A high-to-low transition on the SCL line will force the line low for all masters on the bus, and they will start timing their low clock period. The timing length of the low clock period can vary among the masters. When a master (DEVICE1 in this case) has completed its low period, it releases the SCL line. However, the SCL line will not go high until all masters have released it. Consequently, the SCL line will be held low by the device with the longest low period (DEVICE2). Devices with shorter low periods must insert a wait state until the clock is released. All masters start their high period when the SCL line is released by all devices and has gone high. The device, which first completes its high period (DEVICE1), forces the clock line low, and the procedure is then repeated. The result is that the device with the shortest clock period determines the high period, while the low period of the clock is determined by the device with the longest clock period.

25.3.3 TWI Bus State Logic

The bus state logic continuously monitors the activity on the TWI bus lines when the master is enabled. It continues to operate in all Sleep modes, including power-down.

The bus state logic includes Start and Stop condition detectors, collision detection, inactive bus time-out detection, and a bit counter. These are used to determine the bus state. The software can get the current bus state by reading the Bus State bits in the master STATUS register. The bus state can be unknown, idle, busy, or owner, and is determined according to the state diagram shown in Figure 25-12. The values of the Bus State bits according to state, are shown in binary in the figure below.

When the interrupt condition occurs, the OK flag in the Status register (CRCSCAN.STATUS) is cleared to '0'.

An interrupt is enabled by writing a '1' to the respective Enable bit (NMIEN) in the Control A register (CRCSCAN.CTRLA), but can only be disabled with a system Reset. An NMI is generated when the OK flag in CRCSCAN.STATUS is cleared and the NMIEN bit is '1'. The NMI request remains active until a system Reset, and cannot be disabled.

A non-maskable interrupt can be triggered even if interrupts are not globally enabled.

Related Links

26.5.1 CTRLA
26.5.3 STATUS
13. CPUINT - CPU Interrupt Controller

26.3.4 Sleep Mode Operation

CTCSCAN is halted in all sleep modes. In all CPU Sleep modes, the CRCSCAN peripheral is halted and will resume operation when the CPU wakes up.

The CRCSCAN starts operation three cycles after writing the EN bit in CRCSCAN.CTRLA. During these three cycles, it is possible to enter Sleep mode. In this case:

1. The CRCSCAN will not start until the CPU is woken up.
2. Any interrupt handler will execute after CRCSCAN has finished.

26.3.5 Configuration Change Protection

Not applicable.

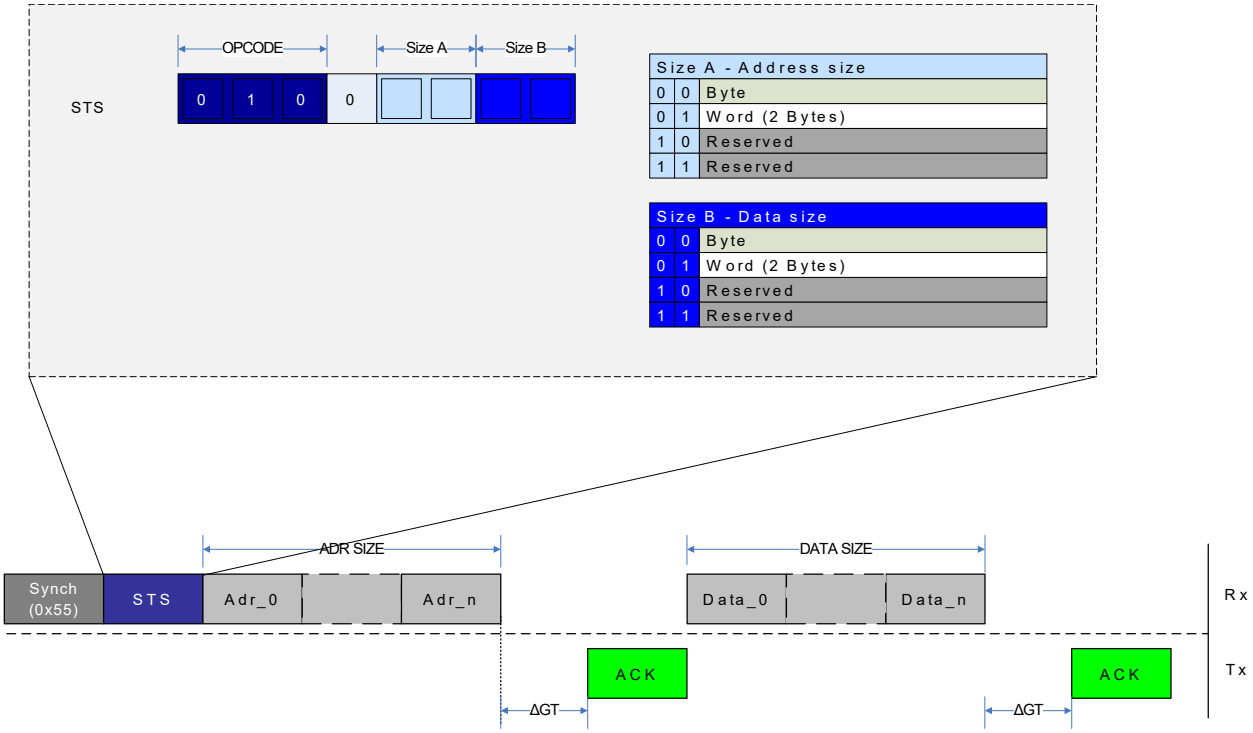
29.5.6 Sample Control

Name: SAMPCTRL
Offset: 0x5
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
				SAMPLEN[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – SAMPLEN[4:0] Sample Length
These bits extend the ADC sampling length in a number of CLK_ADC cycles. By default, the sampling time is two CLK_ADC cycles. Increasing the sampling length allows sampling sources with higher impedance. The total conversion time increases with the selected sampling length.

Figure 30-10. `STS` Instruction Operation



The transfer protocol for an `STS` instruction is depicted in the figure as well, following this sequence:

1. The address is sent.
2. An Acknowledge (ACK) is sent back from the UPDI if the transfer was successful.
3. The number of bytes as specified in the `STS` instruction is sent.
4. A new ACK is received after the data has been successfully transferred.

30.3.3.3 `LD` - Load Data from Data Space Using Indirect Addressing

The `LD` instruction is used to load data from the bus matrix and into the serial shift register for serial readout. The `LD` instruction is based on indirect addressing, which means that the Address Pointer in the UPDI needs to be written prior to bus matrix access. Automatic pointer post-increment operation is supported and is useful when the `LD` instruction is used with `REPEAT`. It is also possible to do an `LD` of the UPDI Pointer register. The maximum supported size for address and data load is 16 bits.

Table 30-6. KEY Activation Signatures

KEY Name	KEY Signature (LSB Written First)	Size
Chip Erase	0x4E564D4572617365	64 bits
NVMPROG	0x4E564D50726F6720	64 bits
USERROW-Write	0x4E564D5573267465	64 bits

30.3.7.1 Chip Erase

The following steps should be followed to issue a Chip Erase.

1. Enter the CHIPERASE KEY by using the `KEY` instruction. See Table 30-6 for the CHIPERASE signature.
2. **Optional:** Read the Chip Erase bit in the AS Key Status register (CHIPERASE in UPDI.ASI_KEY_STATUS) to see that the KEY is successfully activated.
3. Write the Reset signature into the UPDI.ASI_RESET_REQ register. This will issue a System Reset.
4. Write 0x00 to the ASI Reset Request register (UPDI.ASI_RESET_REQ) to clear the System Reset.
5. Read the Lock Status bit in the ASI System Status register (LOCKSTATUS in UPDI.ASI_SYS_STATUS).
6. Chip Erase is done when LOCKSTATUS == 0 in UPDI.ASI_SYS_STATUS. If LOCKSTATUS == 1, go to point 5 again.

After a successful Chip Erase, the Lockbits will be cleared, and the UPDI will have full access to the system. Until Lockbits are cleared, the UPDI cannot access the system bus, and only CS-space operations can be performed.

⚠ CAUTION During Chip Erase, the BOD is forced ON (ACTIVE=0x1 in BOD.CTRLA) and uses the BOD Level from the BOD Configuration fuse (LVL in BOD.CTRLB = LVL in FUSE.BODCFG). If the supply voltage V_{DD} is below that threshold level, the device is unserviceable until V_{DD} is increased adequately.

30.3.7.2 NVM Programming

If the device is unlocked, it is possible to write directly to the NVM Controller using the UPDI. This will lead to unpredictable code execution if the CPU is active during the NVM programming. To avoid this, the following NVM Programming sequence should be executed.

1. Follow the Chip erase procedure as described in Chip Erase. If the part is already unlocked, this point can be skipped.
2. Enter the NVMPROG KEY by using the `KEY` instruction. See Table 30-6 for the NVMPROG signature.
3. **Optional:** Read the NVMPROG field in the KEY_STATUS register to see that the KEY has been activated.
4. Write the Reset signature into the ASI_RESET_REQ register. This will issue a System Reset.
5. Write 0x00 to the Reset signature in the ASI_RESET_REQ register to clear the System Reset.
6. Read NVMPROG in ASI_SYS_STATUS.
7. NVM Programming can start when NVMPROG == 1 in the ASI_SYS_STATUS register. If NVMPROG == 0, go to point 6 again.

⚠ CAUTION

V_{RST}MAX = 13V

Care should be taken to avoid overshoot (overvoltage) when connecting the RESET pin to a 12V source. Exposing the pin to a voltage above the rated absolute maximum can activate the pin's ESD protection circuitry, which will remain activated until the voltage has been brought below approximately 10V. A 12V driver can keep the ESD protection in an activated state (if activated by an overvoltage condition) while driving currents through it, potentially causing permanent damage to the part.

31.3 General Operating Ratings

The device must operate within the ratings listed in this section in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 31-2. General Operating Conditions

Symbol	Description	Condition	Min.	Max.	Unit
V_{DD}	Operating Supply Voltage		1.8(2)	5.5	V
T	Operating temperature range(1)	Standard temperature range	-40	105	°C
		Extended temperature range(3)	-40	125	

Note:

1. Refer to the device ordering codes for the device temperature range.
2. Operation ensured down to 1.8V or V_{BOD} with BODLEVEL0, whichever is lower.
3. Extended temperature range is only ensured down to 2.7V.

Table 31-3. Operating Voltage and Frequency

Symbol	Description	Condition	Min.	Max.	Unit
CLK_CPU	Operating system clock frequency	V_{DD}=[1.8, 5.5]V T=[-40, 105]°C(1)	0	5	MHz
		V_{DD}=[2.7, 5.5]V T=[-40, 105]°C(2)	0	10	
		V_{DD}=[4.5, 5.5]V T=[-40, 105]°C(3)	0	20	
		V_{DD}=[2.7, 5.5]V T=[-40, 125]°C(2)	0	8	
		V_{DD}=[4.5, 5.5]V T=[-40, 125]°C(3)	0	16	

Note:

1. Operation ensured down to BOD triggering level, V_{BOD} with BODLEVEL0.

31.12 SPI

Figure 31-4. SPI - Timing Requirements in Master Mode

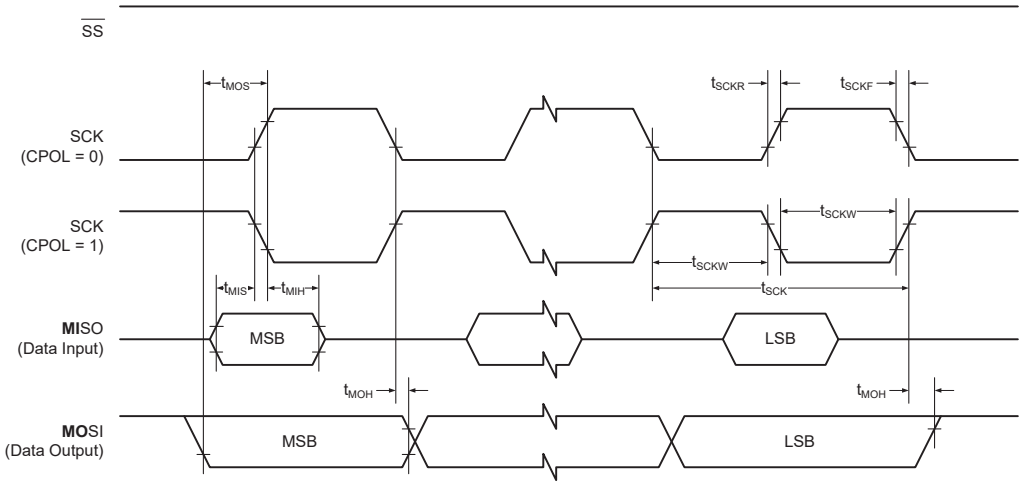


Figure 31-5. SPI - Timing Requirements in Slave Mode

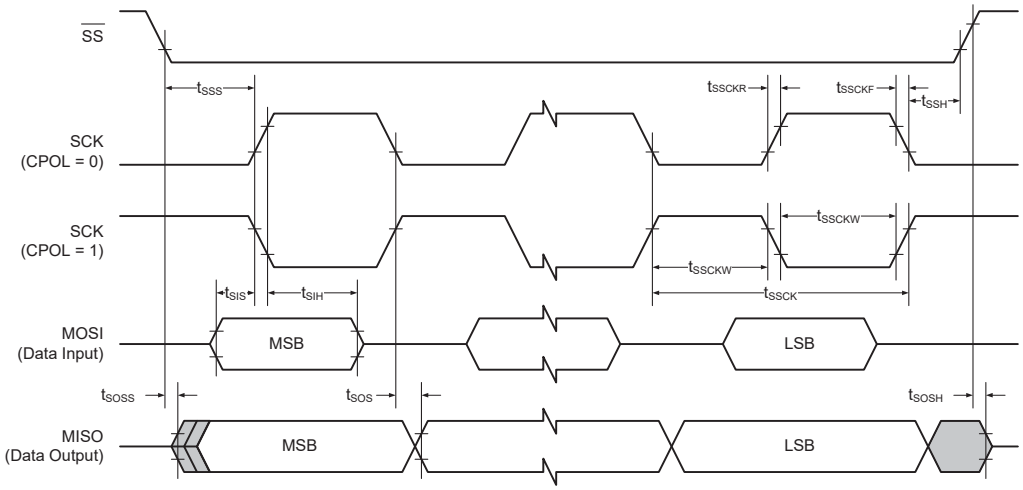


Table 31-17. SPI - Timing Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Master	-	-	10	MHz
t_{SCK}	SCK period	Master	100	-	-	ns
t_{SCKW}	SCK high/low width	Master	-	0.5*SCK	-	ns
t_{SCKR}	SCK rise time	Master	-	2.7	-	ns
t_{SCKF}	SCK fall time	Master	-	2.7	-	ns
t_{MIS}	MISO setup to SCK	Master	-	10	-	ns
t_{MIH}	MISO hold after SCK	Master	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Master	-	0.5*SCK	-	ns
t_{MOH}	MOSI hold after SCK	Master	-	1.0	-	ns

32.2 GPIO

GPIO Input Characteristics

Figure 32-15. I/O Pin Input Hysteresis vs. V_{DD}

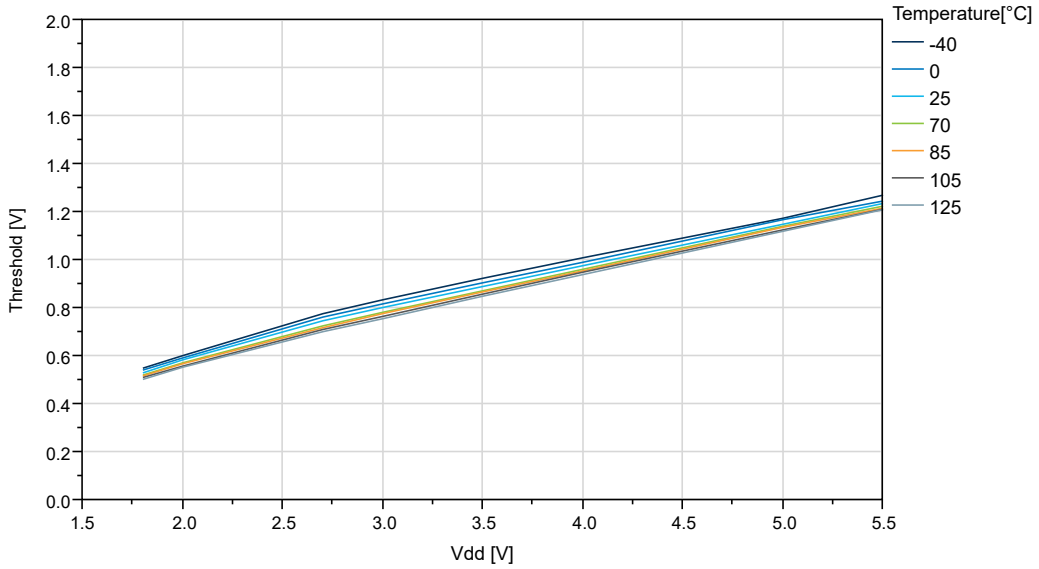


Figure 32-16. I/O Pin Input Threshold Voltage vs. V_{DD} (T=25°C)

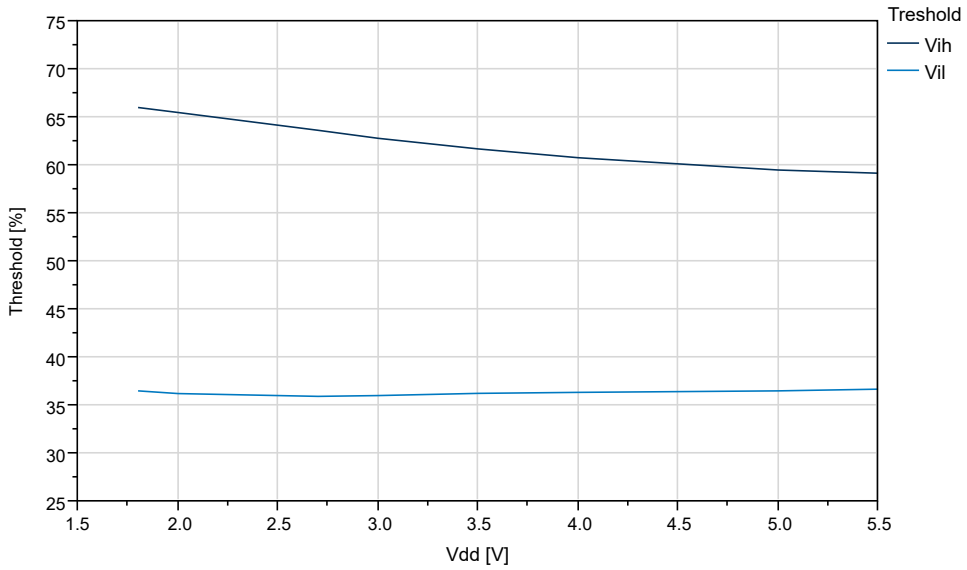


Figure 32-45. Gain Error vs. V_{ref} (V_{DD}=5.0V, f_{ADC}=115 ksps), REFSEL = Internal Reference

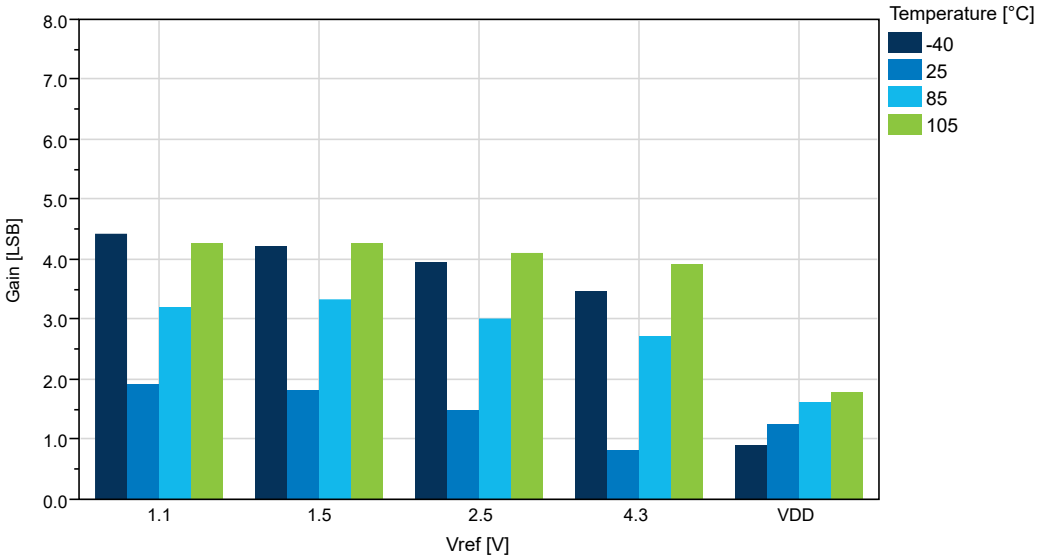
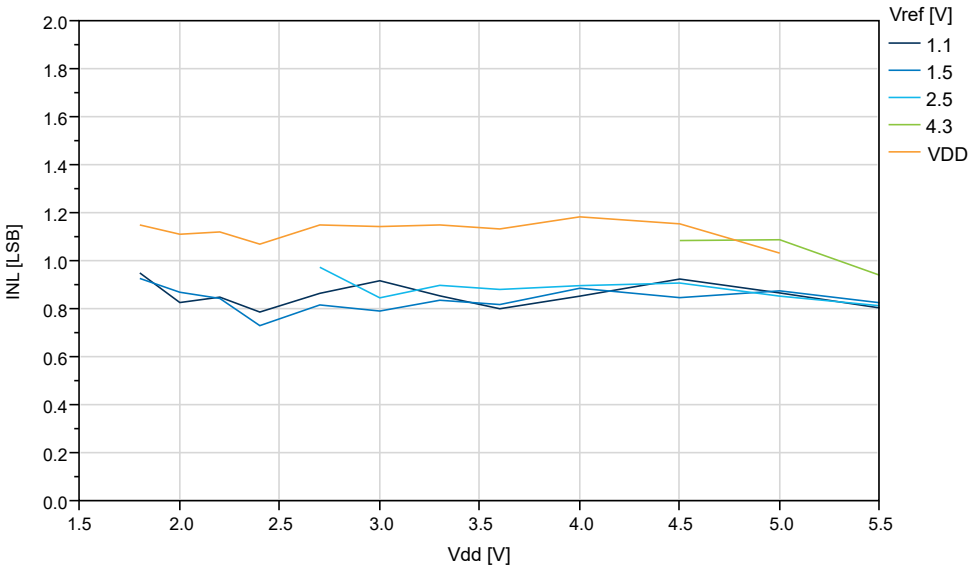


Figure 32-46. INL vs. V_{DD} (f_{ADC}=115 ksps) at T=25°C, REFSEL = Internal Reference

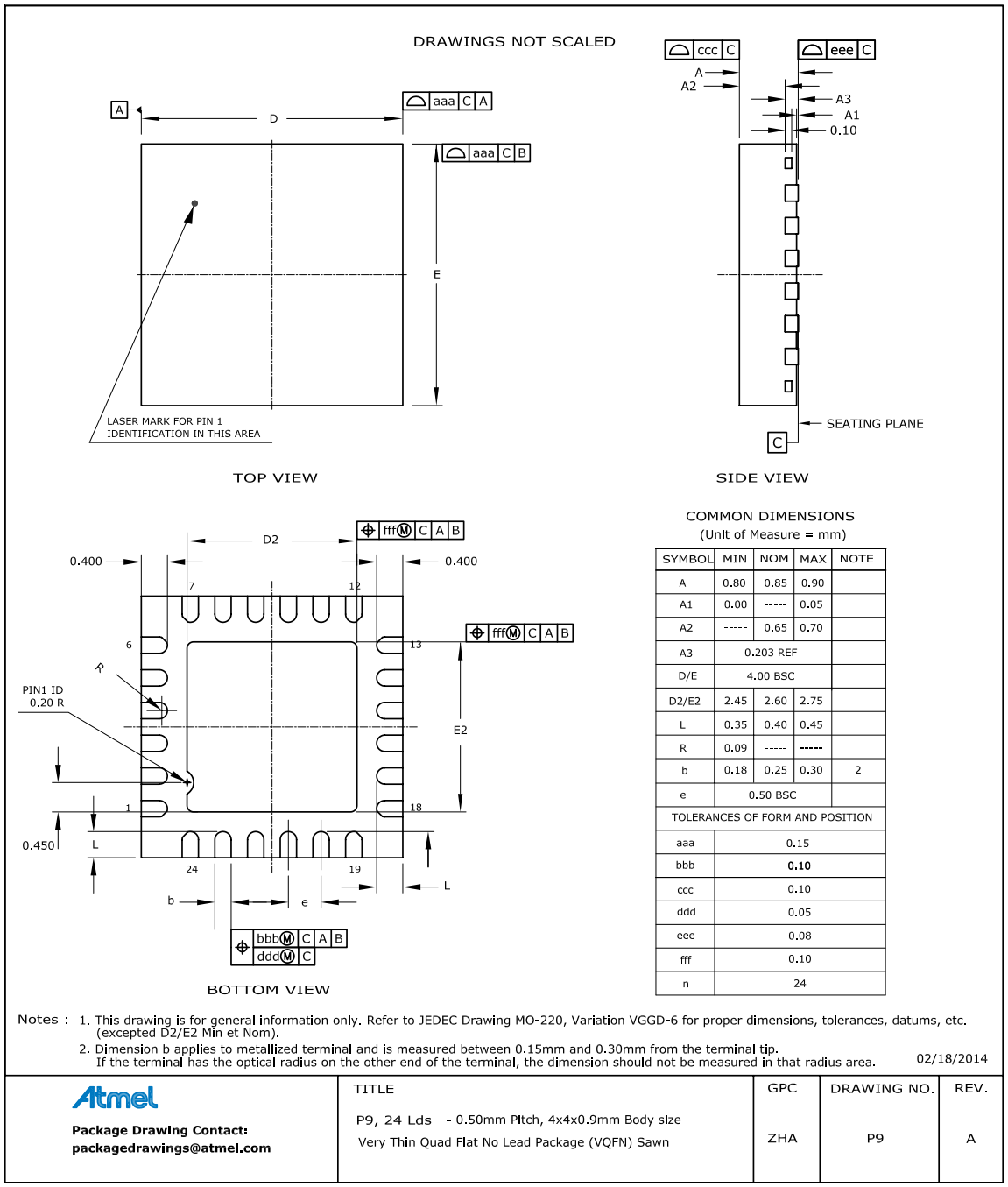


34. Package Drawings

34.1 24-Pin VQFN

Note:

Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	-----	0.05	
A2	-----	0.65	0.70	
A3		0.203 REF		
D/E		4.00 BSC		
D2/E2	2.45	2.60	2.75	
L	0.35	0.40	0.45	
R	0.09	-----	-----	
b	0.18	0.25	0.30	2
e		0.50 BSC		
TOLERANCES OF FORM AND POSITION				
aaa	0.15			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
fff	0.10			
n	24			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VGGD-6 for proper dimensions, tolerances, datums, etc. (excepted D2/E2 Min et Nom).
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

02/18/2014

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE P9, 24 Lds - 0.50mm Pitch, 4x4x0.9mm Body size Very Thin Quad Flat No Lead Package (VQFN) Sawn	GPC ZHA	DRAWING NO. P9	REV. A

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