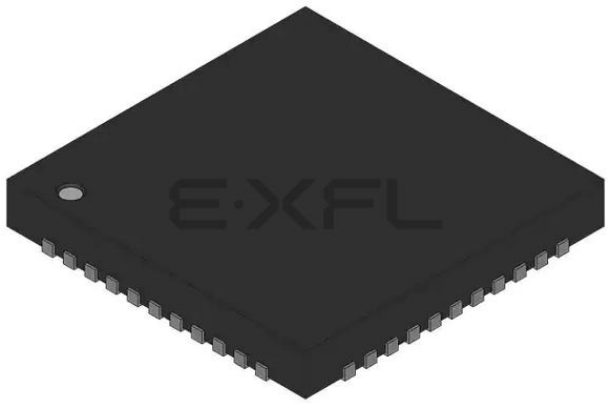

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFLGA Exposed Pad
Supplier Device Package	44-MAPLGA (5x5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ju128vhs

Field	Description	Values
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB
T	Temperature range, ambient (°C)	V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • HS = 44 Laminate QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)

1. All parts also have FlexNVM, FlexRAM, and RAM.

2.4 Example

This is an example part number:

MCF51JU128VLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Symbol	Description	Value	Unit
V_{DD}	3.3 V supply voltage	3.3	V

5.2 Nonswitching electrical specifications

5.2.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	0.7 × V_{DD}	—	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	0.75 × V_{DD}	—	V	
V_{IL}	Input low voltage				2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.35 × V_{DD}	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	
I_{IC}	DC injection current — single pin				3
	• V_{IN} > V_{DD}	0	2	mA	
	• V_{IN} < V_{SS}	0	–0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				3
	• V_{IN} > V_{DD}	0	25	mA	
	• V_{IN} < V_{SS}	0	–5	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. The device always interprets an input as a 1 when the input is greater than or equal to V_{IH} (min.) and less than or equal to V_{IH} (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to V_{IL} (max.) and greater than or equal to V_{IL} (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (VIn > VDD) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from RAM, exercising flash memory					3
	• @ 1.8 V	—	20	23.5	mA	
	• @ 3.0 V	—	20	25	mA	
I_{DD_WAIT}	Wait mode current at 3.0 V — all peripheral clocks disabled	—	5.8	6.8	mA	4
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25 °C	—	0.34	0.41	mA	
	• @ 105 °C	—	0.90	1.8	mA	
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.63	1.32	mA	5
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.78	1.46	mA	6
I_{DD_VLPW}	Very low-power wait mode current at 3.0 V	—	0.15	0.62	mA	7
I_{DD_VLPS}	Very low-power stop mode current at 3.0 V				µA	8
	• @ –40 to 25 °C	—	19	45		
	• @ 105 °C	—	145	312		
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					8,9,10
	• @ –40 to 25 °C	—	3.0	4.8	µA	
	• @ 105 °C	—	53.3	157	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					8,9,10
	• @ –40 to 25 °C	—	1.8	3.3	µA	
	• @ 105 °C	—	39.2	115	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					8,9
	• @ –40 to 25 °C	—	1.6	2.8	µA	
	• @ 105 °C	—	22.2	65	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					8,9
	• @ –40 to 25 °C	—	1.4	2.6	µA	
	• @ 105 °C	—	17.6	50	µA	
I_{DD_RTC}	Average current adder for real-time clock function					11
	• @ –40 to 25 °C	—	0.7	—	µA	

1. The analog supply current is the sum of the active current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode.

5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and I^2C signals. The conditions are 50 pf load, V_{DD} = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 9. EGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
	External reset pulse width (digital glitch filter disabled)	100	—	ns
	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

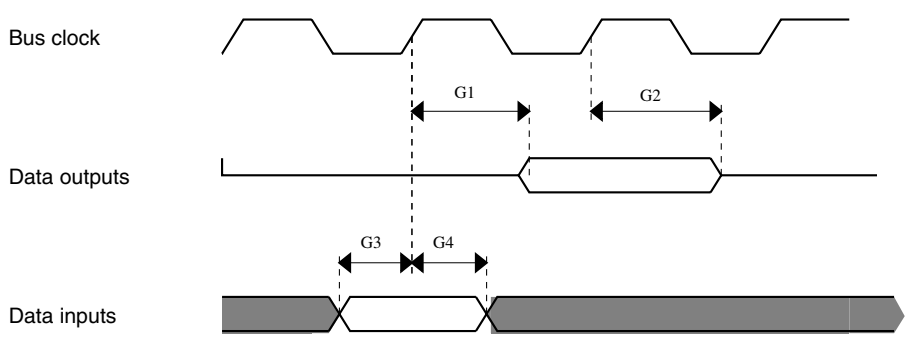


Figure 3. EGPIO timing diagram

Table 13. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	1350 600	— —	ps ps	8

Table continues on the next page...

Table 17. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 B flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	275	2350	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	

Table continues on the next page...

Table 20. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	15	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	0.0	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	15	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	0.0	—	ns
EP7	EZP_CK low to EZP_Q output valid (setup)	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0.0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

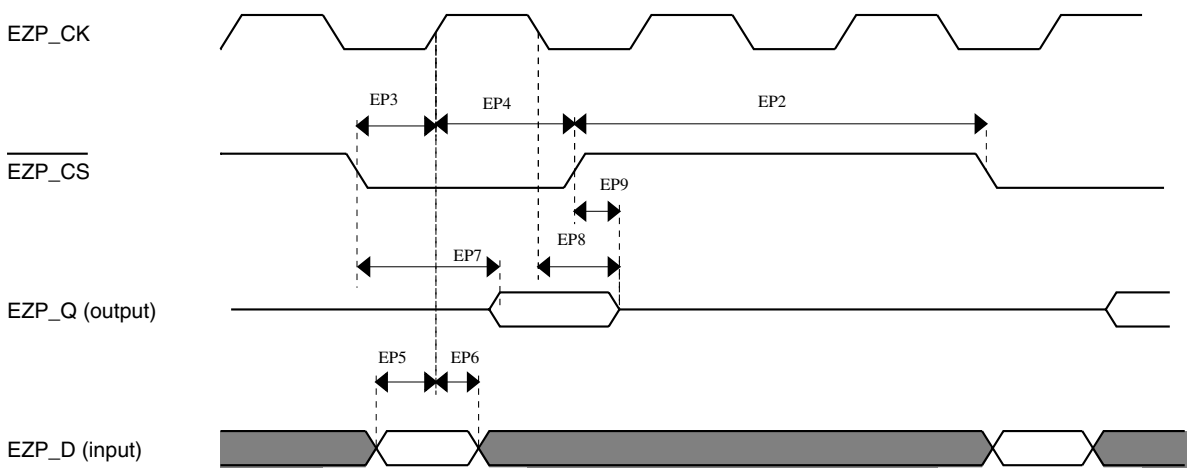


Figure 6. EzPort Timing Diagram

6.4.3 Mini-Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

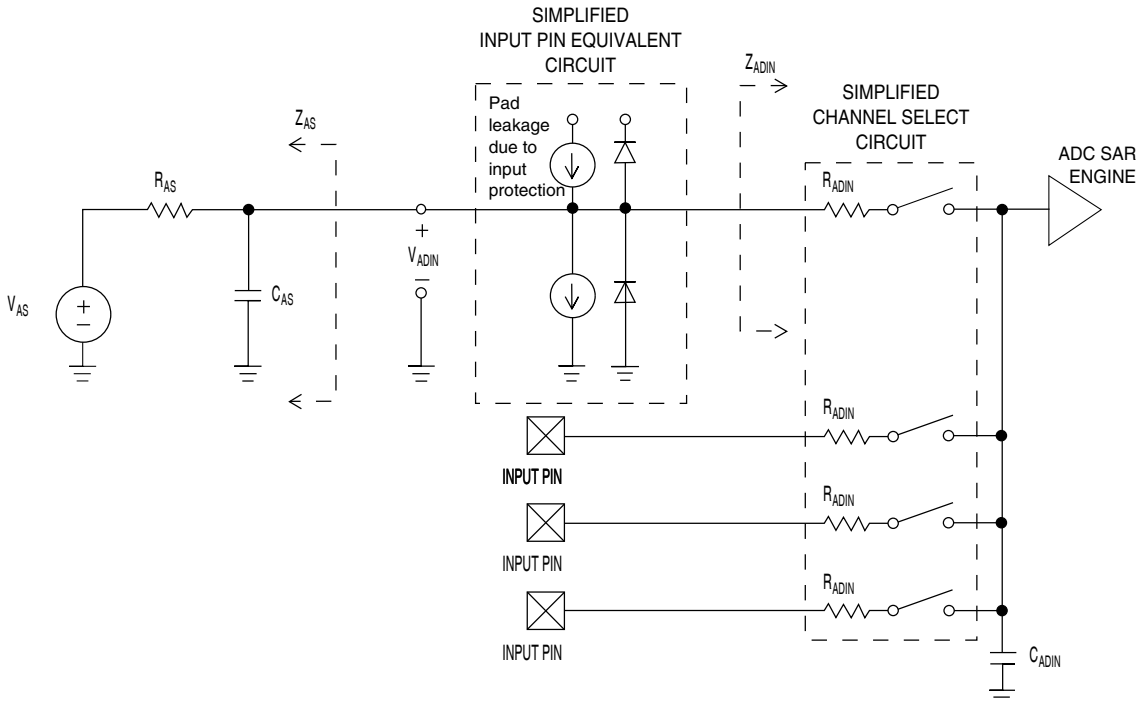


Figure 9. ADC input impedance equivalency diagram

6.6.1.2 12-bit ADC electrical characteristics

Table 23. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5

Table continues on the next page...

5. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}–100 mV
6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

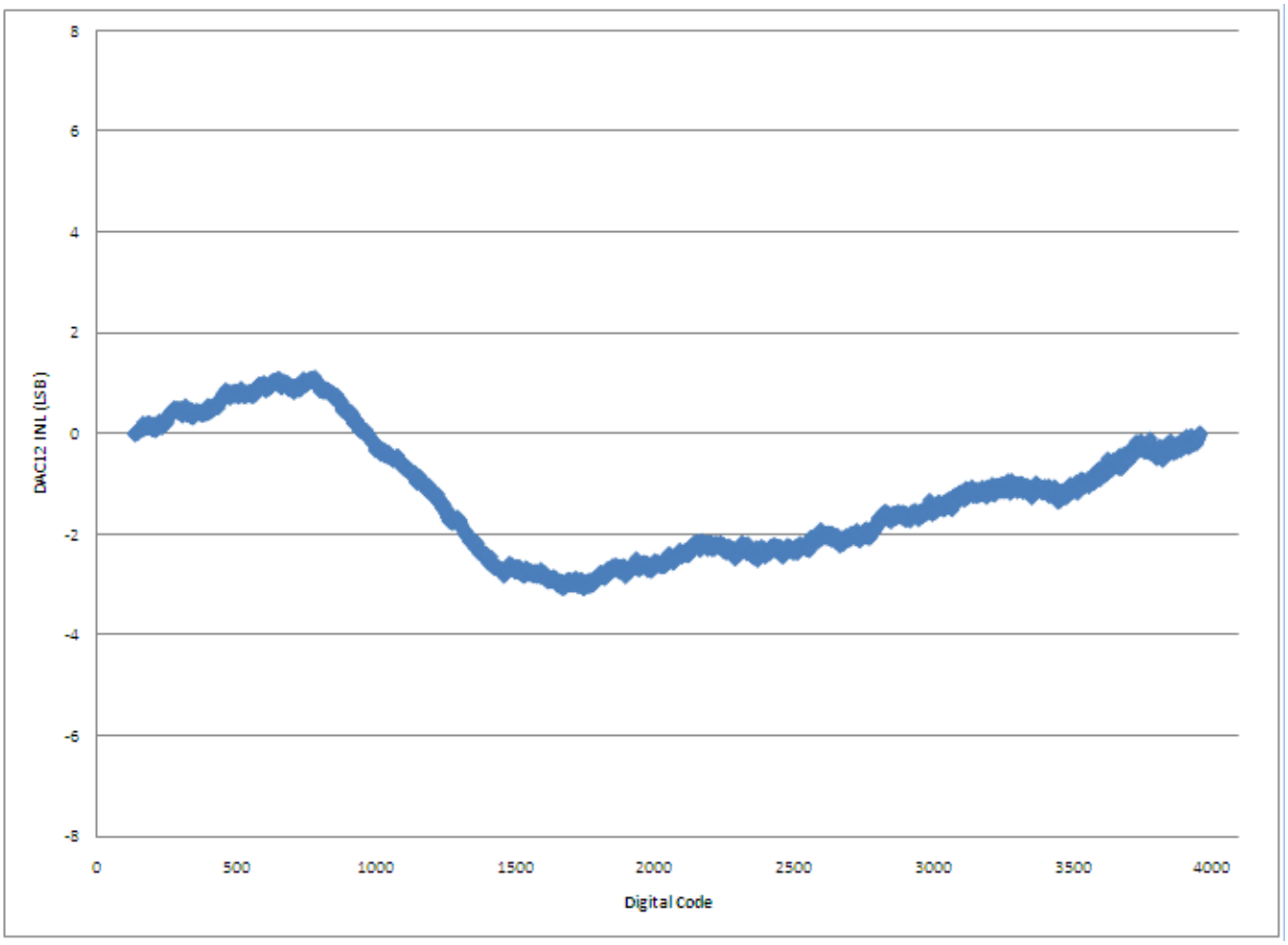
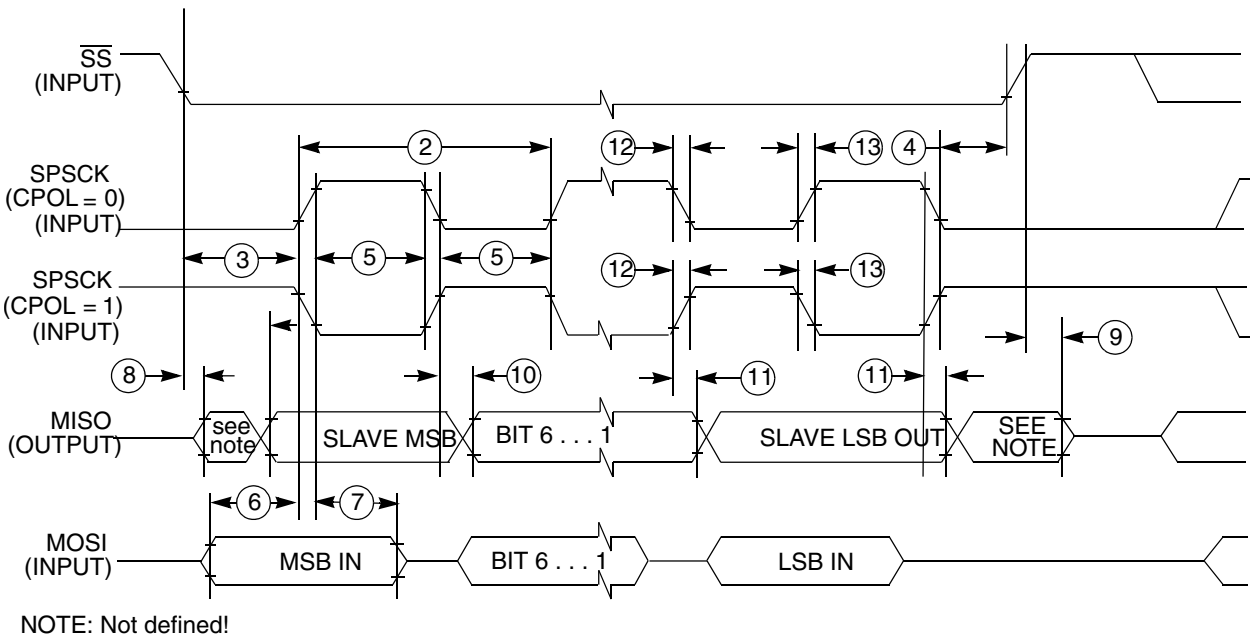


Figure 12. Typical INL error vs. digital code

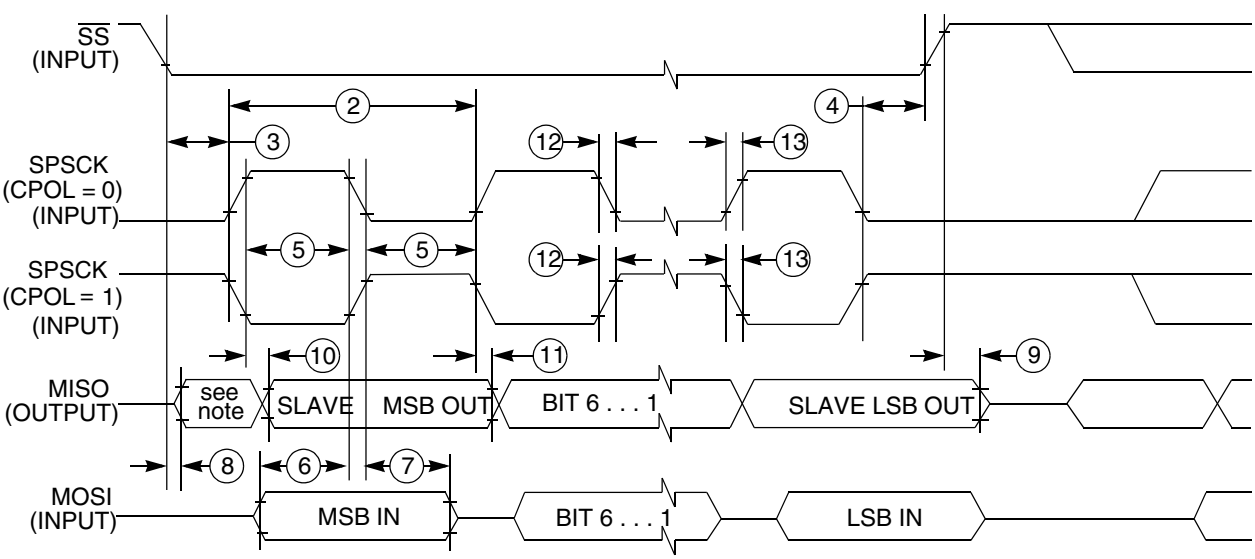
Table 34. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 16. SPI slave mode timing (CPHA=0)



NOTE: Not defined!

Figure 17. SPI slave mode timing (CPHA=1)

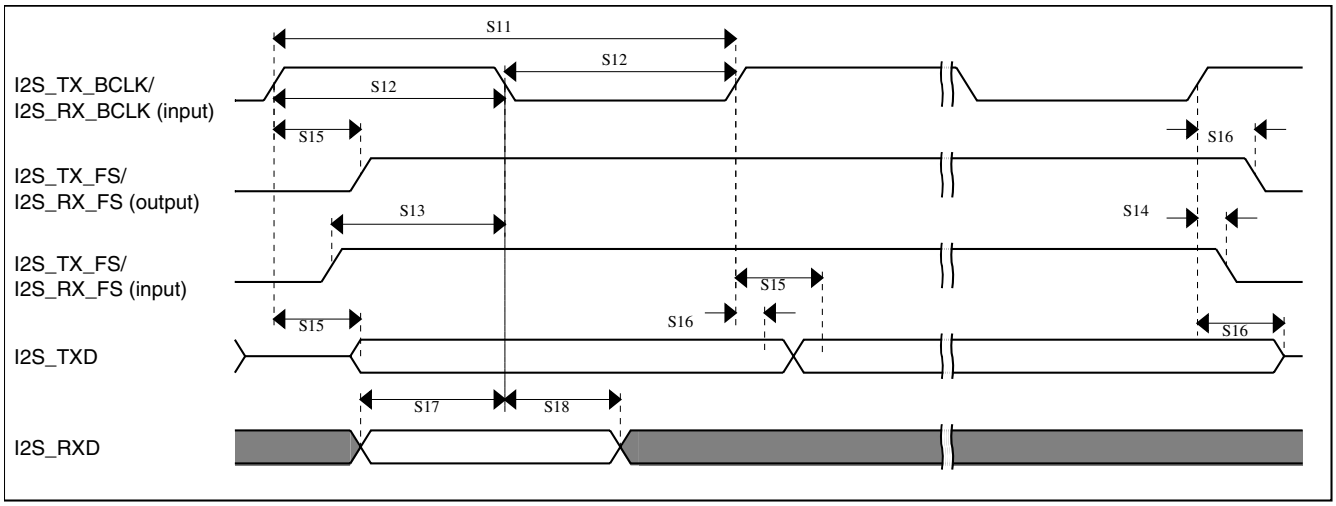


Figure 19. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 37. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	5.5	14	MHz	2
f_{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C_{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V_{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I_{REF}	Reference oscillator current source base current • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 5
I_{ELE}	Electrode oscillator current source base current • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	%	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	%	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	%	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	11

Table continues on the next page...

Table 37. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{TSI_RUN}	Current added in run mode	—	55	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	µA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
7. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
10. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: Iext = 5 µA, EXTCHRG = 4, PS = 128, NSCN = 2, $I_{ref} = 16$ µA, REFCHRG = 15, C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: $I_{ext} = 1$ µA, EXTCHRG = 0, PS = 128, NSCN = 32, $I_{ref} = 32$ µA, REFCHRG = 31, C_{ref}= 0.5 pF
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ARE10566D
44-pin Laminate QFN	98ASA00239D
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Mux Control module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	—	—	—	VDD	VDD								
2	—	—	—	VSS	VSS								
3	—	—	—	Disabled	Disabled	PTC6	UART0_TX	I2C0_SCL	RGPIO6	SPI1_MOSI	FBa_AD11		
4	—	—	—	Disabled	Disabled	PTC7	UART0_RX	I2C0_SDA	RGPIO7	SPI1_MISO	FBa_AD12		
5	1	—	—	Disabled	Disabled	PTD0	UART0_CTS_b	I2C1_SDA	RGPIO8	SPI1_SCLK	FBa_AD13	I2S0_MCLK / I2S0_CLKIN	
6	2	—	—	Disabled	Disabled	PTD1	UART0_RTS_b	I2C1_SCL	RGPIO9	SPI1_SS	FBa_AD14	I2S0_RX_BCLK	
7	3	1	1	Disabled	Disabled	PTA0		I2C2_SCL	FTM1_CH0	SPI0_SS	FBa_AD15	I2S0_RX_FS	
8	4	2	2	Disabled	Disabled	PTA1		I2C2_SDA	FTM1_CH1		FBa_AD16	I2S0_RXD	
9	5	3	3	Disabled	Disabled	PTA2	UART1_TX		FTM1_CH2	SPI1_SS			
10	6	4	4	Disabled	Disabled	PTA3	UART1_RX		FTM1_CH3	SPI1_SCLK		I2S0_TX_BCLK	EZP_CLK
11	7	5	5	ADC0_SE2	ADC0_SE2	PTA4	UART1_CTS_b	I2C2_SCL	FTM1_CH4	SPI1_MISO		I2S0_TX_FS	EZP_DI
12	8	6	6	ADC0_SE3	ADC0_SE3	PTA5	UART1_RTS_b	I2C2_SDA	FTM1_CH5	SPI1_MOSI	CLKOUT	I2S0_TXD	EZP_DO
13	9	7	7	VDDA	VDDA								
14	10	8	—	VREFH	VREFH								
15	11	9	—	VREF_OUT	VREF_OUT								
16	12	10	—	VREFL	VREFL								
17	13	11	8	VSSA	VSSA								
18	14	12	9	DAC0_OUT	DAC0_OUT								
19	15	13	10	VREGIN	VREGIN								
20	16	14	11	VOUT33	VOUT33								
21	17	15	12	USB0_DM	USB0_DM								

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
47	34	30	23	EXTAL2	EXTAL2	PTB6							
48	35	31	24	VDD	VDD								
49	36	32	25	VSS	VSS								
50	37	33	26	EXTAL1	EXTAL1	PTB7		I2C1_SDA	TMR_CLKIN1				
51	38	34	27	XTAL1	XTAL1	PTC0		I2C1_SCL	TMR_CLKIN0	RGPIO0			
52	39	35	28	RESET_b	Disabled	PTC1	RESET_b						
53	—	—	—	CMP0_IN0	CMP0_IN0	PTF0	SPI0_SS				FBa_AD5		
54	—	—	—	Disabled	Disabled	PTF1	SPI0_SCLK			CMP0_OUT	FBa_AD6		
55	—	—	—	CMP0_IN1	CMP0_IN1	PTF2	SPI0_MISO				FBa_AD7		
56	40	36	—	CMP0_IN2	CMP0_IN2	PTF3	SPI0_MOSI			RGPIO1	FBa_AD8	I2S0_TXD	
57	41	37	29	CMP0_IN3	CMP0_IN3	PTC2	UART1_RTS_b	SPI1_SS		RGPIO2	FBa_AD18	I2S0_TX_FS	
58	42	38	—	Disabled	Disabled	PTF4	UART1_CTS_b	SPI1_SCLK		FBa_D3	FBa_AD19	I2S0_TX_BCLK	
59	43	39	—	Disabled	Disabled	PTF5	UART1_RX	SPI1_MISO		FBa_D2	FBa_RW_b	I2S0_RXD	
60	44	40	—	Disabled	Disabled	PTF6	UART1_TX	SPI1_MOSI		FBa_D1	FBa_AD9	I2S0_RX_FS	
61	45	41	—	Disabled	Disabled	PTF7	UART0_RTS_b		SPI0_SS	FBa_D0	FBa_AD10	I2S0_RX_BCLK	
62	46	42	30	Disabled	Disabled	PTC3	UART0_CTS_b	RGPIO3	SPI0_SCLK	CLKOUT	USB_CLKIN	I2S0_MCLK / I2S0_CLKIN	
63	47	43	31	Disabled	Disabled	PTC4	UART0_RX	RGPIO4	SPI0_MISO	PDB0_EXTRG	USB_SOF_PULSE		
64	48	44	32	Disabled	Disabled	PTC5	UART0_TX	RGPIO5	SPI0_MOSI	CMT_IRO			

8.2 Pinout diagrams

The following diagrams show pinouts for the 64-pin, 48-pin, 44-pin, and 32-pin packages. These diagrams are representations for ease of reference. See the package drawings for mechanical details.

For each pin, the diagrams show the default function or (when disabled is the default) the ALT1 signal for a GPIO function. However, many signals may be multiplexed onto a single pin.

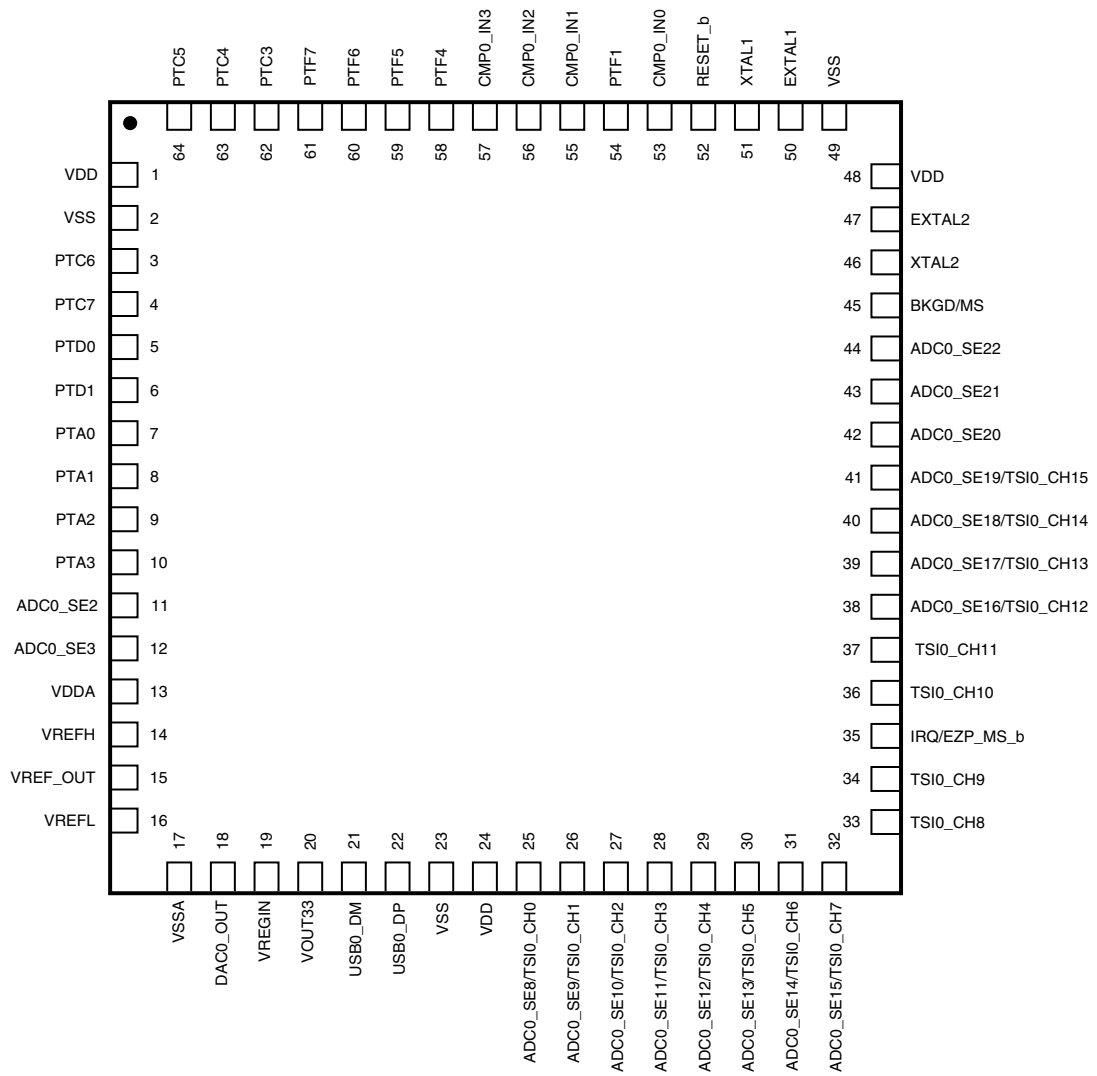


Figure 20. 64-pin LQFP

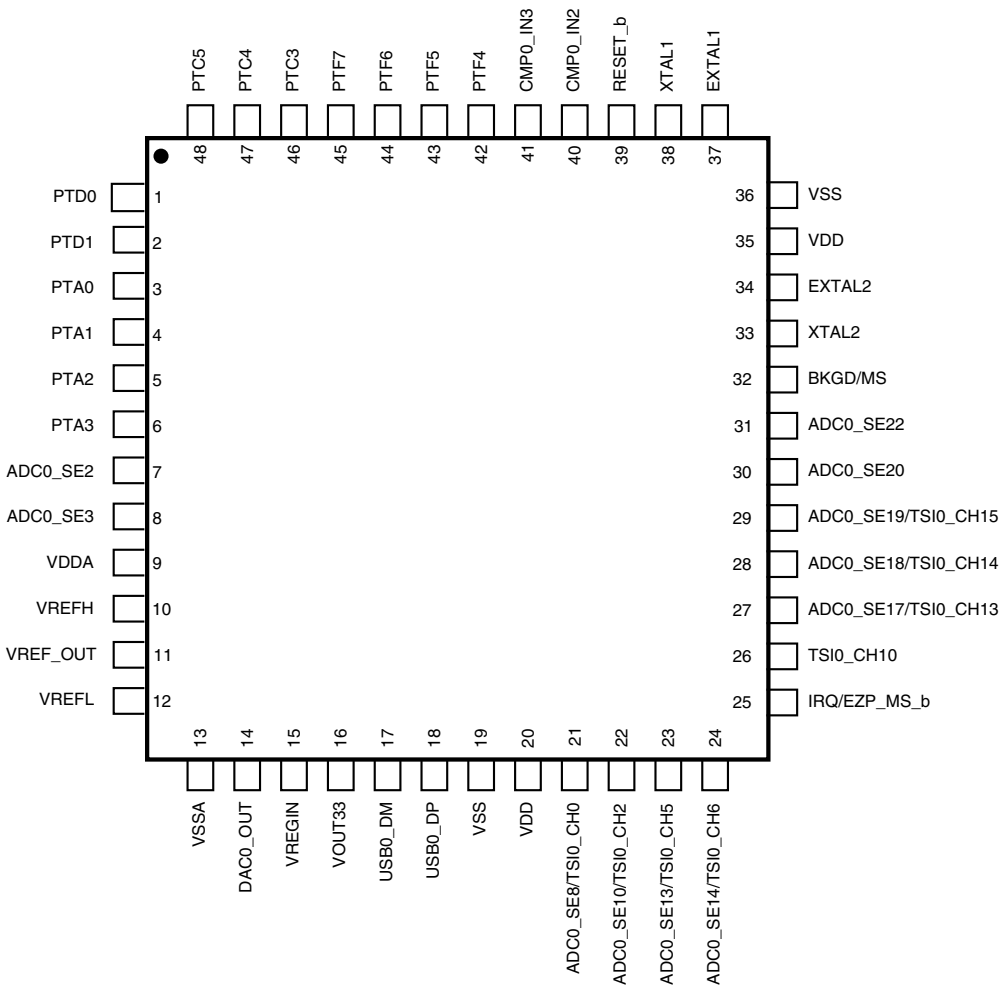


Figure 21. 48-pin LQFP

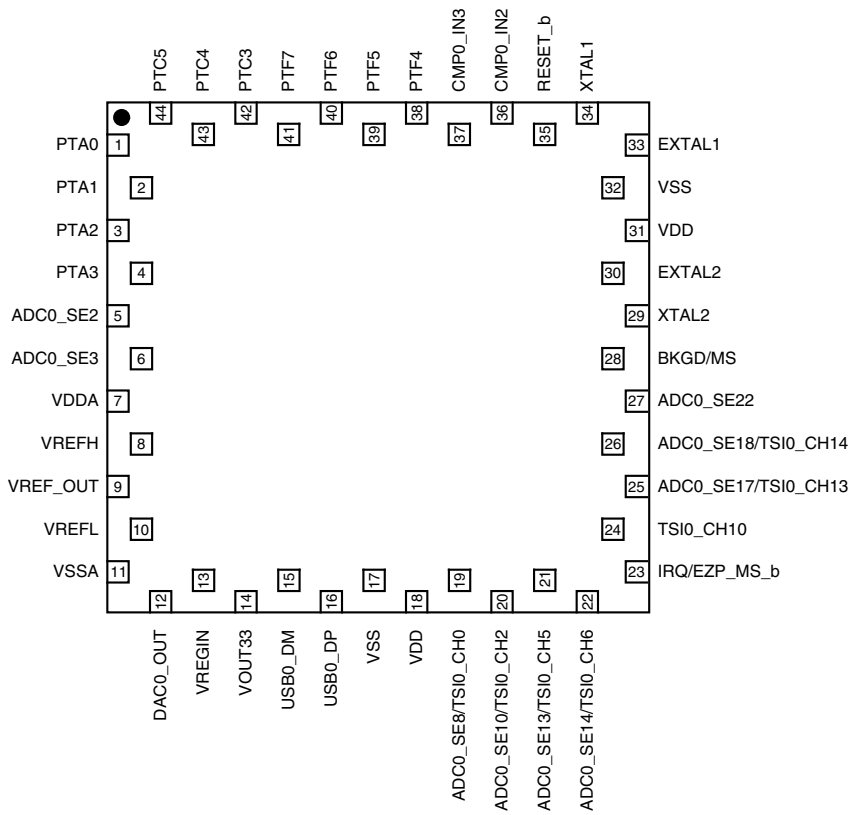


Figure 22. 44-pin Laminate QFN

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17
40	28	26	20	PTB3	ADC0_SE18
41	29			PTE4	ADC0_SE19
42	30			PTE5	ADC0_SE20
43				PTE6	ADC0_SE21
44	31	27		PTE7	ADC0_SE22
13	9	7	7		VDDA
14	10	8			VREFH
16	12	10			VREFL
17	13	11	8		VSSA
DAC0					
18	14	12	9		DAC0_OUT
VREF					
15	11	9			VREF_OUT
CMP0					
53				PTF0	CMP0_IN0
55				PTF2	CMP0_IN1
56	40	36		PTF3	CMP0_IN2
57	41	37	29	PTC2	CMP0_IN3
54				PTF1	CMP0_OUT
CMT					
64	48	44	32	PTC5	CMT_IRO
I2S0					
5	1			PTD0	I2S0_MCLK/ I2S0_CLKIN
62	46	42	30	PTC3	I2S0_MCLK/ I2S0_CLKIN
6	2			PTD1	I2S0_RX_BCLK
61	45	41		PTF7	I2S0_RX_BCLK
7	3	1	1	PTA0	I2S0_RX_FS
60	44	40		PTF6	I2S0_RX_FS
8	4	2	2	PTA1	I2S0_RXD
59	43	39		PTF5	I2S0_RXD
10	6	4	4	PTA3	I2S0_TX_BCLK
58	42	38		PTF4	I2S0_TX_BCLK

Table continues on the next page...

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
11	7	5	5	PTA4	I2S0_TX_FS
57	41	37	29	PTC2	I2S0_TX_FS
12	8	6	6	PTA5	I2S0_TXD
56	40	36		PTF3	I2S0_TXD
TSI0					
25	21	19	15	PTA6	TSI0_CH0
26				PTD2	TSI0_CH1
27	22	20		PTD3	TSI0_CH2
28				PTD4	TSI0_CH3
29				PTD5	TSI0_CH4
30	23	21	16	PTA7	TSI0_CH5
31	24	22		PTD6	TSI0_CH6
32				PTD7	TSI0_CH7
33				PTE0	TSI0_CH8
34				PTE1	TSI0_CH9
36	26	24	18	PTB1	TSI0_CH10
37				PTE2	TSI0_CH11
38				PTE3	TSI0_CH12
39	27	25	19	PTB2	TSI0_CH13
40	28	26	20	PTB3	TSI0_CH14
41	29			PTE4	TSI0_CH15
PDB0					
44	31	27		PTE7	PDB0_EXTRG
63	47	43	31	PTC4	PDB0_EXTRG
FTM0					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2 / FTM0_QD_PHB
26				PTD2	FTM0_CH0/ FTM0_QD_PHA
27	22	20		PTD3	FTM0_CH1 / FTM0_QD_PHB
30	23	21	16	PTA7	FTM0_QD_PHA
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1

Table continues on the next page...

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
43				PTE6	I2C1_SDA
50	37	33	26	PTB7	I2C1_SDA
I2C2 and I2C3					
7	3	1	1	PTA0	I2C2_SCL
11	7	5	5	PTA4	I2C2_SCL
8	4	2	2	PTA1	I2C2_SDA
12	8	6	6	PTA5	I2C2_SDA
32				PTD7	I2C3_SCL
37				PTE2	I2C3_SCL
33				PTE0	I2C3_SDA
38				PTE3	I2C3_SDA
SPI0					
39	27	25	19	PTB2	SPI0_MISO
55				PTF2	SPI0_MISO
63	47	43	31	PTC4	SPI0_MISO
38				PTE3	SPI0_MOSI
40	28	26	20	PTB3	SPI0_MOSI
56	40	36		PTF3	SPI0_MOSI
64	48	44	32	PTC5	SPI0_MOSI
36	26	24	18	PTB1	SPI0_SCLK
54				PTF1	SPI0_SCLK
62	46	42	30	PTC3	SPI0_SCLK
7	3	1	1	PTA0	SPI0_SS
34				PTE1	SPI0_SS
53				PTF0	SPI0_SS
61	45	41		PTF7	SPI0_SS
SPI1					
4				PTC7	SPI1_MISO
11	7	5	5	PTA4	SPI1_MISO
43				PTE6	SPI1_MISO
59	43	39		PTF5	SPI1_MISO
3				PTC6	SPI1_MOSI
12	8	6	6	PTA5	SPI1_MOSI
44	31	27		PTE7	SPI1_MOSI
60	44	40		PTF6	SPI1_MOSI

Table continues on the next page...