NXP USA Inc. - MCF51JU128VLH Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ju128vlh

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to http://www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51JU and MCF51JU.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JF, JU, QF, QH, QM, QU

Table continues on the next page...

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and I^2C signals. The conditions are 50 pf load, V_{DD} = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 9. EGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
	External reset pulse width (digital glitch filter disabled)	100	—	ns
	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

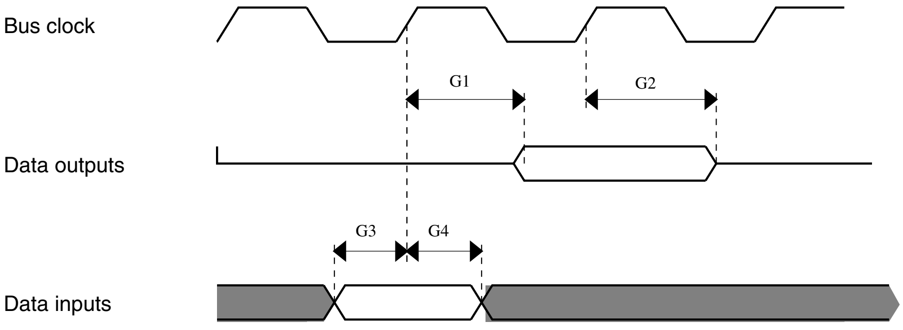


Figure 3. EGPIO timing diagram

Table 17. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 B flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	275	2350	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	μs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	μs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	μs	
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	μs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	

Table continues on the next page...

Table 19. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Write endurance					4
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on T_{javg} = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
4. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —

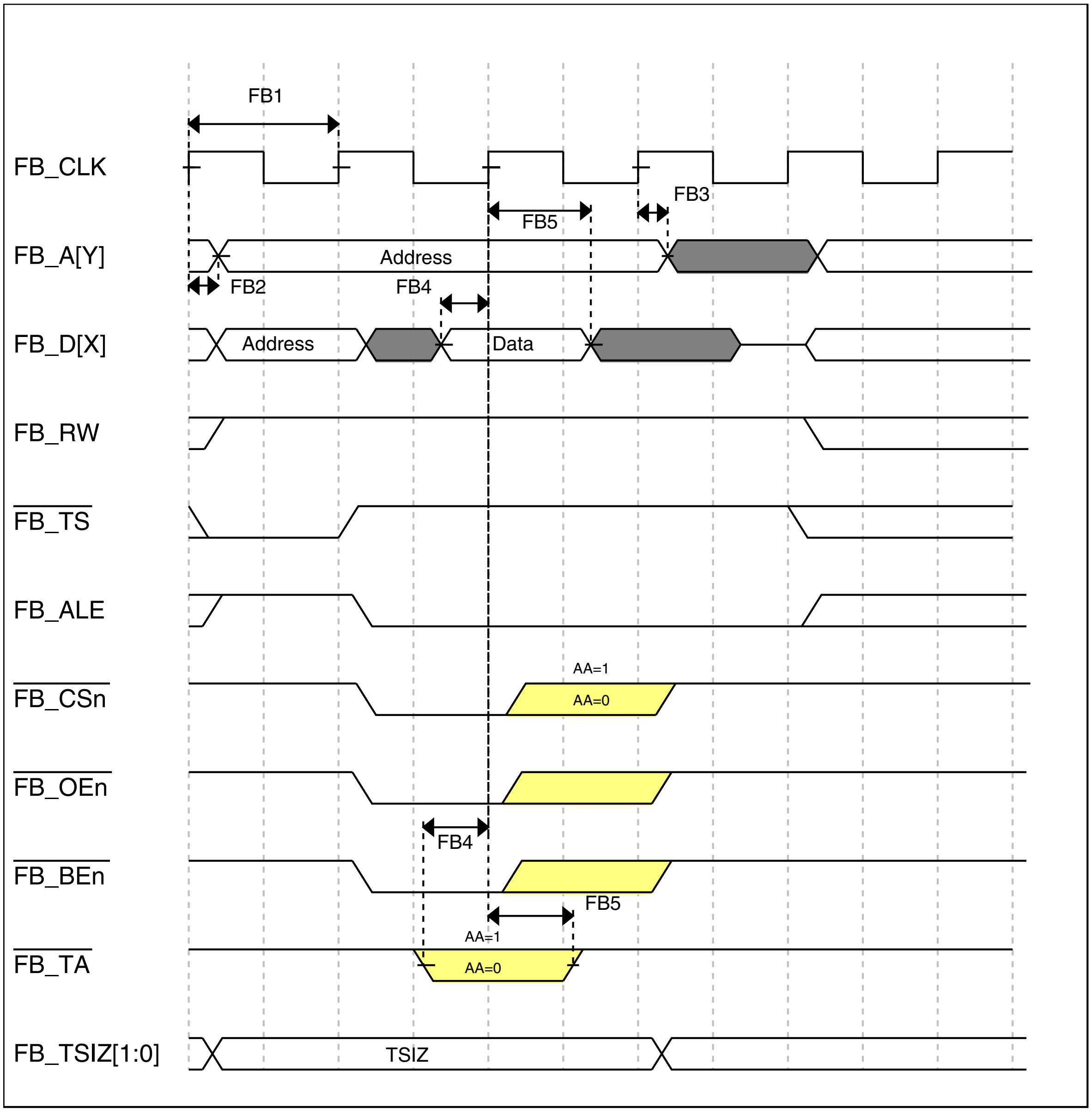


Figure 7. Mini-FlexBus read timing diagram

6.6 Analog

6.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

6.6.1.1 12-bit ADC operating conditions

Table 22. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	Reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 8/10/12 bit modes	— —	4	5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	12 bit modes f_{ADCK} < 4MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 12 bit modes	1.0	—	18.0	MHz	4
C_{rate}	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.

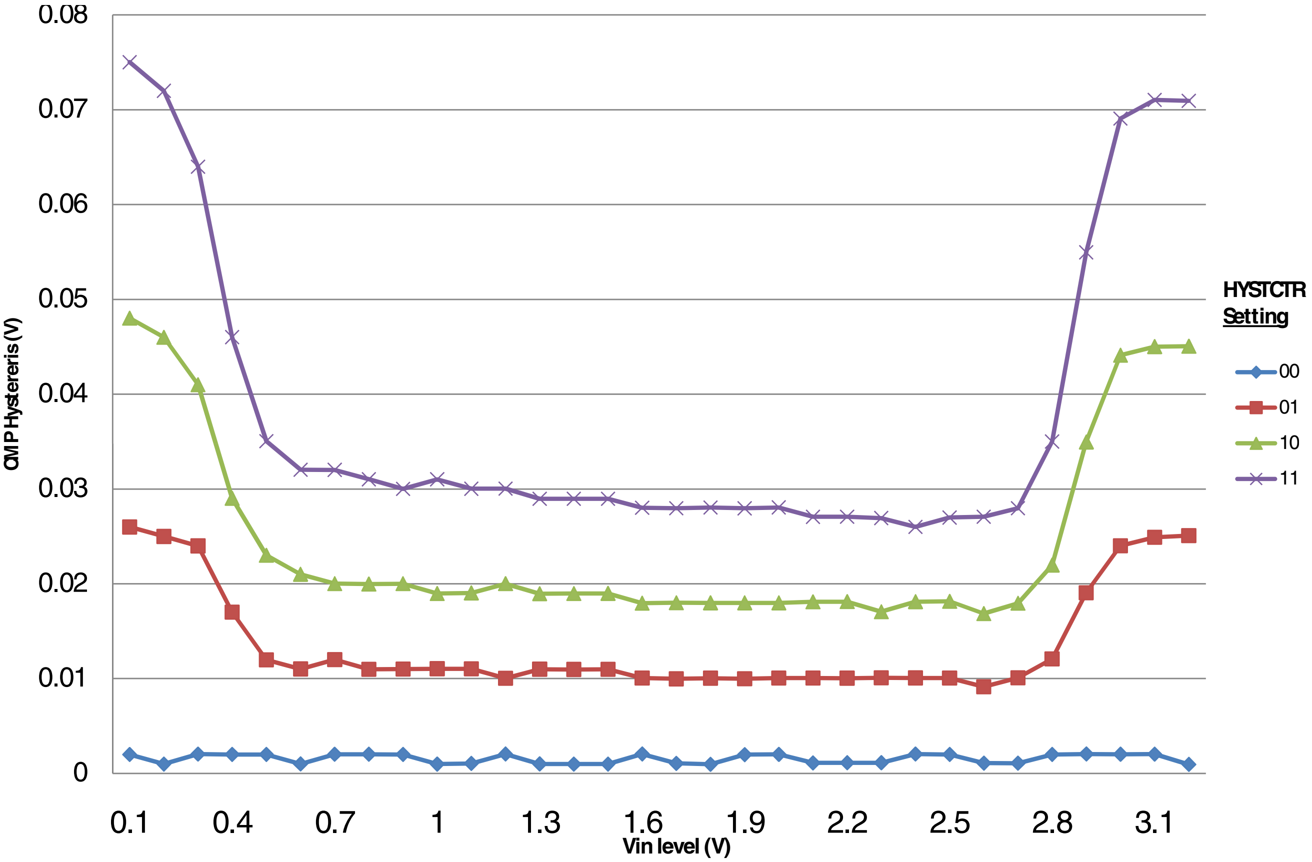


Figure 10. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

6.6.3.2 12-bit DAC operating behaviors

Table 26. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	450	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1000	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} > = 2.4 V	60		90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100 mV to V_{DACR}−100 mV
4. The DNL is measured for 0+100mV to V_{DACR}−100 mV with V_{DDA} > 2.4V

Table 28. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1965	1.2	1.2027	V	
V_{out}	Voltage reference output with— factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only (MODE_LV = 00) current	—	—	80	μA	
I_{tr}	Tight-regulation buffer (MODE_LV =10) current	—	—	1.1	mA	
ΔV_{LOAD}	Load regulation (MODE_LV = 10)				mV	1
	• current = + 1.0 mA	—	2	—		
	• current = - 1.0 mA	—	5	—		
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range) (MODE_LV = 10, REGEN = 1)	—	2	—	mV	

1. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 29. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 30. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General Switching Specifications.

6.8 Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

6.8.2 USB DCD electrical specifications

Table 31. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 μA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	μA
I_{DM_SINK}	USB_DM sink current	50	100	150	μA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

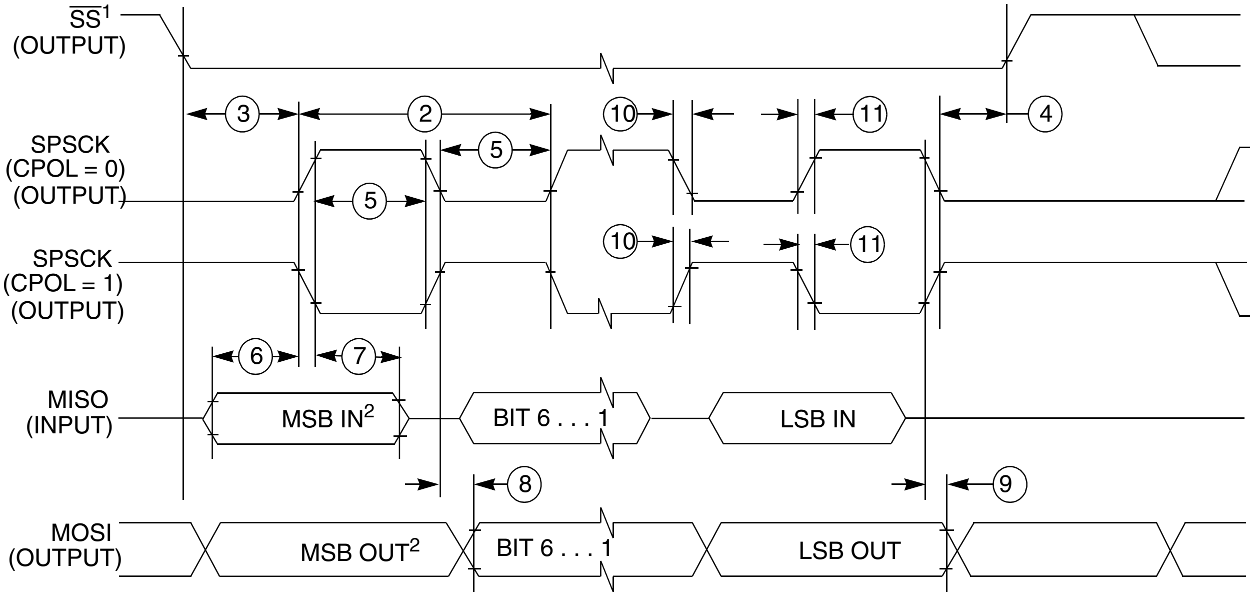
Table 32. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	μA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	μA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA μA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	

Table continues on the next page...

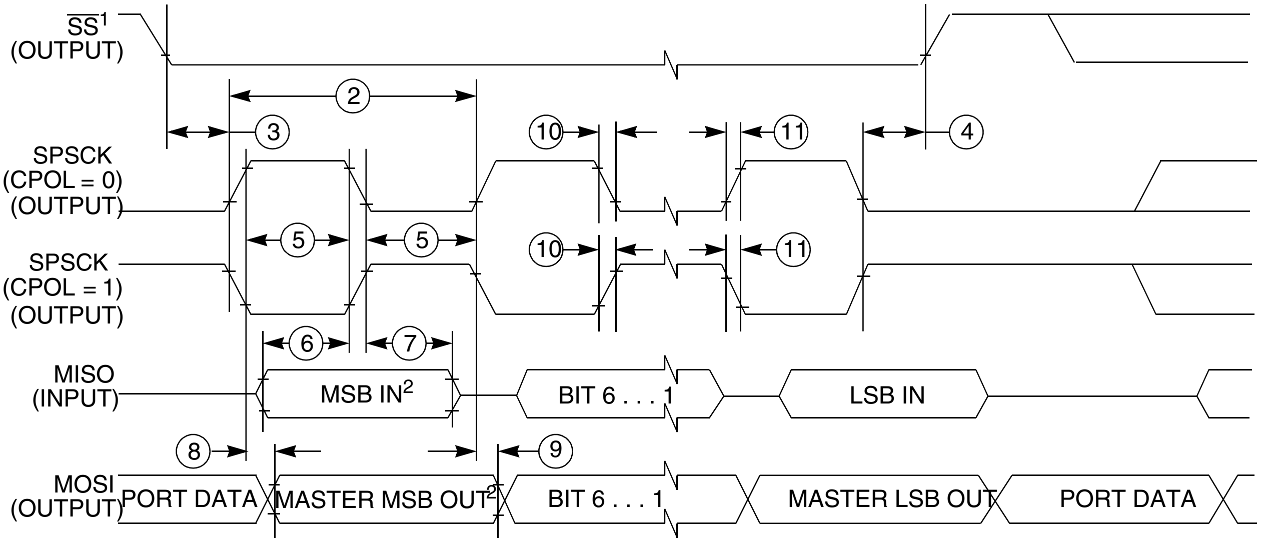
Table 33. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
6	t_{SU}	Data setup time (inputs)	21	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA=0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA=1)

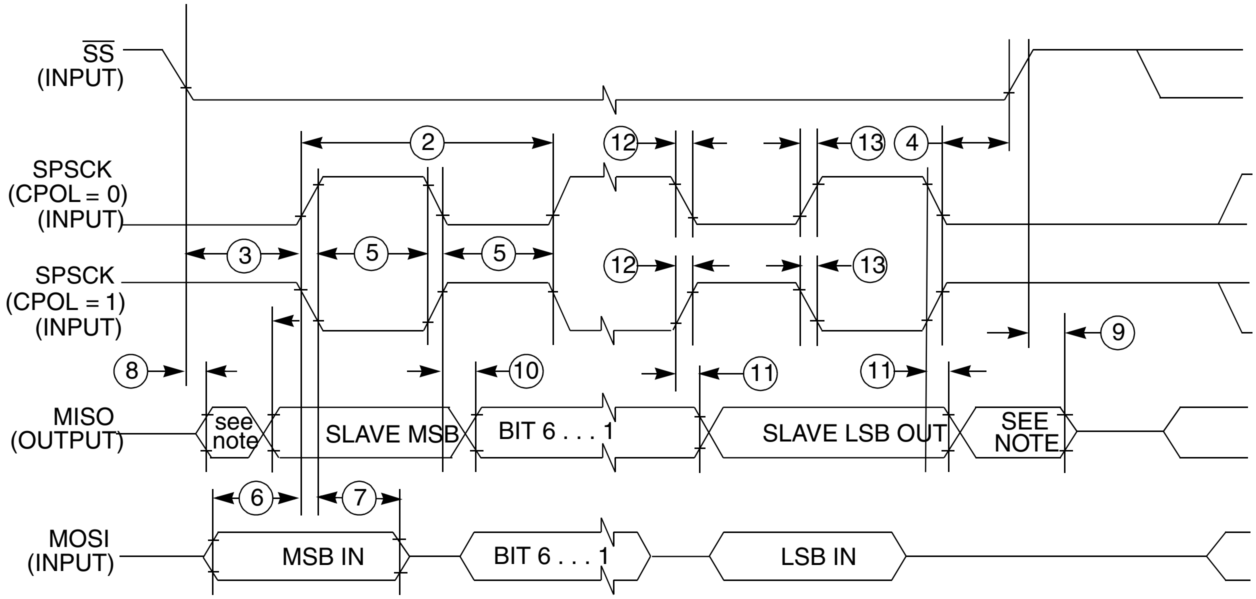
Table 34. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{BUS}/4$	Hz	f_{BUS} is the bus clock as defined in Table 8.
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—

Table continues on the next page...

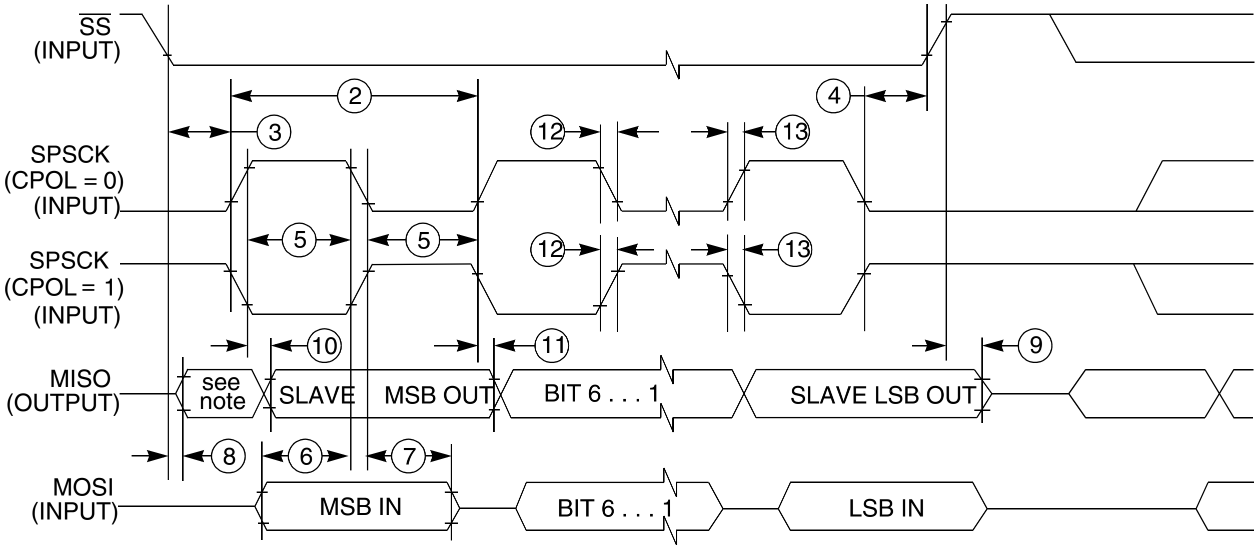
Table 34. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 16. SPI slave mode timing (CPHA=0)



NOTE: Not defined!

Figure 17. SPI slave mode timing (CPHA=1)

8 Pinout

8.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Mux Control module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	—	—	—	VDD	VDD								
2	—	—	—	VSS	VSS								
3	—	—	—	Disabled	Disabled	PTC6	UART0_TX	I2C0_SCL	RGPIO6	SPI1_MOSI	FBa_AD11		
4	—	—	—	Disabled	Disabled	PTC7	UART0_RX	I2C0_SDA	RGPIO7	SPI1_MISO	FBa_AD12		
5	1	—	—	Disabled	Disabled	PTD0	UART0_CTS_b	I2C1_SDA	RGPIO8	SPI1_SCLK	FBa_AD13	I2S0_MCLK / I2S0_CLKIN	
6	2	—	—	Disabled	Disabled	PTD1	UART0_RTS_b	I2C1_SCL	RGPIO9	SPI1_SS	FBa_AD14	I2S0_RX_BCLK	
7	3	1	1	Disabled	Disabled	PTA0		I2C2_SCL	FTM1_CH0	SPI0_SS	FBa_AD15	I2S0_RX_FS	
8	4	2	2	Disabled	Disabled	PTA1		I2C2_SDA	FTM1_CH1		FBa_AD16	I2S0_RXD	
9	5	3	3	Disabled	Disabled	PTA2	UART1_TX		FTM1_CH2	SPI1_SS			
10	6	4	4	Disabled	Disabled	PTA3	UART1_RX		FTM1_CH3	SPI1_SCLK		I2S0_TX_BCLK	EZP_CLK
11	7	5	5	ADC0_SE2	ADC0_SE2	PTA4	UART1_CTS_b	I2C2_SCL	FTM1_CH4	SPI1_MISO		I2S0_TX_FS	EZP_DI
12	8	6	6	ADC0_SE3	ADC0_SE3	PTA5	UART1_RTS_b	I2C2_SDA	FTM1_CH5	SPI1_MOSI	CLKOUT	I2S0_TXD	EZP_DO
13	9	7	7	VDDA	VDDA								
14	10	8	—	VREFH	VREFH								
15	11	9	—	VREF_OUT	VREF_OUT								
16	12	10	—	VREFL	VREFL								
17	13	11	8	VSSA	VSSA								
18	14	12	9	DAC0_OUT	DAC0_OUT								
19	15	13	10	VREGIN	VREGIN								
20	16	14	11	VOUT33	VOUT33								
21	17	15	12	USB0_DM	USB0_DM								

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
22	18	16	13	USB0_DP	USB0_DP								
23	19	17	14	VSS	VSS								
24	20	18	—	VDD	VDD								
25	21	19	15	ADC0_SE8/TSI0_CH0	ADC0_SE8/TSI0_CH0	PTA6		LPTMR_ALT1	FTM_FLT1	FBa_D7	FBa_AD17		
26	—	—	—	ADC0_SE9/TSI0_CH1	ADC0_SE9/TSI0_CH1	PTD2	FTM0_QD_PHA	RGPIO10	FTM0_CH0				
27	22	20	—	ADC0_SE10/TSI0_CH2	ADC0_SE10/TSI0_CH2	PTD3	FTM0_QD_PHB	RGPIO11	FTM0_CH1	FBa_D6	FBa_AD0		
28	—	—	—	ADC0_SE11/TSI0_CH3	ADC0_SE11/TSI0_CH3	PTD4		RGPIO12			FBa_D7		
29	—	—	—	ADC0_SE12/TSI0_CH4	ADC0_SE12/TSI0_CH4	PTD5		RGPIO13			FBa_D6		
30	23	21	16	ADC0_SE13/TSI0_CH5	ADC0_SE13/TSI0_CH5	PTA7	UART0_TX		FTM0_QD_PHA		FBa_D5		
31	24	22	—	ADC0_SE14/TSI0_CH6	ADC0_SE14/TSI0_CH6	PTD6	UART0_RX	RGPIO14			FBa_D4		
32	—	—	—	ADC0_SE15/TSI0_CH7	ADC0_SE15/TSI0_CH7	PTD7	UART0_CTS_b	I2C3_SCL	RGPIO15		FBa_D3		
33	—	—	—	TSI0_CH8	TSI0_CH8	PTE0	UART0_RTS_b	I2C3_SDA			FBa_D2		
34	—	—	—	TSI0_CH9	TSI0_CH9	PTE1	SPI0_SS		FTM_FLT0		FBa_D1		
35	25	23	17	IRQ/EZP_MS_b	Disabled	PTB0		I2C0_SCL		IRQ/EZP_MS_b			EZP_CS_b
36	26	24	18	TSI0_CH10	TSI0_CH10	PTB1	SPI0_SCLK	I2C0_SDA	FTM_FLT2	LPTMR_ALT2	FTM0_QD_PHB	FB_CLKOUT	
37	—	—	—	TSI0_CH11	TSI0_CH11	PTE2		I2C3_SCL			FBa_D0		
38	—	—	—	ADC0_SE16/TSI0_CH12	ADC0_SE16/TSI0_CH12	PTE3	SPI0_MOSI	I2C3_SDA			FBa_OE_b		
39	27	25	19	ADC0_SE17/TSI0_CH13	ADC0_SE17/TSI0_CH13	PTB2	SPI0_MISO				FBa_CS0_b		
40	28	26	20	ADC0_SE18/TSI0_CH14	ADC0_SE18/TSI0_CH14	PTB3	SPI0_MOSI			FBa_CS1_b	FBa_ALE		
41	29	—	—	ADC0_SE19/TSI0_CH15	ADC0_SE19/TSI0_CH15	PTE4	UART0_RTS_b	LPTMR_ALT3	SPI1_SS		FBa_AD1		
42	30	—	—	ADC0_SE20	ADC0_SE20	PTE5	UART0_CTS_b	I2C1_SCL	SPI1_SCLK		FBa_AD2		
43	—	—	—	ADC0_SE21	ADC0_SE21	PTE6	UART0_RX	I2C1_SDA	SPI1_MISO		FBa_AD3		
44	31	27	—	ADC0_SE22	ADC0_SE22	PTE7	UART0_TX	PDB0_EXTRG	SPI1_MOSI	FBa_RW_b	FBa_AD4		
45	32	28	21	BKGD/MS	Disabled	PTB4	BKGD/MS						
46	33	29	22	XTAL2	XTAL2	PTB5							

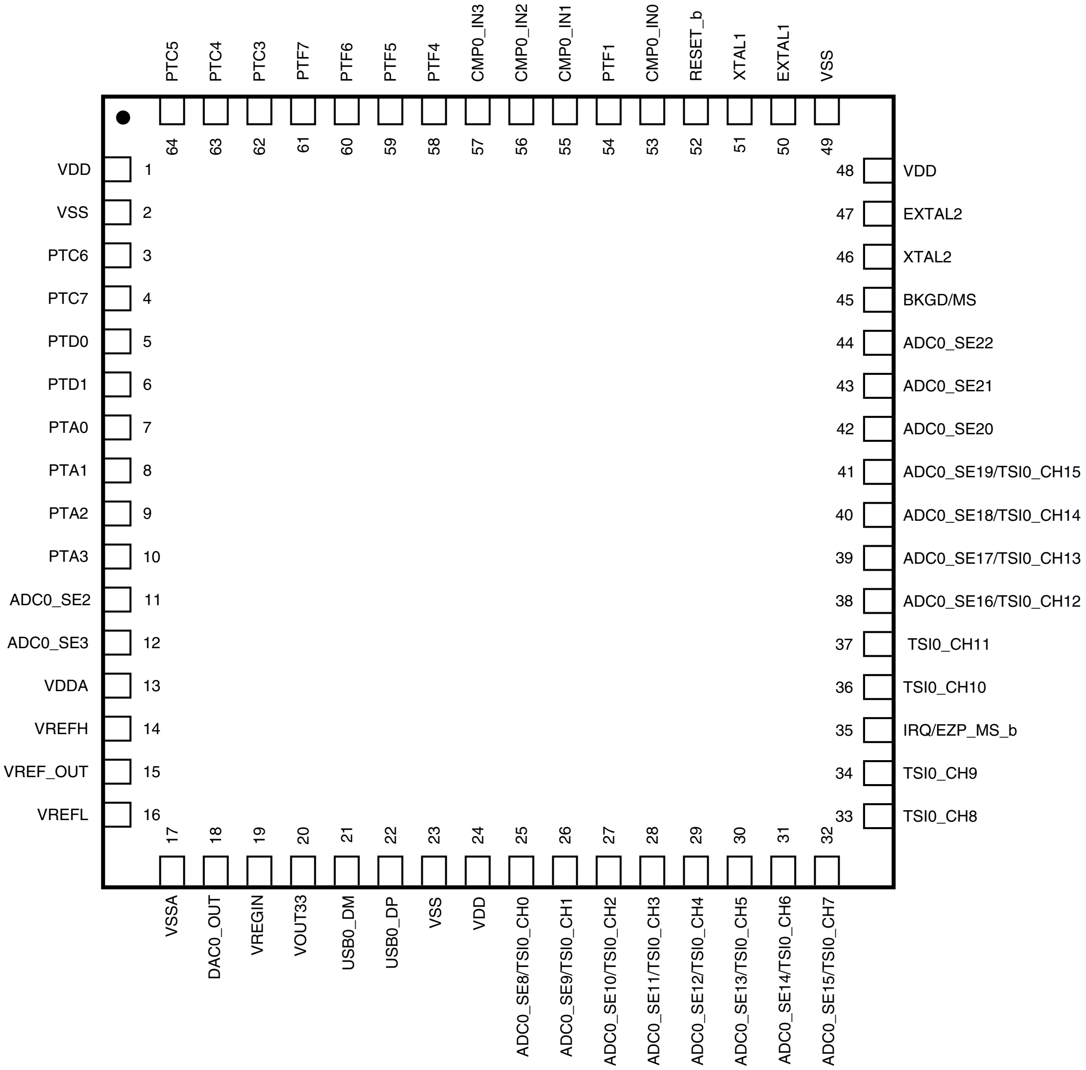


Figure 20. 64-pin LQFP

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
48	35	31	24		VDD
2					VSS
23	19	17	14		VSS
49	36	32	25		VSS
System					
45	32	28	21	PTB4	BKGD/MS
12	8	6	6	PTA5	CLKOUT
62	46	42	30	PTC3	CLKOUT
10	6	4	4	PTA3	EZP_CLK
11	7	5	5	PTA4	EZP_DI
12	8	6	6	PTA5	EZP_DO
35	25	23	17	PTB0	IRQ/EZP_MS_b, EZP_CS_b
52	39	35	28	PTC1	RESET_b
OSC					
50	37	33	26	PTB7	EXTAL1
47	34	30	23	PTB6	EXTAL2
51	38	34	27	PTC0	XTAL1
46	33	29	22	PTB5	XTAL2
LLWU					
4				PTC7	LLWU_P0
6	2			PTD1	LLWU_P1
12	8	6	6	PTA5	LLWU_P2
30	23	21	16	PTA7	LLWU_P3
32				PTD7	LLWU_P4
35	25	23	17	PTB0	LLWU_P5
36	26	24	18	PTB1	LLWU_P6
39	27	25	19	PTB2	LLWU_P7
44	31	27		PTE7	LLWU_P8
45	32	28	21	PTB4	LLWU_P9
55				PTF2	LLWU_P10
56	40	36		PTF3	LLWU_P11
57	41	37	29	PTC2	LLWU_P12
59	43	39		PTF5	LLWU_P13
62	46	42	30	PTC3	LLWU_P14

Table continues on the next page...

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17
40	28	26	20	PTB3	ADC0_SE18
41	29			PTE4	ADC0_SE19
42	30			PTE5	ADC0_SE20
43				PTE6	ADC0_SE21
44	31	27		PTE7	ADC0_SE22
13	9	7	7		VDDA
14	10	8			VREFH
16	12	10			VREFL
17	13	11	8		VSSA
DAC0					
18	14	12	9		DAC0_OUT
VREF					
15	11	9			VREF_OUT
CMP0					
53				PTF0	CMP0_IN0
55				PTF2	CMP0_IN1
56	40	36		PTF3	CMP0_IN2
57	41	37	29	PTC2	CMP0_IN3
54				PTF1	CMP0_OUT
CMT					
64	48	44	32	PTC5	CMT_IRO
I2S0					
5	1			PTD0	I2S0_MCLK/ I2S0_CLKIN
62	46	42	30	PTC3	I2S0_MCLK/ I2S0_CLKIN
6	2			PTD1	I2S0_RX_BCLK
61	45	41		PTF7	I2S0_RX_BCLK
7	3	1	1	PTA0	I2S0_RX_FS
60	44	40		PTF6	I2S0_RX_FS
8	4	2	2	PTA1	I2S0_RXD
59	43	39		PTF5	I2S0_RXD
10	6	4	4	PTA3	I2S0_TX_BCLK
58	42	38		PTF4	I2S0_TX_BCLK

Table continues on the next page...

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