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## What is "Embedded - Microcontrollers"?

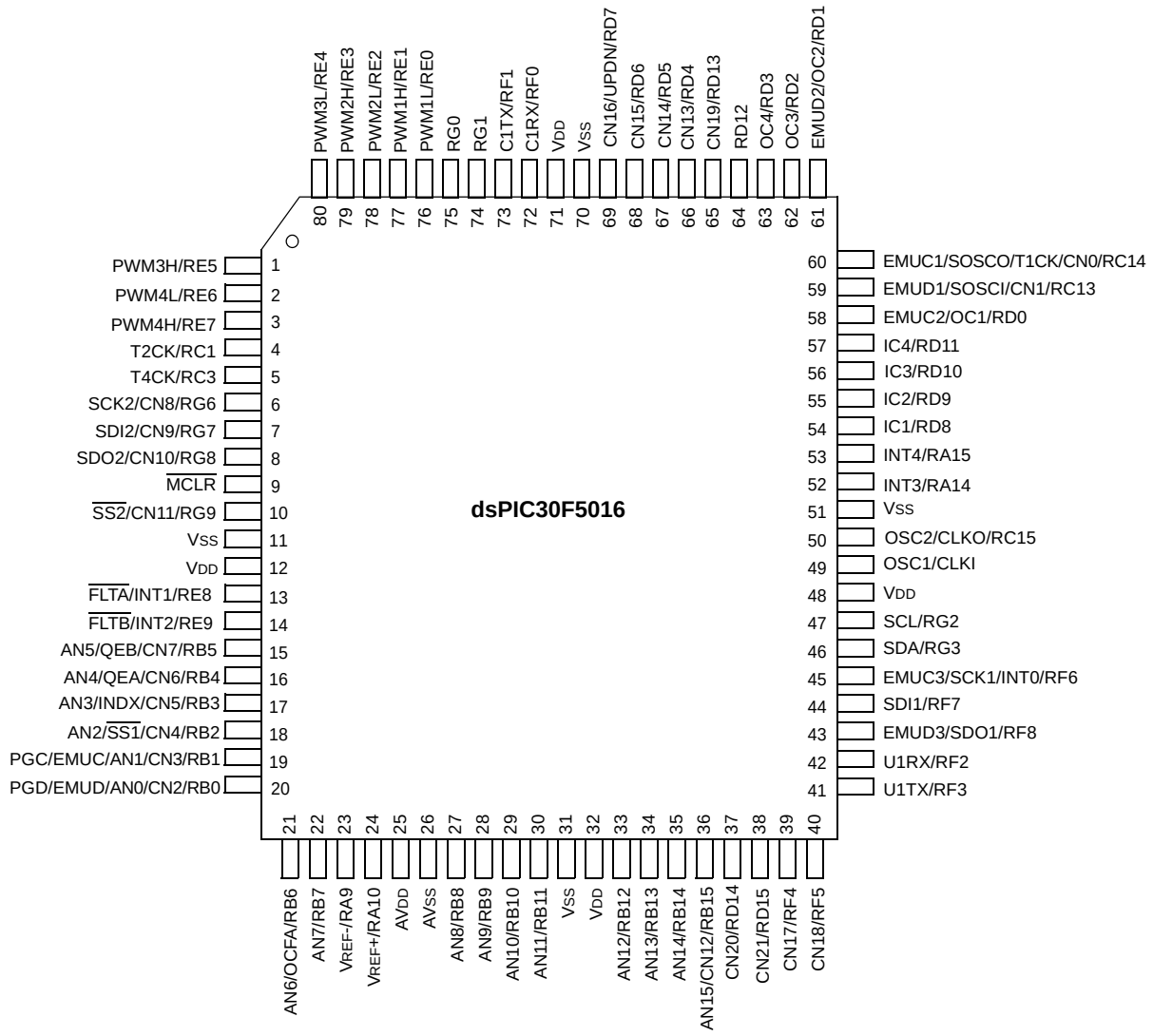
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 30 MIPs |
| Connectivity | CANbus, I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT |
| Number of I/O | 68 |
| Program Memory Size | 66KB (22K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic30f5016-30i-pt |

## Pin Diagram

**80-Pin TQFP**



## 1.0 DEVICE OVERVIEW

| | |
|---|---|
| **Note:** | This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157). |

This document contains device specific information for the dsPIC30F5015/5016 devices. The dsPIC30F devices contain extensive Digital Signal Processor (DSP) functionality within a high-performance 16-bit microcontroller (MCU) architecture.

Figure 1-1 is a block diagram of the dsPIC30F5015 device. Following the block diagram, Table 1-1 provides a brief description of the device I/O pinout and the functions that are multiplexed to the port pins on the dsPIC30F5015.

Figure 1-2 is a block diagram of the dsPIC30F5016 device. Following the block diagram, Table 1-2 provides a brief description of the device I/O pinout and the functions that are multiplexed to the port pins on the dsPIC30F5016.

**FIGURE 2-2: DSP ENGINE BLOCK DIAGRAM**

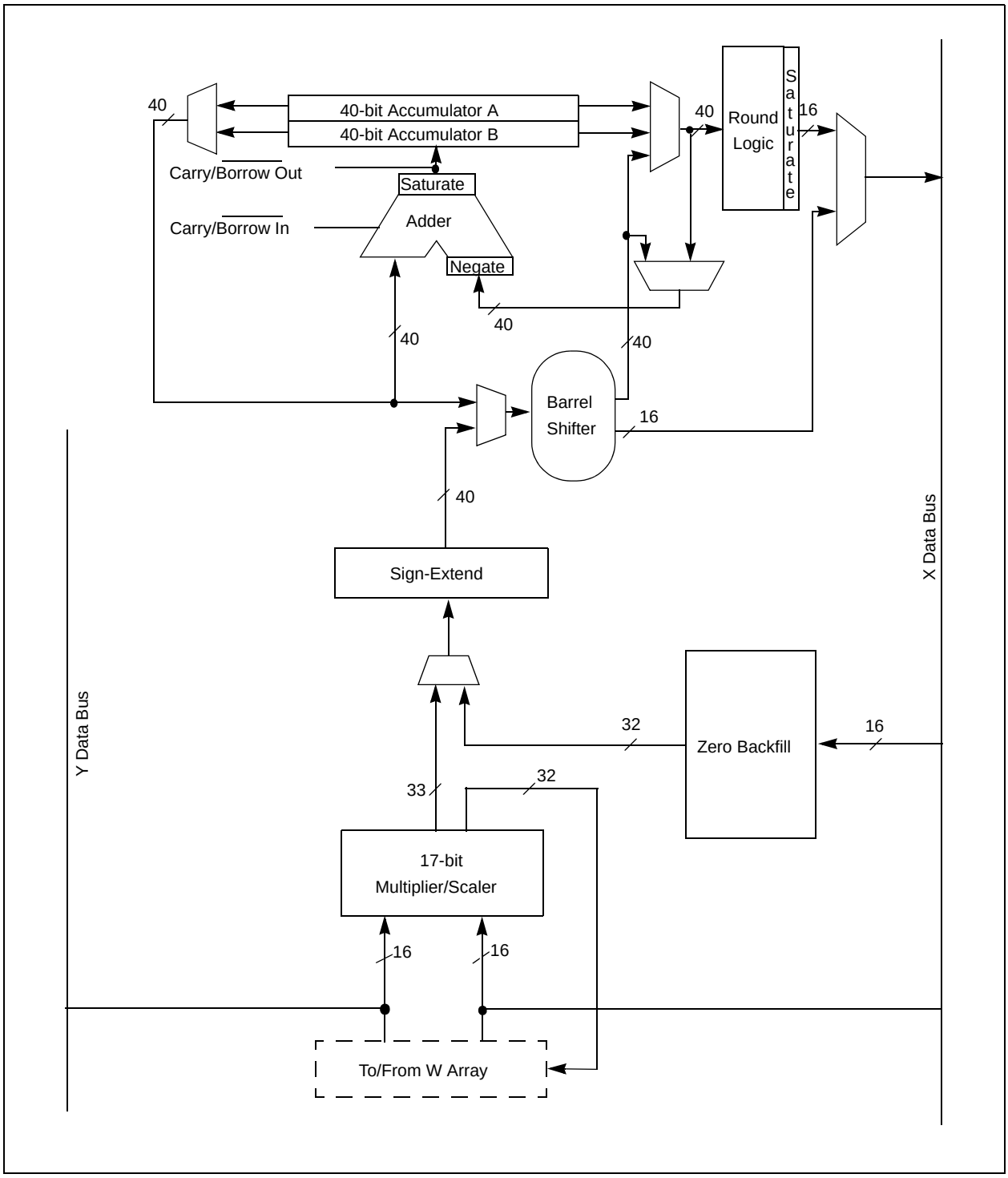


**TABLE 3-3: CORE REGISTER MAP(1)**

| SFR Name | Address (Home) | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0/WREG | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | 0000 1000 0000 0000 |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| ACCAU | 0026 | Sign-Extension (ACCA<39>) | | | | | | | | ACCAU | | | | | | | | 0000 0000 0000 0000 |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| ACCBU | 002C | Sign-Extension (ACCB<39>) | | | | | | | | ACCBU | | | | | | | | 0000 0000 0000 0000 |
| PCL | 002E | PCL | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH | | | | | | | 0000 0000 0000 0000 |
| TBLPAG | 0032 | — | — | — | — | — | — | — | — | TBLPAG | | | | | | | | 0000 0000 0000 0000 |
| PSVPAG | 0034 | — | — | — | — | — | — | — | — | PSVPAG | | | | | | | | 0000 0000 0000 0000 |
| RCOUNT | 0036 | RCOUNT | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| DCOUNT | 0038 | DCOUNT | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| DOSTARTL | 003A | DOSTARTL | | | | | | | | | | | | | | | 0 | uuuu uuuu uuuu uuu0 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | DOSTARTH | | | | | | | 0000 0000 0uuu uuuu |
| DOENDL | 003E | DOENDL | | | | | | | | | | | | | | | 0 | uuuu uuuu uuuu uuu0 |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | DOENDH | | | | | | | 0000 0000 0uuu uuuu |
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 0000 0000 0000 |
| CORCON | 0044 | — | — | — | US | EDT | DL2 | DL1 | DL0 | SATA | SATB | SATDW | ACCSAT | IPL3 | PSV | RND | IF | 0000 0000 0010 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note 1:** Refer to the *"dsPIC30F Family Reference Manual"* (DS70046) for descriptions of register bit fields.

**NOTES:**

## 9.4 Timer Interrupt

The 16-bit timer has the ability to generate an interrupt on period match. When the timer count matches the Period register, the T1IF bit is asserted and an interrupt will be generated, if enabled. The T1IF bit must be cleared in software. The Timer Interrupt Flag, T1IF, is located in the IFS0 Control register in the interrupt controller.

When the Gated Time Accumulation mode is enabled, an interrupt will also be generated on the falling edge of the gate signal (at the end of the accumulation cycle).

Enabling an interrupt is accomplished via the respective Timer Interrupt Enable bit, T1IE. The Timer Interrupt Enable bit is located in the IEC0 Control register in the interrupt controller.

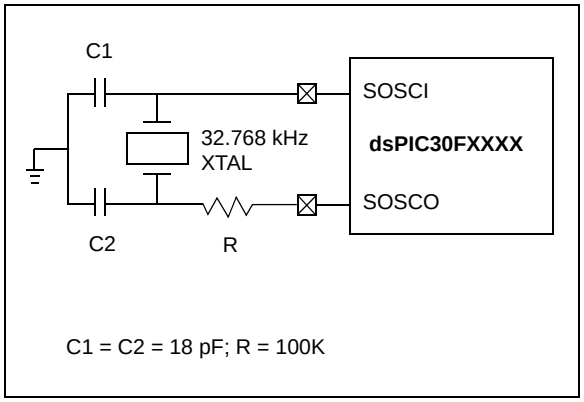
## 9.5 Real-Time Clock

Timer1, when operating in Real-Time Clock (RTC) mode, provides time-of-day and event time-stamping capabilities. Key operational features of the RTC are:

- Operation from 32 kHz LP oscillator
- 8-bit prescaler
- Low power
- Real-Time Clock Interrupts

These operating modes are determined by setting the appropriate bit(s) in the T1CON Control register.

**FIGURE 9-2: RECOMMENDED COMPONENTS FOR TIMER1 LP OSCILLATOR RTC**




### 9.5.1 RTC OSCILLATOR OPERATION

When the TON = 1, TCS = 1 and TGATE = 0, the timer increments on the rising edge of the 32 kHz LP oscillator output signal, up to the value specified in the Period register, and is then reset to '0'.

The TSYNC bit must be asserted to a logic '0' (Asynchronous mode) for correct operation.

Enabling LPOSCEN (OSCCON<1>) will disable the normal Timer and Counter modes and enable a timer carry-out wake-up event.

When the CPU enters Sleep mode, the RTC will continue to operate, provided the 32 kHz external crystal oscillator is active and the control bits have not been changed. The TSIDL bit should be cleared to '0' in order for RTC to continue operation in Idle mode.

### 9.5.2 RTC INTERRUPTS

When an interrupt event occurs, the respective interrupt flag, T1IF, is asserted and an interrupt will be generated, if enabled. The T1IF bit must be cleared in software. The respective Timer Interrupt Flag, T1IF, is located in the IFS0 Status register in the interrupt controller.

Enabling an interrupt is accomplished via the respective Timer Interrupt Enable bit, T1IE. The Timer Interrupt Enable bit is located in the IEC0 Control register in the interrupt controller.

**TABLE 12-1: INPUT CAPTURE REGISTER MAP(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC1BUF | 0140 | Input 1 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC1CON | 0142 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC2BUF | 0144 | Input 2 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC2CON | 0146 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC3BUF | 0148 | Input 3 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC3CON | 014A | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC4BUF | 014C | Input 4 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC4CON | 014E | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note 1:** Refer to the *"dsPIC30F Family Reference Manual"* (DS70046) for descriptions of register bit fields.

**NOTES:**

## 14.8 Quadrature Encoder Interface Interrupts

The Quadrature Encoder Interface has the ability to generate an interrupt on occurrence of the following events:

- Interrupt on 16-bit up/down position counter rollover/underflow
- Detection of qualified index pulse, or if CNTERR bit is set
- Timer period match event (overflow/underflow)
- Gate accumulation event

The QEI Interrupt Flag bit, QEIIF, is asserted upon occurrence of any of the above events. The QEIIF bit must be cleared in software. QEIIF is located in the IFS2 Status register.

Enabling an interrupt is accomplished via the respective enable bit, QEIIE. The QEIIE bit is located in the IEC2 Control register.

#### 17.4.1 10-BIT MODE SLAVE TRANSMISSION

Once a slave is addressed in this fashion, with the full 10-bit address (we will refer to this state as “PRIOR_ADDR_MATCH”), the master can begin sending data bytes for a slave reception operation.

#### 17.4.2 10-BIT MODE SLAVE RECEPTION

Once addressed, the master can generate a Repeated Start, reset the high byte of the address and set the R_W bit without generating a Stop bit, thus initiating a slave transmit operation.

## 17.5 Automatic Clock Stretch

In the slave modes, the module can synchronize buffer reads and write to the master device by clock stretching.

#### 17.5.1 TRANSMIT CLOCK STRETCHING

Both 10-bit and 7-bit transmit modes implement clock stretching by asserting the SCLREL bit after the falling edge of the ninth clock if the TBF bit is cleared, indicating the buffer is empty.

In slave transmit modes, clock stretching is always performed, irrespective of the STREN bit.

Clock synchronization takes place following the ninth clock of the transmit sequence. If the device samples an $\overline{\text{ACK}}$ on the falling edge of the ninth clock, and if the TBF bit is still clear, then the SCLREL bit is automatically cleared. The SCLREL being cleared to ‘0’ will assert the SCL line low. The user’s ISR must set the SCLREL bit before transmission is allowed to continue. By holding the SCL line low, the user has time to service the ISR and load the contents of the I2CTRN before the master device can initiate another transmit sequence.

| | |
|---|---|
| **Note 1:** | If the user loads the contents of I2CTRN, setting the TBF bit before the falling edge of the ninth clock, the SCLREL bit will not be cleared and clock stretching will not occur. |
| **2:** | The SCLREL bit can be set in software, regardless of the state of the TBF bit. |

#### 17.5.2 RECEIVE CLOCK STRETCHING

The STREN bit in the I2CCON register can be used to enable clock stretching in Slave Receive mode. When the STREN bit is set, the SCL pin will be held low at the end of each data receive sequence.

#### 17.5.3 CLOCK STRETCHING DURING 7-BIT ADDRESSING (STREN = 1)

When the STREN bit is set in Slave Receive mode, the SCL line is held low when the Buffer register is full. The method for stretching the SCL output is the same for both 7 and 10-bit addressing modes.

Clock stretching takes place following the ninth clock of the receive sequence. On the falling edge of the ninth clock at the end of the ACK sequence, if the RBF bit is set, the SCLREL bit is automatically cleared, forcing the SCL output to be held low. The user’s ISR must set the SCLREL bit before reception is allowed to continue. By holding the SCL line low, the user has time to service the ISR and read the contents of the I2CRCV before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring.

| | |
|---|---|
| **Note 1:** | If the user reads the contents of the I2CRCV, clearing the RBF bit before the falling edge of the ninth clock, the SCLREL bit will not be cleared and clock stretching will not occur. |
| **2:** | The SCLREL bit can be set in software, regardless of the state of the RBF bit. The user should be careful to clear the RBF bit in the ISR before the next receive sequence in order to prevent an overflow condition. |

#### 17.5.4 CLOCK STRETCHING DURING 10-BIT ADDRESSING (STREN = 1)

Clock stretching takes place automatically during the addressing sequence. Because this module has a register for the entire address, it is not necessary for the protocol to wait for the address to be updated.

After the address phase is complete, clock stretching will occur on each data receive or transmit sequence as was described earlier.

## 17.6 Software Controlled Clock Stretching (STREN = 1)

When the STREN bit is ‘1’, the SCLREL bit may be cleared by software to allow software to control the clock stretching. The logic will synchronize writes to the SCLREL bit with the SCL clock. Clearing the SCLREL bit will not assert the SCL output until the module detects a falling edge on the SCL output and SCL is sampled low. If the SCLREL bit is cleared by the user while the SCL line has been sampled low, the SCL output will be asserted (held low). The SCL output will remain low until the SCLREL bit is set, and all other devices on the $I^2C$ bus have deasserted SCL. This ensures that a write to the SCLREL bit will not violate the minimum high time requirement for SCL.

If the STREN bit is ‘0’, a software write to the SCLREL bit will be disregarded and have no effect on the SCLREL bit.

### 18.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF) is located in the corresponding Interrupt Flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on UTXISEL control bit:

- If UTXISEL = 0, an interrupt is generated when a word is transferred from the Transmit buffer to the Transmit Shift register (UxTSR). This implies that the transmit buffer has at least one empty word.
- If UTXISEL = 1, an interrupt is generated when a word is transferred from the Transmit buffer to the Transmit Shift register (UxTSR) and the Transmit buffer is empty.

Switching between the two interrupt modes during operation is possible and sometimes offers more flexibility.

### 18.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) will cause the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB or starting other transmitter activity. Transmission of a break character does not generate a transmit interrupt.

## 18.4 Receiving Data

### 18.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

1. Set up the UART (see **Section 18.3.1 "Transmitting in 8-bit Data Mode"**).
2. Enable the UART (see **Section 18.3.1 "Transmitting in 8-bit Data Mode"**).
3. A receive interrupt will be generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read the received data from UxRXREG. The act of reading UxRXREG will move the next word to the top of the receive FIFO, and the PERR and FERR values will be updated.

### 18.4.2 RECEIVE BUFFER (UxRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 implies that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer will be read and no data shift will occur within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a Power-Saving mode.

### 18.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding Interrupt Flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

- If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the Receive Buffer. There may be one or more characters in the receive buffer.
- If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the Receive Buffer, which, as a result of the transfer, contains 3 characters.
- If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the Receive Buffer, which, as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

## 18.5 Reception Error Handling

### 18.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

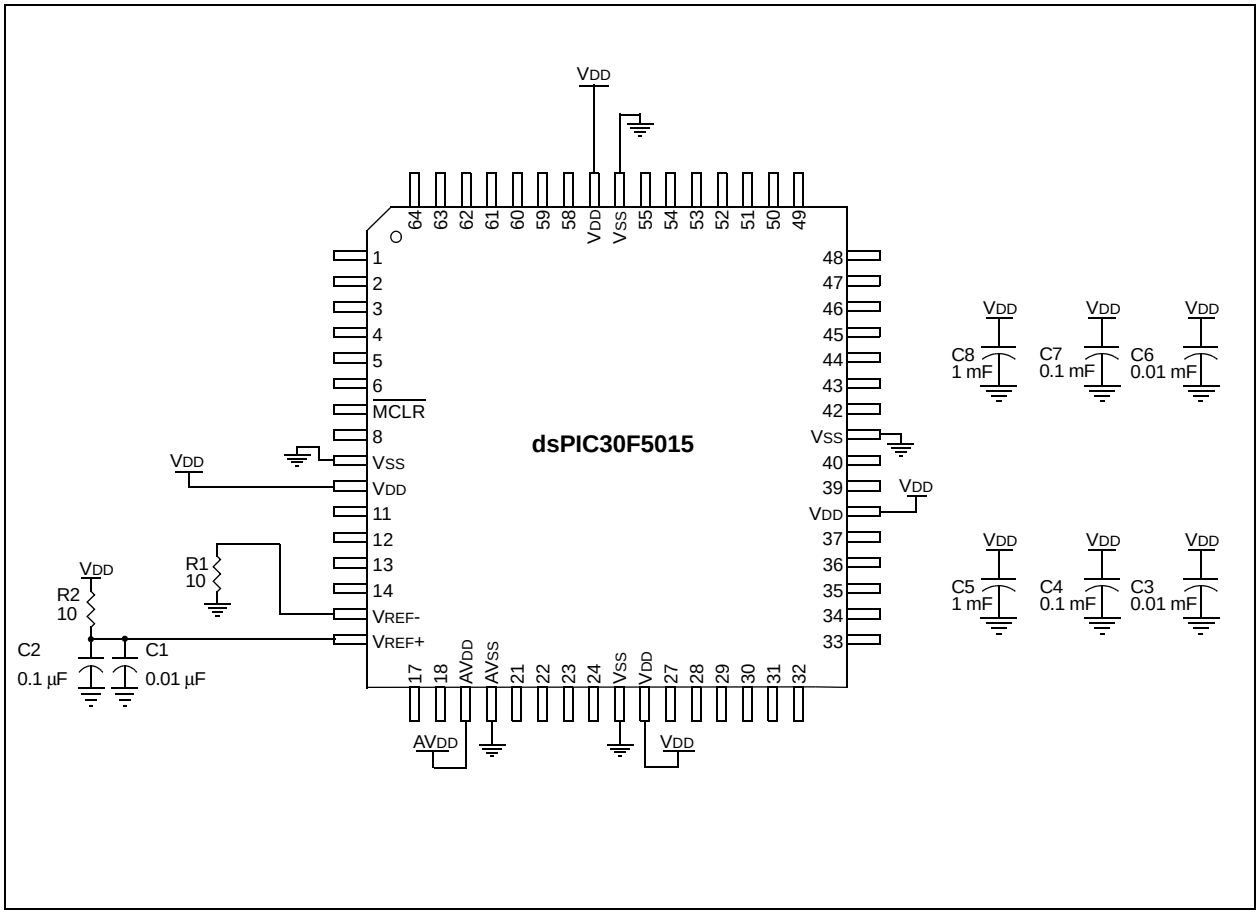
- The receive buffer is full.
- The Receive Shift register is full, but unable to transfer the character to the receive buffer.
- The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

The configuration guidelines give the required setup values for the conversion speeds above 500 ksps, since they require external VREF pins usage and there are some differences in the configuration procedure. Configuration details that are not critical to the conversion speed have been omitted.

The following figure depicts the recommended circuit for the conversion rates above 500 ksps.

**FIGURE 20-2: ADC VOLTAGE REFERENCE SCHEMATIC**




### 20.7.1 1 Msps CONFIGURATION GUIDELINE

The configuration for 1 Msps operation is dependent on whether a single input pin is to be sampled or whether multiple pins will be sampled.

#### 20.7.1.1 Single Analog Input

For conversions at 1 Msps for a single analog input, at least two sample and hold channels must be enabled. The analog input multiplexer must be configured so that the same input pin is connected to both sample and hold channels. The ADC converts the value held on one S/H channel, while the second S/H channel acquires a new input sample.

#### 20.7.1.2 Multiple Analog Inputs

The ADC can also be used to sample multiple analog inputs using multiple sample and hold channels. In this case, the total 1 Msps conversion rate is divided among the different input signals. For example, four inputs can be sampled at a rate of 250 ksps for each signal or two inputs could be sampled at a rate of 500 ksps for each signal. Sequential sampling must be used in this configuration to allow adequate sampling time on each input.

Table 21-5 shows the Reset conditions for the RCON register. Since the control bits within the RCON register are R/W, the information in the table implies that all the bits are negated prior to the action specified in the condition column.

**TABLE 21-5: INITIALIZATION CONDITION FOR RCON REGISTER CASE 1**

| Condition | Program Counter | TRAPR | IOPUWR | EXTR | SWR | WDTO | IDLE | SLEEP | POR | BOR |
|---|---|---|---|---|---|---|---|---|---|---|
| Power-on Reset | 0x000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Brown-out Reset | 0x000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| $\overline{\text{MCLR}}$ Reset during normal operation | 0x000000 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Software Reset during normal operation | 0x000000 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| $\overline{\text{MCLR}}$ Reset during Sleep | 0x000000 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| $\overline{\text{MCLR}}$ Reset during Idle | 0x000000 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| WDT Time-out Reset | 0x000000 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| WDT Wake-up | PC + 2 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Interrupt Wake-up from Sleep | PC + 2(1) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Clock Failure Trap | 0x000004 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Trap Reset | 0x000000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Illegal Operation Trap | 0x000000 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note 1:** When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

Table 21-6 shows a second example of the bit conditions for the RCON register. In this case, it is not assumed the user has set/cleared specific bits prior to action specified in the condition column.

**TABLE 21-6: INITIALIZATION CONDITION FOR RCON REGISTER CASE 2**

| Condition | Program Counter | TRAPR | IOPUWR | EXTR | SWR | WDTO | IDLE | SLEEP | POR | BOR |
|---|---|---|---|---|---|---|---|---|---|---|
| Power-on Reset | 0x000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Brown-out Reset | 0x000000 | u | u | u | u | u | u | u | 0 | 1 |
| $\overline{\text{MCLR}}$ Reset during normal operation | 0x000000 | u | u | 1 | 0 | 0 | 0 | 0 | u | u |
| Software Reset during normal operation | 0x000000 | u | u | 0 | 1 | 0 | 0 | 0 | u | u |
| $\overline{\text{MCLR}}$ Reset during Sleep | 0x000000 | u | u | 1 | u | 0 | 0 | 1 | u | u |
| $\overline{\text{MCLR}}$ Reset during Idle | 0x000000 | u | u | 1 | u | 0 | 1 | 0 | u | u |
| WDT Time-out Reset | 0x000000 | u | u | 0 | 0 | 1 | 0 | 0 | u | u |
| WDT Wake-up | PC + 2 | u | u | u | u | 1 | u | 1 | u | u |
| Interrupt Wake-up from Sleep | PC + 2(1) | u | u | u | u | u | u | 1 | u | u |
| Clock Failure Trap | 0x000004 | u | u | u | u | u | u | u | u | u |
| Trap Reset | 0x000000 | 1 | u | u | u | u | u | u | u | u |
| Illegal Operation Reset | 0x000000 | u | 1 | u | u | u | u | u | u | u |

**Legend:** u = unchanged

**Note 1:** When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions, but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction, require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

**Note:** For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

**TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator write-back destination address register ∈ {W13, [W13] + = 2} |
| bit4 | 4-bit bit selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0x0000...0x1FFF} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16384} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388608}; LSB must be '0' |
| None | Field does not require an entry, may be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |

## 24.1 DC Characteristics

**TABLE 24-1: OPERATING MIPS VS. VOLTAGE FOR dsPIC30F5015**

| VDD Range (in Volts) | Temp Range (in °C) | Max MIPS | |
|---|---|---|---|
| | | dsPIC30F5015-30I | dsPIC30F5015-20E |
| 4.5-5.5 | -40 to +85 | 30 | — |
| 4.5-5.5 | -40 to +125 | — | 20 |
| 3.0-3.6 | -40 to +85 | 20 | — |
| 3.0-3.6 | -40 to +125 | — | 15 |
| 2.5-3.0 | -40 to +85 | 10 | — |

**TABLE 24-2: OPERATING MIPS VS. VOLTAGE FOR dsPIC30F5016**

| VDD Range (in Volts) | Temp Range (in °C) | Max MIPS | |
|---|---|---|---|
| | | dsPIC30F5016-30I | dsPIC30F5016-20E |
| 4.5-5.5 | -40 to +85 | 30 | — |
| 4.5-5.5 | -40 to +125 | — | 20 |
| 3.0-3.6 | -40 to +85 | 20 | — |
| 3.0-3.6 | -40 to +125 | — | 15 |
| 2.5-3.0 | -40 to +85 | 10 | — |

**TABLE 24-3: THERMAL OPERATING CONDITIONS FOR dsPIC30F5015/5016**

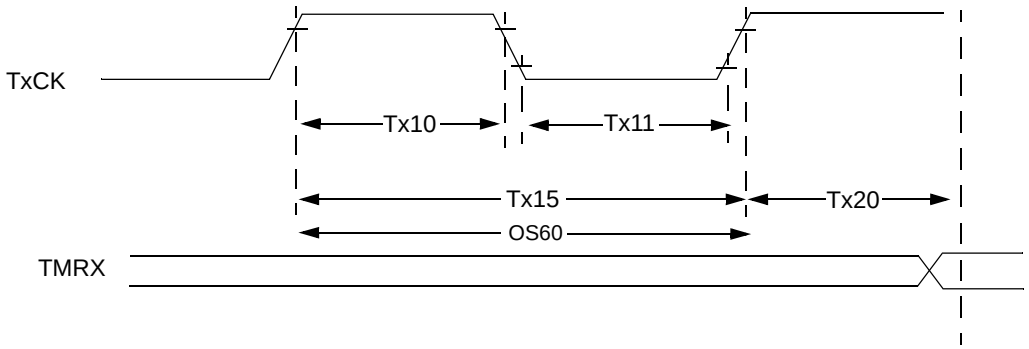
| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| dsPIC30F5015-30I/dsPIC30F5016-30I | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| dsPIC30F5015-20E/dsPIC30F5016-20E | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +150 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>$P_{INT} = V_{DD} \times \left(I_{DD} - \sum I_{OH}\right)$<br>I/O Pin Power Dissipation:<br>$P_{I/O} = \sum(\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum(V_{OL} \times I_{OL})$ | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 24-4: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 80-pin TQFP (12x12x1mm) | θJA | 39 | — | °C/W | **1** |
| Package Thermal Resistance, 64-pin TQFP (10x10x1mm) | θJA | 39 | — | °C/W | **1** |

**Note 1:** Junction to ambient thermal resistance, Theta-ja (θJA) numbers are achieved by package simulations.

**FIGURE 24-7: TIMER1, 2, 3, 4 AND 5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 24-2 for load conditions.

**TABLE 24-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TA15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| | | | Asynchronous | 10 | — | — | ns | |
| TA11 | TTXL | TxCK Low Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TA15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| | | | Asynchronous | 10 | — | — | ns | |
| TA15 | TTXP | TxCK Input Period | Synchronous, no prescaler | TCY + 10 | — | — | ns | — |
| | | | Synchronous, with prescaler | Greater of: 20 ns or (TCY + 40)/N | — | — | — | N = prescale value (1, 8, 64, 256) |
| | | | Asynchronous | 20 | — | — | ns | — |
| OS60 | Ft1 | SOSC1/T1CK oscillator input frequency range (oscillator enabled by setting bit TCS (T1CON, bit 1)) | | DC | — | 50 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.5 TCY | — | 1.5 TCY | — | — |

**Note 1:** Timer1 is a Type A.

**TABLE 24-40: 10-BIT HIGH-SPEED A/D MODULE SPECIFICATIONS(1) (CONTINUED)**

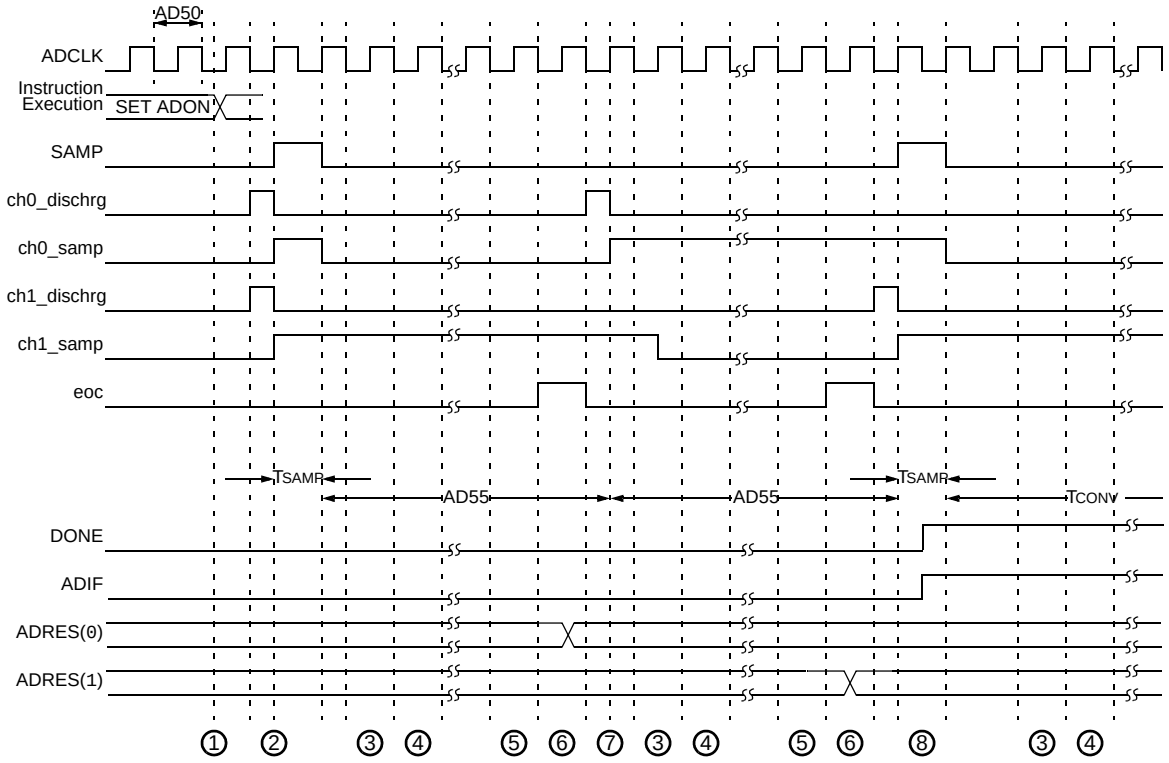
| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.7V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| AD24 | EOFF | Offset Error(2) | ±1 | ±2 | ±3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V |
| AD24A | EOFF | Offset Error(2) | ±1 | ±2 | ±3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V |
| AD25 | — | Monotonicity(3) | — | — | — | — | Guaranteed |
| **Dynamic Performance** | | | | | | | |
| AD30 | THD | Total Harmonic Distortion | — | -64 | -67 | dB | — |
| AD31 | SINAD | Signal to Noise and Distortion | — | 57 | 58 | dB | — |
| AD32 | SFDR | Spurious Free Dynamic Range | — | 67 | 71 | dB | — |
| AD33 | FNYQ | Input Signal Bandwidth | — | — | 500 | kHz | — |
| AD34 | ENOB | Effective Number of Bits | 9.29 | 9.41 | — | bits | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Measurements taken with external VREF+ and VREF- used as the ADC voltage references.

**3:** The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

**FIGURE 24-26: 10-BIT HIGH-SPEED A/D CONVERSION TIMING CHARACTERISTICS (CHPS = 01, SIMSAM = 0, ASAM = 1, SSRC = 111, SAMC = 00001)**




(1) – Software sets ADCON. ADON to start AD operation.

(2) – Sampling starts after discharge period.
TSAMP is described in **Section 17. "10-bit A/D Converter"** of the "*dsPIC30F Family Reference Manual" (*DS70046).

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

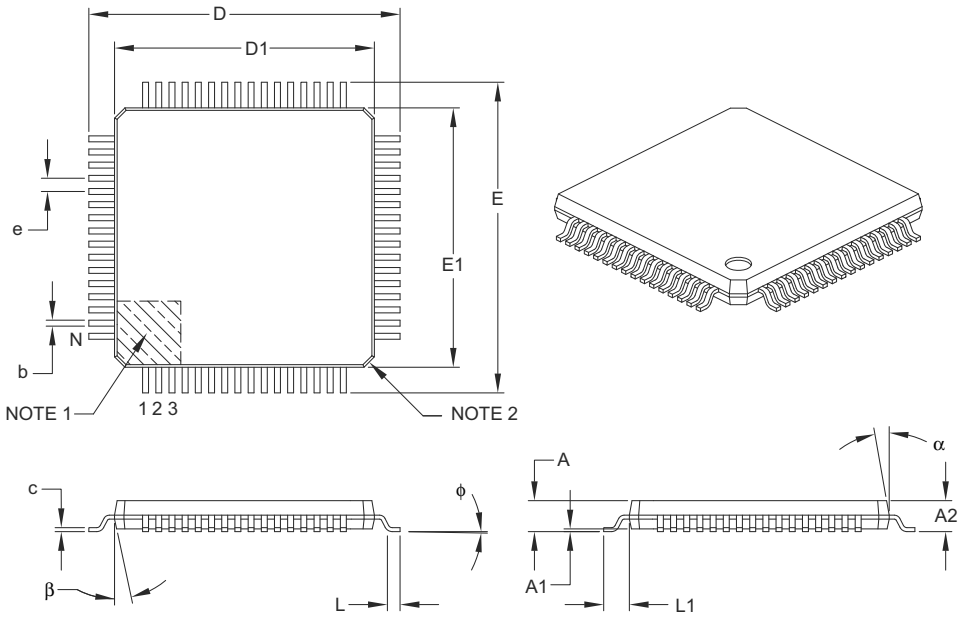
(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC.
TSAMP is described in **Section 17. "10-bit Converter"** of the *"dsPIC30F Family Reference Manual" (*DS70046).

### 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | φ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B