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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM9® |
| Core Size | 16/32-Bit |
| Speed | 96MHz |
| Connectivity | CANbus, I²C, Microwire, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 2V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/str910fm32x6 |

See *Table 2* for recommended interrupt source assignments to physical IRQ interrupt channels. Interrupt source assignments are made by CPU firmware during initialization, thus establishing interrupt priorities.

**Table 2. Recommended IRQ Channel assignments (set by CPU firmware)**

| VIC IRQ Channel | Logic Block | Interrupt Source |
|---|---|---|
| 0 (high priority) | WatchDog | Timeout in WDT mode, Terminal Count in Counter Mode |
| 1 | CPU Firmware | Firmware generated interrupt |
| 2 | CPU Core | Debug Receive Command |
| 3 | CPU Core | Debug Transmit Command |
| 4 | TIM Timer 0 | Logic OR of ICI0_0, ICI0_1, OCI0_0, OCI0_1, Timer overflow |
| 5 | TIM Timer 1 | Logic OR of ICI1_0, ICI1_1, OCI1_0, OCI1_1, Timer overflow |
| 6 | TIM Timer 2 | Logic OR of ICI2_0, ICI2_1, OCI2_0, OCI2_1, Timer overflow |
| 7 | TIM Timer 3 | Logic OR of ICI3_0, ICI3_1, OCI3_0, OCI3_1, Timer overflow |
| 8 | USB | Logic OR of high priority USB interrupts |
| 9 | USB | Logic OR of low priority USB interrupts |
| 10 | CCU | Logic OR of all interrupts from Clock Control Unit |
| 11 | Ethernet MAC | Logic OR of Ethernet MAC interrupts via its own dedicated DMA channel. |
| 12 | DMA | Logic OR of interrupts from each of the 8 individual DMA channels |
| 13 | CAN | Logic OR of all CAN interface interrupt sources |
| 14 | IMC | Logic OR of 8 Induction Motor Control Unit interrupts |
| 15 | ADC | End of AtoD conversion interrupt |
| 16 | UART0 | Logic OR of 5 interrupts from UART channel 0 |
| 17 | UART1 | Logic OR of 5 interrupts from UART channel 1 |
| 18 | UART2 | Logic OR of 5 interrupts from UART channel 2 |
| 19 | I2C0 | Logic OR of transmit, receive, and error interrupts of I2C channel 0 |
| 20 | I2C1 | Logic OR of transmit, receive, and error interrupts of I2C channel 1 |
| 21 | SSP0 | Logic OR of all interrupts from SSP channel 0 |
| 22 | SSP1 | Logic OR of all interrupts from SSP channel 1 |
| 23 | BROWNOUT | LVD warning interrupt |
| 24 | RTC | Logic OR of Alarm, Tamper, or Periodic Timer interrupts |
| 25 | Wake-Up (all) | Logic OR of all 32 inputs of Wake-Up unit (30 pins, RTC, and USB Resume) |
| 26 | Wake-up Group 0 | Logic OR of 8 interrupt sources: RTC, USB Resume, pins P3.2 to P3.7 |
| 27 | Wake-up Group 1 | Logic OR of 8 interrupts from pins P5.0 to P5.7 |
| 28 | Wake-up Group 2 | Logic OR of 8 interrupts from pins P6.0 to P6.7 |
| 29 | Wake-up Group 3 | Logic OR of 8 interrupts from pins P7.0 to P7.7 |
| 30 | USB | USB Bus Resume Wake-up (also input to wake-up unit) |
| 31 (low priority) | PFQ-BC | Special use of interrupts from Prefetch Queue and Branch Cache |

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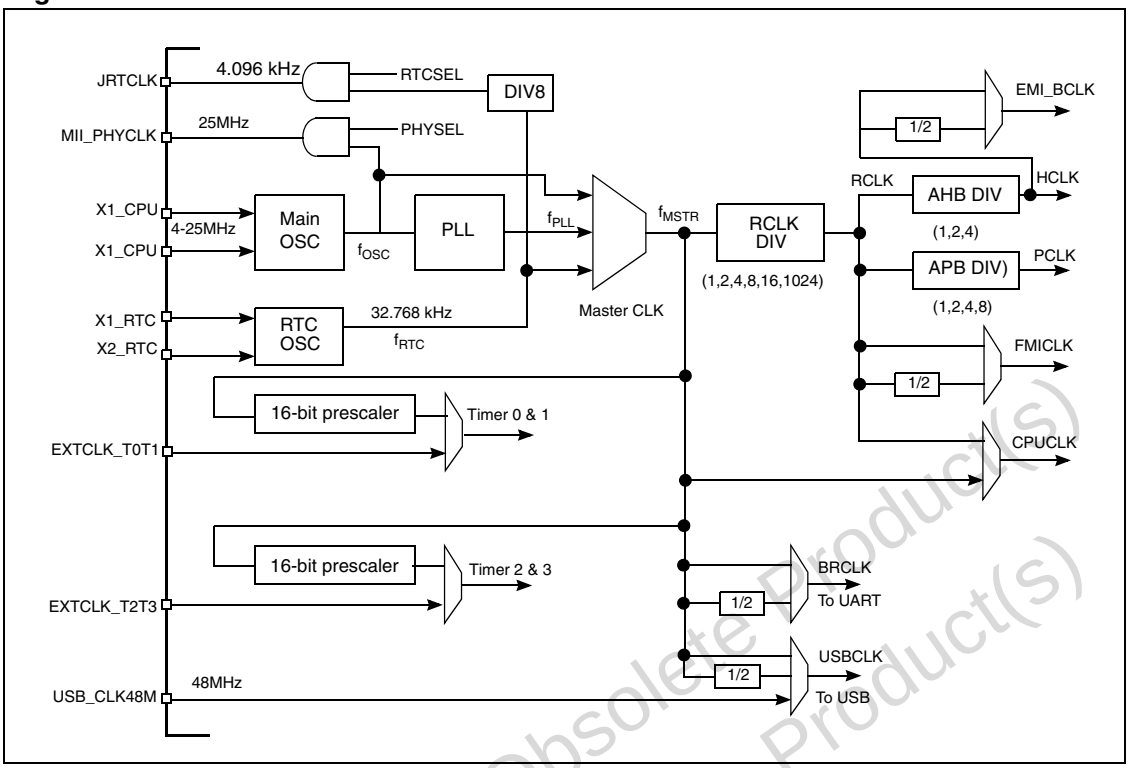
**Figure 2. Clock control**




## 2.10.2 Reference clock (RCLK)

The main clock ($f_{MSTR}$) can be divided to operate at a slower frequency reference clock (RCLK) for the ARM core and all the peripherals. The RCLK provides the divided clock for the ARM core, and feeds the dividers for the AHB, APB, External Memory Interface, and FMI units.

## 2.10.3 AHB clock (HCLK)

The RCLK can be divided by 1, 2 or 4 to generate the AHB clock. The AHB clock is the bus clock for the AHB bus and all bus transfers are synchronized to this clock. The maximum HCLK frequency is 96 MHz.

## 2.10.4 APB clock (PCLK)

The RCLK can be divided by 1, 2, 4 or 8 to generate the APB clock. The APB clock is the bus clock for the APB bus and all bus transfers are synchronized to this clock. Many of the peripherals that are connected to the AHB bus also use the PCLK as the source for external bus data transfers. The maximum PCLK frequency is 48 MHz.

## 2.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96MHz.

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peripheral clock from the APB, and an 8-bit clock pre-scaler is available. When enabled by firmware as a watchdog, this timer will cause a system reset if firmware fails to periodically reload this timer before the terminal count of 0x0000 occurs, ensuring firmware sanity. The watchdog function is off by default after a reset and must be enabled by firmware.

### 2.13.4 External RESET_INn pin

This input signal is active-low with hystereses ($V_{RHYS}$). Other open-drain, active-low system reset signals on the circuit board (such as closure to ground from a push-button) may be connected directly to the RESET_INn pin, but an external pull-up resistor to $V_{DDQ}$ must be present as there is no internal pullup on the RESET_INn pin.

A valid active-low input signal of $t_{RINMIN}$ duration on the RESET_INn pin will cause a system reset within the STR91xF. There is also a RESET_OUTn pin on the STR91xF that can drive other system components on the circuit board. RESET_OUTn is active-low and has the same timing of the Power-On-Reset (POR) shown next, $t_{POR}$.

### 2.13.5 Power-up

The LVD circuitry will always generate a global reset when the STR91xF powers up, meaning internal reset is active until $V_{DDQ}$ and $V_{DD}$ are both above the LVD thresholds. This POR condition has a duration of $t_{POR}$, after which the CPU will fetch its first instruction from address 0x0000.0000 in Flash memory. It is not possible for the CPU to boot from any other source other than Flash memory.

### 2.13.6 JTAG debug command

When the STR91xF is in JTAG debug mode, an external device which controls the JTAG interface can command a system reset to the STR91xF over the JTAG channel.

### 2.13.7 Tamper detection

On 128-pin STR91xF devices only, there is a tamper detect input pin, TAMPER_IN, used to detect and record the time of a tamper event on the end product such as malicious opening of an enclosure, unwanted opening of a panel, etc. The activation mode of the tamper pin is programmable to one of two modes. One is Normally Closed/Tamper Open, the other mode will detect when a signal on the tamper input pin is driven from low-to-high, or high-to-low depending on firmware configuration. Once a tamper event occurs, the RTC time (millisecond resolution) and the date are recorded in the RTC unit. Simultaneously, the SRAM standby voltage source will be cut off to invalidate all SRAM contents. Tamper detection control and status logic are part of the RTC unit.

## 2.14 Real-time clock (RTC)

The RTC combines the functions of a complete time-of-day clock (millisecond resolution) with an alarm programmable up to one month, a 9999-year calender with leap-year support, periodic interrupt generation from 1 to 512 Hz, tamper detection (described in *Section 2.13.7*), and an optional clock calibration output on the JRTCK pin. The time is in 24 hour mode, and time/calendar values are stored in binary-coded decimal format.

The RTC also provides a self-isolation mode that is automatically activated during power down. This feature allows the RTC to continue operation when $V_{DDQ}$ and $V_{DD}$ are absent, as long as

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an alternate power source, such as a battery, is connected to the VBATT input pin. The current drawn by the RTC unit on the VBATT pin is very low in this standby mode, $I_{RTC\_STBY}$.

## 2.15 JTAG interface

An IEEE-1149.1 JTAG interface on the STR91xF provides In-System-Programming (ISP) of all memory, boundary scan testing of pins, and the capability to debug the CPU.

STR91xF devices are shipped from ST with blank Flash memories. The CPU can only boot from Flash memory (selection of which Flash bank is programmable). Firmware must be initially programmed through JTAG into one of these Flash memories before the STR91xF is used.

Six pins are used on this JTAG serial interface. The five signals JTDI, JTDO, JTMS, JTCK, and JTRSTn are all standard JTAG signals complying with the IEEE-1149.1 specification. The sixth signal, JRTCK (Return TCK), is an output from the STR91xF and it is used to pace the JTCK clock signal coming in from the external JTAG test equipment for debugging. The frequency of the JTCK clock signal coming from the JTAG test equipment must be at least 10 times less than the ARM966E-S CPU core operating frequency ($f_{CPUCLK}$). To ensure this, the signal JRTCK is output from the STR91xF and is input to the external JTAG test equipment to hold off transitions of JTCK until the CPU core is ready, meaning that the JTAG equipment cannot send the next rising edge of JTCK until the equipment receives a rising edge of JRTCK from the STR91xF. The JTAG test equipment must be able to interpret the signal JRTCK and perform this adaptive clocking function. If it is known that the CPU clock will always be at least ten times faster than the incoming JTCK clock signal, then the JRTCK signal is not needed.

The two die inside the STR91xF (CPU die and Flash memory die) are internally daisy-chained on the JTAG bus, see *Figure 3 on page 22*. The CPU die has two JTAG Test Access Ports (TAPs), one for boundary scan functions and one for ARM CPU debug. The Flash memory die has one TAP for program/erase of non-volatile memory. Because these three TAPs are daisy-chained, only one TAP will converse on the JTAG bus at any given time while the other two TAPs are in BYPASS mode. The TAP positioning order within this JTAG chain is the boundary scan TAP first, followed by the ARM debug TAP, followed by the Flash TAP. All three TAP controllers are reset simultaneously by one of two methods:

- A chip-level global reset, caused only by a Power-On-Reset (POR) or a Low Voltage Detect (LVD).
- A reset command issued by the external JTAG test equipment. This can be the assertion of the JTAG JTRSTn input pin on the STR91xF or a JTAG reset command shifted into the STR91xF serially.

This means that chip-level system resets from watchdog time-out or the assertion of RESET_INn pin do not affect the operation of any JTAG TAP controller. Only global resets effect the TAPs.

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the host computer must have a static image of the code being executed for decompressing the ETM9 data. Because of this, self-modified code cannot be traced.

## 2.17 Ethernet MAC interface with DMA

STR91xF devices in 128-pin packages provide an IEEE-802.3-2002 compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry standard Medium Independent Interface (MII). The STR91xF requires an external Ethernet physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the STR91xF MII port using as many as 18 signals (see pins which have signal names MII_* in *Table 3*).

The MAC corresponds to the OSI Data Link layer and the PHY corresponds to the OSI Physical layer. The STR91xF MAC is responsible for:

- Data encapsulation, including frame assembly before transmission, and frame parsing/ error detection during and after reception.
- Media access control, including initiation of frame transmission and recover from transmission failure.

The STR91xF MAC includes the following features:

- Supports 10 and 100 Mbps rates
- Tagged MAC frame support (VLAN support)
- Half duplex (CSMA/CD) and full duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. Transmit FIFO depth is 4 words (32 bits each), and the receive FIFO is 16 words deep.

A 32-bit burst DMA channel residing on the AHB is dedicated to the Ethernet MAC for high-speed data transfers, side-stepping the CPU for minimal CPU impact during transfers. This DMA channel includes the following features:

- Direct SRAM to MAC transfers of transmit frames with the related status, by descriptor chain
- Direct MAC to SRAM transfers of receive frames with the related status, by descriptor chain
- Open and Closed descriptor chain management

## 2.18 USB 2.0 slave device interface with DMA

The STR91xF provides a USB slave controller that implements both the OSI Physical and Data Link layers for direct bus connection by an external USB host on pins USBDP and USBPN. The USB interface detects token packets, handles data transmission and reception, and processes handshake packets as required by the USB 2.0 standard.

The USB slave interface includes the following features:

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SRAM, handling of transmission requests, and interrupt generation. The CPU has access to the Message SRAM via the Message Handler using a set of 38 control registers.

The follow features are supported by the CAN interface:

- Bitrates up to 1 Mbps
- Disable Automatic Retransmission mode for Time Triggered CAN applications
- 32 Message Objects
- Each Message Object has its own Identifier Mask
- Programmable FIFO mode
- Programmable loopback mode for self-test operation

The CAN interface is not supported by DMA.

## 2.20 UART interfaces with DMA

The STR91xF supports three independent UART serial interfaces, designated UART0, UART1, and UART2. Each interface is very similar to the industry-standard 16C550 UART device. All three UART channels support IrDA encoding/decoding, requiring only an external LED transceiver to pins UARTx_RX and UARTx_Tx for communication. One UART channel (UART0) supports full modem control signals.

UART interfaces include the following features:

- Maximum baud rate of 1.5 Mbps
- Separate FIFOs for transmit and receive, each 16 deep, each FIFO can be disabled by firmware if desired
- Programmable FIFO trigger levels between 1/8 and 7/8
- Programmable baud rate generator based on CCU master clock, or CCU master clock divided by two
- Programmable serial data lengths of 5, 6, 7, or 8 bits with start bit and 1 or 2 stop bits
- Programmable selection of even, odd, or no-parity bit generation and detection
- False start-bit detection
- Line break generation and detection
- Support of IrDA SIR ENDEC functions for data rates of up to 115.2K bps
- IrDA bit duration selection of 3/16 or low-power (1.14 to 2.23 µsec)
- Channel UART0 supports modem control functions CTS, DCD, DSR, RTS, DTR, and RI

For your reference, only two standard 16550 UART features are not supported, 1.5 stop bits and independent receive clock.

### 2.20.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service channels UART0 and UART1 for fast and direct transfers between the UART bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that UART FIFOs are enabled.

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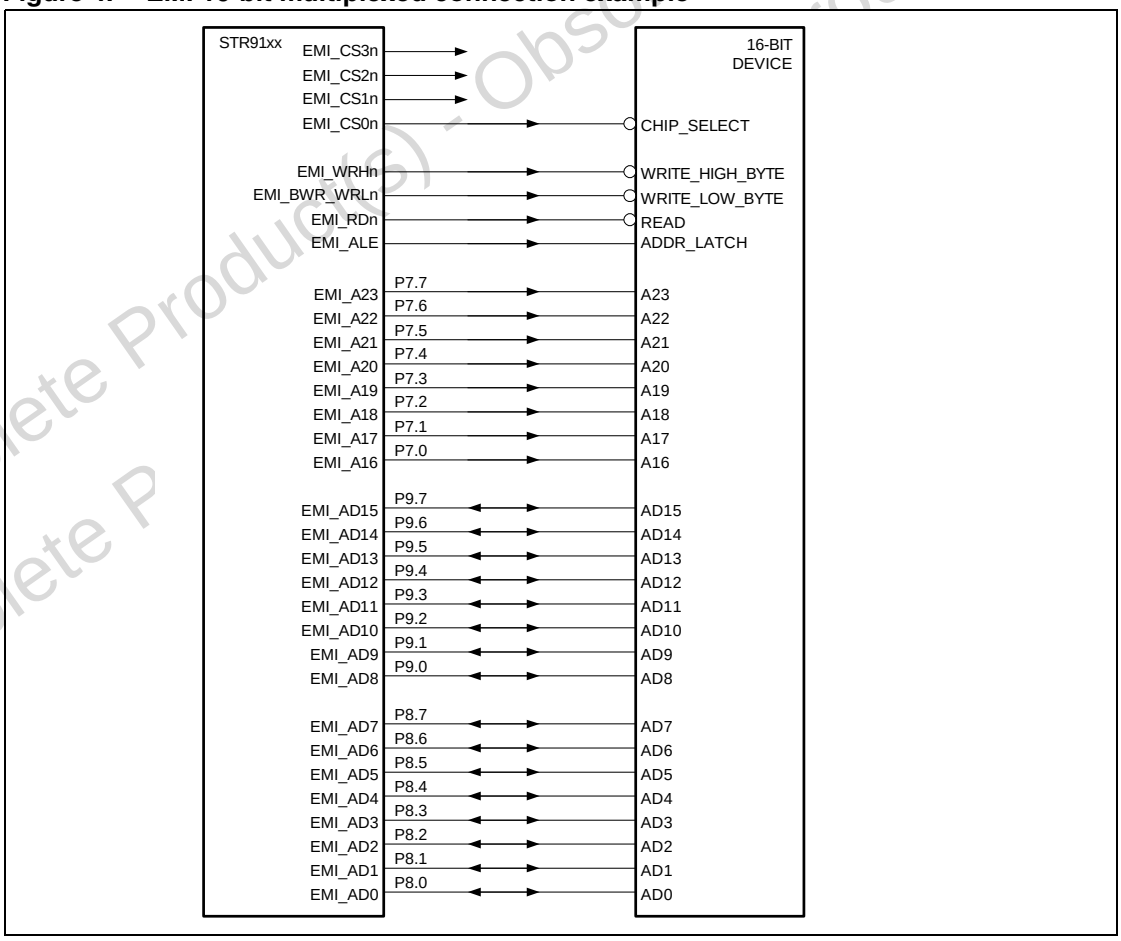
respectively. The output signal EMI_RDn is the read strobe for both the low and high data bytes.

- **8-bit multiplexed data mode**: This is a variant of the 16-bit multiplexed mode. Although this mode can provide 24 bits of address and 8 bits of data, it does require an external latch device on Port 8. However, this mode is most efficient when connecting devices that only require 8 bits of address on an 8-bit multiplexed address/data bus, and have simple read, write, and latch inputs as shown in *Figure 5*

  To use all 24 address bits, the following applies: 8 bits of lowest-order data and 8 bits of lowest-order address are multiplexed on port 8. On port 9, 8-bits of mid-order address are multiplexed with 8 bits of data, but these 8 data values are always at logic zero on this port during a write operation, and these 8 data bits are ignored during a read operation. An external latch device (such as a '373 latch) is needed to de-multiplex the mid-order 8 address bits that are generated on port 8. Port 7 outputs the 8 highest-order address signals directly (not multiplexed). The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signal on pin EMI_BWR_WRLn is the data write strobe, and the output on pin EMI_RDn is the data read strobe.
- **8-bit non-multiplexed data mode** (*Figure 6*): Eight bits of data are on port 8, while 16 bits of address are output on ports 7 and 9. The output signal on pin EMI_BWR_BWLn is the data write strobe and the output on pin EMI_RDn is the data read strobe.

**Figure 4. EMI 16-bit multiplexed connection example**

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# 5 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes ($2^{32}$) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

## 5.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

## 5.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xF Reference manual for the address of data locations within each individual peripheral.

## 5.3 SRAM

The SRAM is aliased at three separate address ranges as shown in *Figure 9*. When the CPU accesses SRAM starting at 0x0400.0000, the SRAM appears on the D-TCM. When CPU access starts at 0x4000.0000, SRAM appears in the buffered AHB range. Beginning at CPU address 0x5000.0000, SRAM is in non-buffered AHB range. The SRAM size must be specified by CPU intitialization firmware writing to a control register after any reset condition. Default SRAM size is 32K bytes, with option to set to 64K bytes on STR91xFx32 devices, and to 96K bytes on STR91xFx44 devices.

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When other AHB bus masters (such as a DMA controller) write to SRAM, their access is never buffered. Only the CPU can make use of buffered AHB writes.

## 5.4 Two independent Flash memories

The STR91xF has two independent Flash memories, the larger primary Flash and the small secondary Flash. It is possible for the CPU to erase/write to one of these Flash memories while simultaneously reading from the other.

One or the other of these two Flash memories may reside at the “boot” address position of 0x0000.0000 at power-up or at reset as shown in *Figure 9*. The default configuration is that the first sector of primary Flash memory is enabled and residing at the boot position, and the secondary Flash memory is disabled. This default condition may be optionally changed as described below.

### 5.4.1 Default configuration

When the primary Flash resides at boot position, typical CPU initialization firmware would set the start address and size of the main Flash memory, and go on to enable the secondary Flash, define it’s start address and size. Most commonly, firmware would place the secondary Flash start address at the location just after the end of the primary Flash memory. In this case, the primary Flash is used for code storage, and the smaller secondary flash can be used for data storage (EEPROM emulation).

### 5.4.2 Optional configuration

Using the STR91xF device configuration software tool, or IDE from 3rd party, one can specify that the smaller secondary Flash memory is at the boot location at reset and the primary Flash is disabled. The selection of which Flash memory is at the boot location is programmed in a non-volatile Flash-based configuration bit during JTAG ISP. The boot selection choice will remain as the default until the bit is erased and re-written by the JTAG interface. The CPU cannot change this choice for boot Flash, only the JTAG interface has access.

In this case where the secondary Flash defaults to the boot location upon reset, CPU firmware would typically initialize the Flash memories the following way. The secondary Flash start address and size is specified, then the primary Flash is enabled and its start address and size is specified. The primary Flash start address would typically be located just after the final address location of the secondary Flash. This configuration is particularly well-suited for In-Application-Programming (IAP). The CPU would boot from the secondary Flash memory, initialize the system, then check the contents of the primary Flash memory (by checksum or other means). If the contents of primary Flash is OK, then CPU execution continues from either Flash memory. If the main Flash contents are incorrect, the CPU, while executing code from the secondary Flash, can download new data from any STR91xF communication channel and program into primary Flash memory. Application code then starts after the new contents of primary Flash are verified.

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## 6.4 DC electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 7. DC Electrical Characteristics**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | Input High Level | General inputs | 2.0 | | (1) | V |
| | | RESET and TCK inputs | $0.8V_{DDQ}$ | | | |
| $V_{IL}$ | Input Low Level | General inputs | | | 0.8 | |
| | | RESET and TCK inputs | | | $0.2V_{DDQ}$ | |
| $V_{HYS}$ | Input Hysteresis Schmitt Trigger | General inputs | 0.4 | | | V |
| $V_{OH}$ | Output High Level High current pins | I/O ports 3 and 6: Push-Pull, $I_{OH}$ = 8mA | $V_{DDQ}$-0.7 | | | V |
| | Output High Level Standard current pins | I/O ports 0,1,2,4,5,7,8,9: Push-Pull, $I_{OH}$ = 4mA | $V_{DDQ}$-0.7 | | | |
| $V_{OL}$ | Output Low Level High current pins | I/O ports 3 and 6: Push-Pull, $I_{OL}$ = 8mA | | | 0.4 | V |
| | Output Low Level Standard current pins | I/O ports 0,1,2,4,5,7,8,9: Push-Pull, $I_{OL}$ = 4mA | | | 0.4 | |

*Notes: 1 Input pins are 5V tolerant, max input voltage is 5.5V*

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## 6.5 AC electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 8. AC electrical characteristics**

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $I_{DDRUN}$ | Run Mode Current | All peripherals on | CPU_CLK = 96MHz [1] [5] | | 1.7 | 2.3 | mA/ MHz |
| | | All peripherals off | | | 1.3 | 1.6 | |
| $I_{IDLE}$ | Idle Mode Current | All peripherals on [2] [5] | | | 1.14 | 1.7 | mA/ MHz |
| | | All peripherals off [3] [5] | | | 0.45 | 0.75 | mA/ MHz |
| $I_{SLEEP}$ | Sleep Mode Current | LVD On [4] [5] | | | 55 | 825 | µA |
| | | LVD Off [4] [5] | | | 50 | 820 | µA |
| $I_{RTC\_STBY}$ | RTC Standby Current | Measured on VBATT pin | | | 0.3 | 0.9 | µA |
| $I_{SRAM\_STBY}$ | SRAM Standby Current | Measured on VBATT pin | | | 5 | 85 | µA |

*Notes: 1 ARM core and peripherals active with all clocks on. Power can be conserved by turning off clocks to peripherals which are not required.*

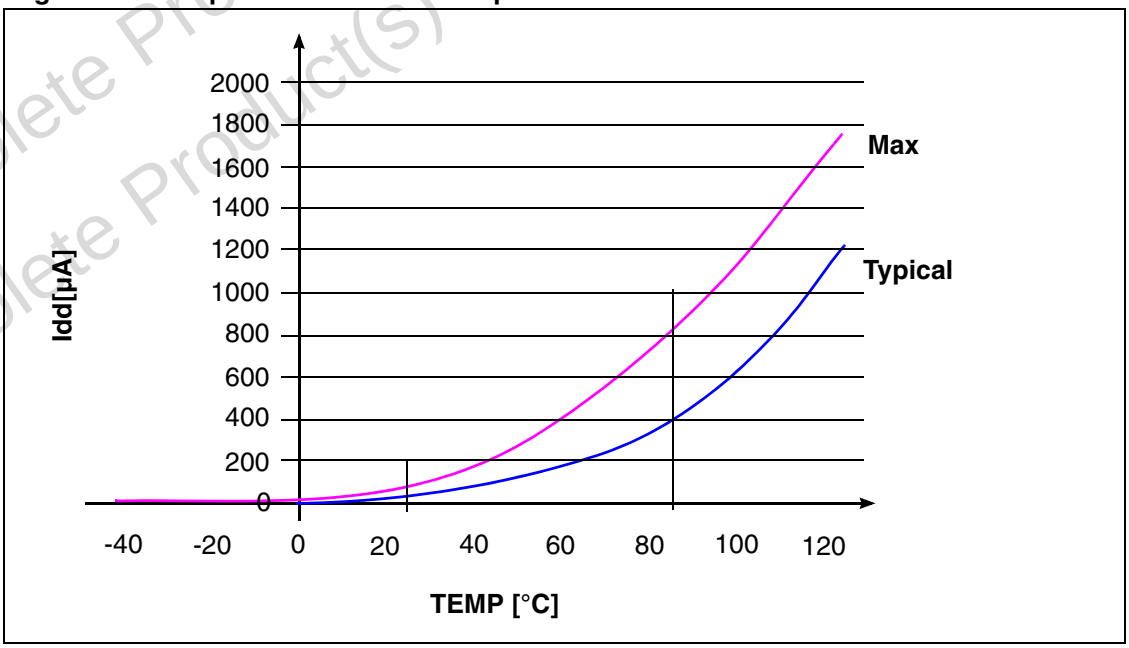
*2 ARM core stopped and all peripheral clocks active.*

*3 ARM core stopped and all peripheral clocks stopped.*

*4 ARM core and all peripheral clocks stopped (with exception of RTC).*

*5 Current measured on the $V_{DD}$ pins. $V_{DDQ}$ current is not included.*

**Figure 10. Sleep Mode current vs temperature**




Obsolete Product(s) - Obsolete Product(s)

## 6.7 Main oscillator electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 11. Main oscillator electrical characteristics**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{STUP(OSC)}$ | Oscillator Start-up Time | Stable $V_{DDQ}$ | | | 3 | mS |

## 6.8 RTC oscillator electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 12. RTC oscillator electrical characteristics**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $g_{M(RTC)}$ | Oscillator Start _voltage | | LVD [1)] | | | V |
| $t_{STUP(RTC)}$ | Oscillator Start-up Time | Stable $V_{DDQ}$ | | | 1 | S |

*Notes: 1 Min oscillator start voltage is the same as low voltage detect level (2.4V or 2.7V) for VDDQ*

**Table 13. RTC crystal electrical characteristics**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_O$ | Resonant frequency | | | 32.768 | | kHz |
| $R_S$ | Series resistance | | | | 40 | kΩ |
| $C_L$ | Load capacitance | | | 8 | | pF |

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Obsolete Product(s) - Obsolete Product(s)

## 6.9 PLL electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 14. PLL Electrical Characteristics**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{PLL}$ | PLL Output Clock | | 6.25 | | 96 | MHz |
| $f_{OSC}$ | Clock Input | | 4 | | 25 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 300 | 1500 | µs |
| $\Delta t_{JITTER}$ | PLL Jitter (peak to peak) | | | 0.1 | 0.2 | ns |

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

## 6.10 Flash memory characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 15. Flash memory program/erase characteristics**

| Parameter | | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Typ[2] | Typ after 100K W/E cycles[2] | Max | |
| Bank erase | Primary Bank (512 Kbytes)[1] | | 8 | 9 | 11.5 | s |
| | Primary Bank (256 Kbytes)[1] | | 4 | 4.5 | 6 | s |
| | Secondary Bank (32 Kbytes) | | 700 | 750 | 950 | ms |
| Sector erase | Of Primary Bank (64 Kbytes) | | 1300 | 1400 | 1800 | ms |
| | Of Secondary Bank (8 Kbytes) | | 300 | 320 | 450 | ms |
| Bank program | Primary Bank (512 Kbytes)[1] | | 3700 | 4700 | 5100 | ms |
| | Primary Bank (256 Kbytes)[1] | | 1900 | 2000 | 2550 | ms |
| | Secondary Bank (32 Kbytes) | | 250 | 260 | 320 | ms |
| Sector program | Of Primary Bank (64 Kbytes) | | 500 | 520 | 640 | ms |
| | Of Secondary Bank (8 Kbytes) | | 60 | 62 | 80 | ms |
| Word program | | | 8 | 9 | 11 | µs |
| Sector erase timeout | | | | | | µs |

*Notes: 1 STR91xFx44 devices have 512 Kbytes primary Flash, STR91xFx32 devices have 256 Kbytes primary Flash*

2 $V_{DD}$ = 1.8V, $V_{DDQ}$ = 3.3V, $T_A$ = 25°C.

3 Flash read access for synchronous addresses is 96 MHz maximum.

4 Flash read access for asynchronous accesses requires 2 wait states when FMI clock is above 66 MHz. See STR91xF Flash Programming Manual for more information.

**Table 16. Flash memory endurance**

| Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Program/erase cycles | Per word | 100K | | | cycles |
| Data retention | | 20 | | | years |

Obsolete Product(s) - Obsolete Product(s)

## 6.14 Communication interface electrical characteristics

### 6.14.1 10/100 Ethernet MAC electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

#### Ethernet MII Interface Timings

**Figure 16. MII_RX_CLK and MII_TX_CLK timing diagram**

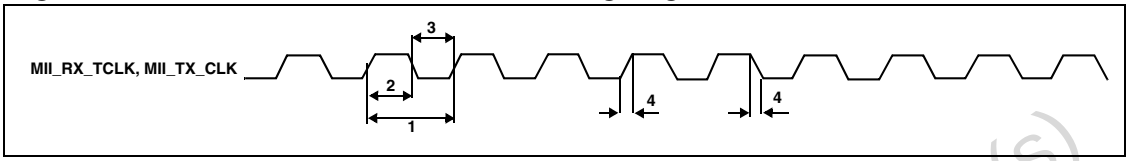



**Table 24. MII_RX_CLK and MII_TX_CLK timing table**

| Symbol | Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | Cycle time | $t_c$(CLK) | 40 | | ns |
| 2 | Pulse duration HIGH | $t_{HIGH}$(CLK) | 40% | 60% | |
| 3 | Pulse duration LOW | $t_{LOW}$(CLK) | 40% | 60% | |
| 4 | Transition time | $t_t$(CLK) | | 1 | ns |

**Figure 17. MDC timing diagram**

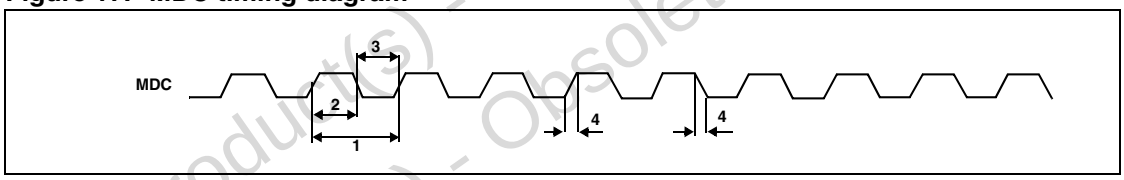
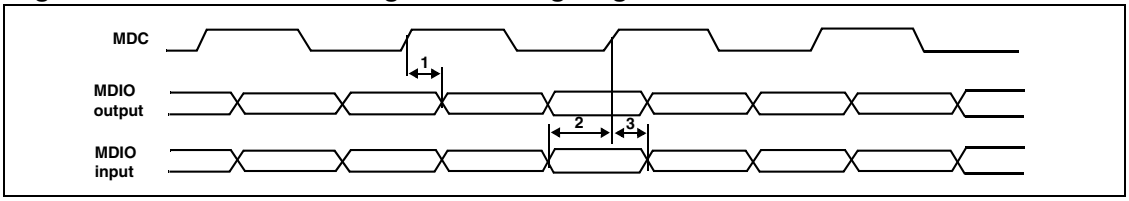



**Table 25. MDC timing table**

| Symbol | Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | Cycle time | $t_c$(MDC) | 266 | | ns |
| 2 | Pulse duration HIGH | $t_{HIGH}$(MDC) | 40% | 60% | |
| 3 | Pulse duration LOW | $t_{LOW}$(MDC) | 40% | 60% | |
| 4 | Transition time | $t_t$(MDC) | | 1 | ns |

#### Ethernet MII management timings

**Figure 18. Ethernet MII management timing diagram**




Obsolete Product(s) - Obsolete Product(s)

**Table 26. Ethernet MII management timing table**

| Symbol | Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | MDIO delay from rising edge of MDC | $t_c$(MDIO) | | 2.83 | ns |
| 2 | MDIO setup time to rising edge of MDC | $T_{su}$ (MDIO) | 2.70 | | ns |
| 3 | MDIO hold time from rising edge of MDC | $T_h$ (MDIO) | -2.03 | | ns |

## Ethernet MII transmit timings

**Figure 19. Ethernet MII transmit timing diagram**

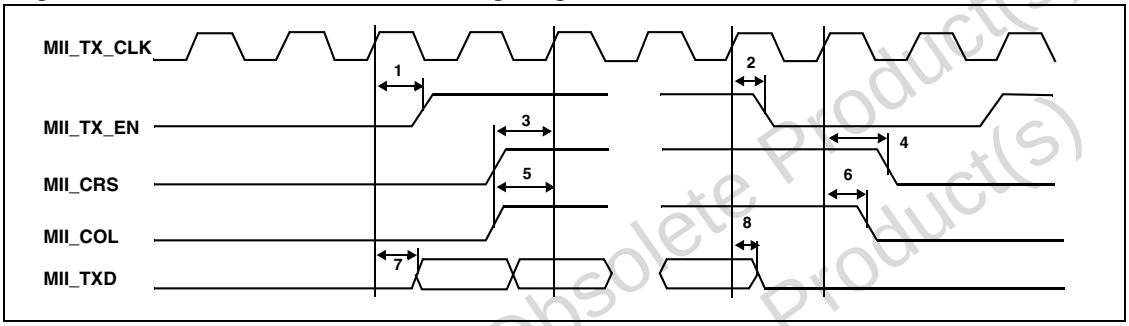



**Table 27. Ethernet MII transmit timing table**

| Symbol | Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | MII_TX_CLK high to MII_TX_EN valid | $t_{VAL}$(MII_TX_EN) | | 4.20 | ns |
| 2 | MII_TX_CLK high to MII_TX_EN invalid | $T_{inval}$(MII_TX_EN) | | 4.86 | ns |
| 3 | MII_CRS valid to MII_TX_CLK high | $T_{su}$(MII_CRS) | 0.61 | | ns |
| 4 | MII_TX_CLK high to MII_CRS invalid | $T_h$(MII_CRS) | 0.00 | | ns |
| 5 | MII_COL valid to MII_TX_CLK high | $T_{su}$(MII_COL) | 0.81 | | ns |
| 6 | MII_TX_CLK high to MII_COL invalid | $T_h$(MII_COL) | 0.00 | | ns |
| 7 | MII_TX_CLK high to MII_TXD valid | $t_{VAL}$(MII_TXD) | | 5.02 | ns |
| 8 | MII_TXCLK high to MII_TXD invalid | $T_{inval}$(MII_TXD | | 5.02 | ns |

Obsolete Product(s) - Obsolete Product(s)

### 6.14.4 $I^2C$ electrical characteristics

$V_{DDQ}$ = 2.7 - 3.6V, $V_{DD}$ = 1.65 - 2V, $T_A$ = -40 / 85 °C unless otherwise specified.

**Table 28. $I^2C$ Electrical Characteristics**

| Symbol | Parameter | Standard $I^2C$ | | Fast $I^2C$ | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | 1.3 | | ms |
| $t_{HD:STA}$ | Hold time START condition. After this period, the first clock pulse is generated | 4.0 | | 0.6 | | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | | 1.3 | | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | | 0.6 | | µs |
| $t_{SU:STA}$ | Set-up time for a repeated START condition | 4.7 | | 0.6 | | µs |
| $t_{HD:DAT}$ | Data hold time | 0 | | 0 | | ns |
| $t_{SU:DAT}$ | Data set-up time | 250 | | 100 | | ns |
| $t_R$ | Rise time of both SDA and SCL signals | | 1000 | $20+0.1C_b$ | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | | 300 | $20+0.1C_b$ | 300 | ns |
| $t_{SU:STO}$ | Set-up time for STOP condition | 4.0 | | 0.6 | | µs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

*Notes: 1 The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL*

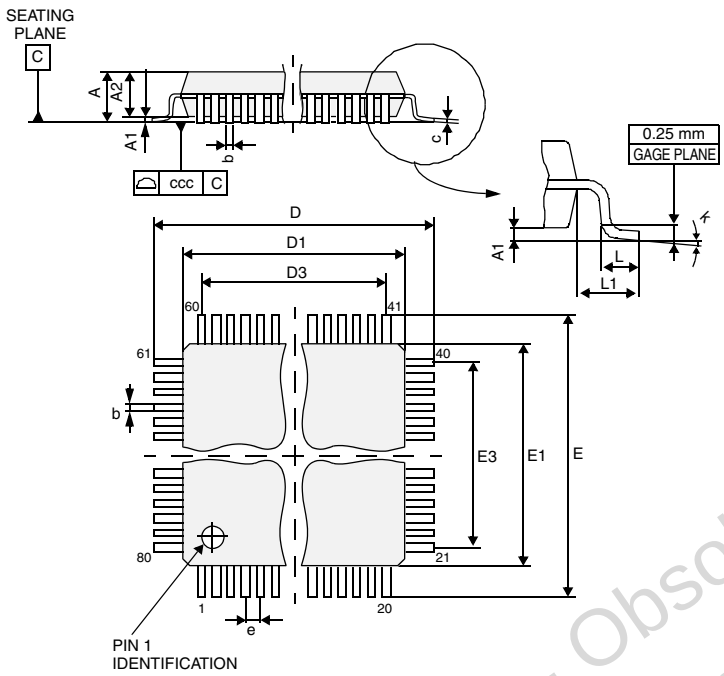
*2 The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal*

*3 $C_b$ = total capacitance of one bus line in pF*

Obsolete Product(s) Obsolete Product(s) Obsolete Product(s)

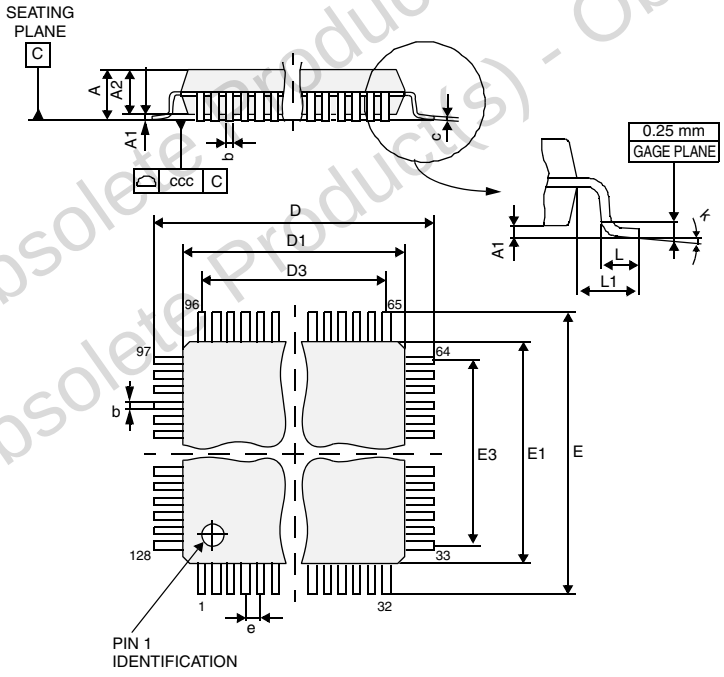
# 7 Package mechanical data

**Figure 25. 80-Pin Low Profile Quad Flat Package**




| Dim. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 14.00 | | | 0.551 | |
| D1 | | 12.00 | | | 0.472 | |
| D2 | | 9.50 | | | 0.374 | |
| E | | 14.00 | | | 0.551 | |
| E1 | | 12.00 | | | 0.472 | |
| E2 | | 9.50 | | | 0.374 | |
| e | | 0.50 | | | 0.020 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| k | 0d | | 7d | 0d | | 7d |
| ddd | | | 0.08 | | | 0.003 |
| | Number of Pins | | | | | |
| N | 80 | | | | | |

**128-Pin Low Profile Quad Flat Package**




| Dim. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | 15.80 | 16.00 | 16.20 | 0.622 | 0.630 | 0.638 |
| D1 | 13.80 | 14.00 | 14.20 | 0.543 | 0.551 | 0.559 |
| D3 | | 12.40 | | | 0.488 | |
| E | 15.80 | 16.00 | 16.20 | 0.622 | 0.630 | 0.638 |
| E1 | 13.80 | 14.00 | 14.20 | 0.543 | 0.551 | 0.559 |
| E3 | | 12.40 | | | 0.488 | |
| e | | 0.40 | | | 0.016 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| k | 0d | 3.5d | 7d | 0d | 3.5d | 7d |
| ccc | | | 0.08 | | | 0.003 |
| | Number of Pins | | | | | |
| N | 128 | | | | | |

Obsolete Product(s) - Obsolete Product(s) - Obsolete Product(s)

## 7.1 Thermal characteristics

The average chip-junction temperature, $T_J$ must never exceed 125° C.

The average chip-junction temperature, $T_J$, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) (1)$$

Where:

- $T_A$ is the Ambient Temperature in °C,
- $\Theta_{JA}$ is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- $P_D$ is the sum of $P_{INT}$ and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- $P_{INT}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories. The worst case $P_{INT}$ of the STR91xF is 500mW ($I_{DD} \times V_{DD}$, or 250mA x 2.0V).

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 (3)$$

where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ may be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

**Table 30. Thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal Resistance Junction-Ambient** LQFP 80 - 12 x 12 mm / 0.5 mm pitch | 41.5 | °C/W |
| $\Theta_{JA}$ | **Thermal Resistance Junction-Ambient** LQFP128 - 14 x 14 mm / 0.4 mm pitch | 38 | °C/W |

Obsolete Product(s) - Obsolete Product(s)

# 9 Revision history

| Date | Revision | Changes |
|---|---|---|
| 12-Apr-2006 | 1 | Initial release |
| 28-June-2006 | 2 | Added LFBGA144 package<br>Updated electrical characteristics section |
| 04-Sep-2006 | 3 | Changed number of GPIOs in 80 pin packge to 40<br>Changed EMI_RDYn pin name to EMI_WAITn<br>Added RTC clock to description of JRTCK in *Table 3*<br>UART max baud rate changed to 1.5 Mbps in *Section 2.20 on page 26*<br>Modified *Figure 2: Clock control on page 15* |
| 01-Feb-2007 | 4 | Removed LFBGA144 package, (transferred to separate STR91xFA datasheet). |

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)