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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, I²C, Microwire, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	40
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911fm42x6

1 Introduction

STR91xF is a series of ARM-powered microcontrollers which combines a 16/32-bit ARM966E-S RISC processor core, dual-bank Flash memory, large SRAM for data or code, and a rich peripheral set to form an ideal embedded controller for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment. The ARM966E-S core can perform single-cycle DSP instructions, good for speech processing, audio algorithms, and low-end imaging.

This datasheet provides STR91xF ordering information, functional overview, mechanical information, and electrical device characteristics.

For complete information on STR91xF memory, registers, and peripherals, please refer to the STR91xF Reference Manual.

For information on programming the STR91xF Flash memory please refer to the STR9 Flash Programming Reference Manual

For information on the ARM966E-S core, please refer to the ARM966E-S Rev. 2 Technical Reference Manual.

Table 1. Device summary

Features	STR910F		STR911F		STR912F	
	M32X6	W32X6	M42X6	M44X6	W42X6	W44X6
Flash Kbytes	256+32		256+32	512+32	256+32	512+32
RAM - Kbytes	64		96		96	
Peripheral functions	CAN, 40 I/Os	CAN, EMI, 80 I/Os	USB, CAN, 40 I/Os		Ethernet, USB, CAN, EMI, 80 I/Os	
Packages	LQFP80	LQFP128	LQFP80		LQFP128	

2.10 Clock control unit (CCU)

The CCU generates a master clock of frequency f_{MSTR}. From this master clock the CCU also generates individually scaled and gated clock sources to each of the following functional blocks within the STR91xF.

- CPU, f_{CPUCLK}
- Advanced High-performance Bus (AHB), f_{HCLK}
- Advanced Peripheral Bus (APB), f_{PCLK}
- Flash Memory Interface (FMI), f_{FMICLK}
- External Memory Interface (EMI), f_{BCLK}
- UART Baud Rate Generators, f_{BAUD}
- USB, f_{USB}

2.10.1 Master clock sources

The master clock in the CCU (f_{MSTR}) is derived from one of three clock input sources. Under firmware control, the CPU can switch between the three CCU inputs without introducing any glitches on the master clock output. Inputs to the CCU are:

- Main Oscillator (f_{OSC}). The source for the main oscillator input is a 4 to 25 MHz external crystal connected to STR91xF pins X1_CPU and X2_CPU, or an external oscillator device connected to pin X1_CPU.
- PLL (f_{PLL}). The PLL takes the 4 to 25 MHz oscillator clock as input and generates a master clock output up to 96 MHz (programmable). By default, at power-up the master clock is sourced from the main oscillator until the PLL is ready (locked) and then the CPU may switch to the PLL source under firmware control. The CPU can switch back to the main oscillator source at any time and turn off the PLL for low-power operation. The PLL is always turned off in Sleep mode.
- RTC (f_{RTC}). A 32.768 kHz external crystal can be connected to pins X1_RTC and X2_RTC, or an external oscillator connected to pin X1_RTC to constantly run the real-time clock unit. This 32.768 kHz clock source can also be used as an input to the CCU to run the CPU in slow clock mode for reduced power.

As an option, there are a number of peripherals that do not have to receive a clock sourced from the CCU. The USB interface can receive an external clock on pin P2.7, TIM timers TIM0/TIM1 can receive an external clock on pin P2.4, and timers TIM2/TIM3 on pin P2.5.

- Some resets (external reset pin, low-voltage, power-up, JTAG debug command)
- RTC alarm
- Input from wake-up unit

2.12 Voltage supplies

The STR91xF requires two separate operating voltage supplies. The CPU and memories operate from a 1.65V to 2.0V on the VDD pins, and the I/O ring operates at 2.7V to 3.6V on the VDDQ pins.

2.12.1 Independent A/D converter supply and reference voltage

The ADC unit on 128-pin packages has an isolated analog voltage supply input at pin AVDD to accept a very clean voltage source, independent of the digital voltage supplies. The analog voltage supply range on pin AVDD is the same range as the digital voltage supply on pin VDDQ. Additionally, an isolated analog supply ground connection is provided on pin AVSS only on 128-pin packages for further ADC supply isolation. On 80-pin packages, the analog voltage supply is shared with the ADC reference voltage pin (as described next), and the analog ground is shared with the digital ground at a single point in the STR91xF device on pin AVSS_VSSQ.

A separate external analog reference voltage input for the ADC unit is available on 128-pin packages at the AVREF pin for better accuracy on low voltage inputs, and the voltage on AVREF can range from 1.0V to V_{DDQ}. For 80-pin packages, the ADC reference voltage is tied internally to the ADC unit supply voltage at pin AVCC_AVREF, meaning the ADC reference voltage is fixed to the ADC unit supply voltage.

2.12.2 Battery supply

An optional stand-by voltage from a battery or other source may be connected to pin VBATT to retain the contents of SRAM in the event of a loss of the V_{DD} supply. The SRAM will automatically switch its supply from the internal V_{DD} source to the VBATT pin when the voltage of V_{DD} drops below that of VBATT.

The VBATT pin also supplies power to the RTC unit, allowing the RTC to function even when the main digital supplies (V_{DD} and V_{DDQ}) are switched off. By configuring the RTC register, it is possible to select whether or not to power from VBATT only the RTC unit, or power the RTC unit and the SRAM when the STR91xF device is powered off.

2.21 I²C interfaces with DMA

The STR91xF supports two independent I2C serial interfaces, designated I2C0, and I2C1. Each interface allows direct connection to an I2C bus as either a bus master or bus slave device (firmware configurable). I2C is a two-wire communication channel, having a bi-directional data signal and a single-directional clock signal based on open-drain line drivers, requiring external pull-up resistors.

Byte-wide data is transferred between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I2C supports collision detection and arbitration. More than one Slave device may be present on the bus, each having a unique address. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device that is addressed is considered a Slave. Automatic clock synchronization allows I2C devices with different bit rates to communicate on the same physical bus. A single device can play the role of Master or Slave, or a single device can be a Slave only. A Master or Slave device has the ability to suspend data transfers if the device needs more time to transmit or receive data.

Each I2C interface on the STR91xF has the following features:

- Programmable clock supports various rates up to I2C Standard rate (100 KHz) or Fast rate (400 KHz).
- Serial I/O Engine (SIOE) takes care of serial/parallel conversion; bus arbitration; clock generation and synchronization; and handshaking
- Multi-master capability
- 7-bit or 10-bit addressing

2.21.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service each I2C channel for fast and direct transfers between the I2C bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive.

2.22 SSP interfaces (SPI, SSI, and Microwire) with DMA

The STR91xF supports two independent Synchronous Serial Port (SSP) interfaces, designated SSP0, and SSP1. Primary use of each interface is for supporting the industry standard Serial Peripheral Interface (SPI) protocol, but also supporting the similar Synchronous Serial Interface (SSI) and Microwire communication protocols.

SPI is a three or four wire synchronous serial communication channel, capable of full-duplex operation. In three-wire configuration, there is a clock signal, and two data signals (one data signal from Master to Slave, the other from Slave to Master). In four-wire configuration, an additional Slave Select signal is output from Master and received by Slave.

The SPI clock signal is a gated clock generated from the Master and regulates the flow of data bits. The Master may transmit at a variety of baud rates, up to 24 MHz

In multi-Slave operation, no more than one Slave device can transmit data at any given time. Slave selection is accomplished when a Slave's "Slave Select" input is permanently grounded or asserted active-low by a Master device. Slave devices that are not selected do not interfere with SPI activities. Slave devices ignore the clock signals and keep their data output pins in

Pkg		Pin Name	Signal Type	Default Pin Function	Default Input Function	Alternate functions			
LQFP80	LQFP128					Alternate Input 1	Alternate Output 1	Alternate Output 2	Alternate Output 3
43	68	P3.7	I/O	GPIO_3.7, GP Input, HiZ	EXINT7, External Intr	SSP1_NSS, SSP slv select in	GPIO_3.7, GP Output	SSP1_NSS, SSP mstr sel out	TIM1_OCMP1, *Out comp/PWM*
4	3	P4.0	I/O	GPIO_4.0, GP Input, HiZ	ADC0, ADC input chnl	TIM0_ICAP1, Input Capture	GPIO_4.0, GP Output	TIM0_OCMP1, *Out comp/PWM*	ETM_PCK0, *ETM Packet*
3	2	P4.1	I/O	GPIO_4.1, GP Input, HiZ	ADC1, ADC input chnl	TIM0_ICAP2, Input Capture	GPIO_4.1, GP Output	TIM0_OCMP2, *Out comp*	ETM_PCK1, *ETM Packet*
2	1	P4.2	I/O	GPIO_4.2, GP Input, HiZ	ADC2, ADC input chnl	TIM1_ICAP1, Input Capture	GPIO_4.2, GP Output	TIM1_OCMP1, *Out comp/PWM*	ETM_PCK2, *ETM Packet*
1	128	P4.3	I/O	GPIO_4.3, GP Input, HiZ	ADC3, ADC input chnl	TIM1_ICAP2, Input Capture	GPIO_4.3, GP Output	TIM1_OCMP2, *Out comp*	ETM_PCK3, *ETM Packet*
80	127	P4.4	I/O	GPIO_4.4, GP Input, HiZ	ADC4, ADC input chnl	TIM2_ICAP1, Input Capture	GPIO_4.4, GP Output	TIM2_OCMP1, *Out comp/PWM*	ETM_PSTAT0, ETM pipe status
79	126	P4.5	I/O	GPIO_4.5, GP Input, HiZ	ADC5, ADC input chnl	TIM2_ICAP2, Input Capture	GPIO_4.5, GP Output	TIM2_OCMP2, *Out comp*	ETM_PSTAT1, ETM pipe status
78	125	P4.6	I/O	GPIO_4.6, GP Input, HiZ	ADC6, ADC input chnl	TIM3_ICAP1, Input Capture	GPIO_4.6, GP Output	TIM3_OCMP1, *Out comp/PWM*	ETM_PSTAT2, ETM pipe status
77	124	P4.7	I/O	GPIO_4.7, GP Input, HiZ	ADC7, ADC input chnl	TIM3_ICAP2, Input Capture	GPIO_4.7, GP Output	TIM3_OCMP2, *Out comp*	ETM_TRSYNC, ETM trace sync
9	12	P5.0	I/0	GPIO_5.0, GP Input, HiZ	EXINT8, External Intr	CAN_RX, CAN rcv data	GPIO_5.0, GP Output	ETM_TRCLK, ETM trace clock	UART0_TX, UART xmit data
12	18	P5.1	I/0	GPIO_5.1, GP Input, HiZ	EXINT9, External Intr	UART0_RxD, UART rcv data	GPIO_5.1, GP Output	CAN_TX, CAN Tx data	UART2_TX, UART xmit data
17	25	PHYCLK _P5.2	I/O	GPIO_5.2, GP Input, HiZ	EXINT10, External Intr	UART2_RxD, UART rcv data	GPIO_5.2, GP Output	MII_PHYCLK, *25Mhz to PHY*	TIM3_OCMP1, *Out comp/PWM*
18	27	P5.3	I/O	GPIO_5.3, GP Input, HiZ	EXINT11, External Intr	ETM_EXTRIG, ETM ext. trigger	GPIO_5.3, GP Output	MII_TX_EN, MAC xmit enbl	TIM2_OCMP1, *Out comp/PWM*
44	70	P5.4	I/O	GPIO_5.4, GP Input, HiZ	EXINT12, External Intr	SSP0_SCLK, SSP slv clk in	GPIO_5.4, GP Output	SSP0_SCLK, SSP mstr clk out	EMI_CS0n, EMI Chip Select
47	77	P5.5	I/O	GPIO_5.5, GP Input, HiZ	EXINT13, External Intr	SSP0_MOSI, SSP slv dat in	GPIO_5.5, GP Output	SSP0_MOSI, SSP mstr dat out	EMI_CS1n, EMI Chip Select
48	79	P5.6	I/O	GPIO_5.6, GP Input, HiZ	EXINT14, External Intr	SSP0_MISO, SSP mstr dat in	GPIO_5.6, GP Output	SSP0_MISO, SSP slv data out	EMI_CS2n, EMI Chip Select
49	80	P5.7	I/O	GPIO_5.7, GP Input, HiZ	EXINT15, External Intr	SSP0_NSS, SSP slv select in	GPIO_5.7, GP Output	SSP0_NSS, SSP mstr sel out	EMI_CS3n, EMI Chip Select
19	29	P6.0	I/O	GPIO_6.0, GP Input, HiZ	EXINT16, External Intr	TIM0_ICAP1, Input Capture	GPIO_6.0, GP Output	TIM0_OCMP1, *Out comp/PWM*	MC_UH, IMC phase U hi
20	31	P6.1	I/O	GPIO_6.1, GP Input, HiZ	EXINT17, External Intr	TIM0_ICAP2, Input Capture	GPIO_6.1, GP Output	TIM0_OCMP2, *Out comp*	MC_UL, IMC phase U lo
13	19	P6.2	I/O	GPIO_6.2, GP Input, HiZ	EXINT18, External Intr	TIM1_ICAP1, Input Capture	GPIO_6.2, GP Output	TIM1_OCMP1, *Out comp/PWM*	MC_VH, IMC phase V hi
14	20	P6.3	I/O	GPIO_6.3, GP Input, HiZ	EXINT19, External Intr	TIM1_ICAP2, Input Capture	GPIO_6.3, GP Output	TIM1_OCMP2, *Out comp*	MC_VL, IMC phase V lo
52	83	P6.4	I/O	GPIO_6.4, GP Input, HiZ	EXINT20, External Intr	TIM2_ICAP1, Input Capture	GPIO_6.4, GP Output	TIM2_OCMP1, *Out comp/PWM*	MC_WH, IMC phase W hi
53	84	P6.5	I/O	GPIO_6.5, GP Input, HiZ	EXINT21, External Intr	TIM2_ICAP2, Input Capture	GPIO_6.5, GP Output	TIM2_OCMP2, *Out comp*	MC_WL, IMC phase W lo
57	92	P6.6	I/O	GPIO_6.6, GP Input, HiZ	EXINT22_TRIG, Ext Intr & Tach	UART0_RxD, UART rcv data	GPIO_6.6, GP Output	TIM3_OCMP1, *Out comp/PWM*	ETM_TRCLK, ETM trace clock
58	93	P6.7	I/O	GPIO_6.7, GP Input, HiZ	EXINT23_STOP, Ext Intr & Estop	ETM_EXTRIG, ETM ext. trigger	GPIO_6.7, GP Output	TIM3_OCMP2, *Out comp*	UART0_TX, UART xmit data

Pkg		Pin Name	Signal Type	Default Pin Function	Default Input Function	Alternate functions			
LQFP80	LQFP128					Alternate Input 1	Alternate Output 1	Alternate Output 2	Alternate Output 3
-	21	EMI_BWR_WRLn (used as EMI_LBn in future rev.)	O	EMI byte write strobe (8 bit mode) or low byte write strobe (16 bit mode)	N/A				
-	22	EMI_WRHn (used as EMI_UBn in future rev.)	O	EMI high byte write strobe (16-bit mode)	N/A				
-	74	EMI_ALE	O	EMI address latch enable (mux mode)	N/A				
-	75	EMI_RDn	O	EMI read strobe	N/A				
-	-	EMI_BAAn	O	TBD	N/A				
-	-	EMI_WAITn	I	TBD	N/A				
-	-	EMI_BCLK	O	TBD	N/A				
-	-	EMI_WEn	O	Reserved for future use	N/A				
-	91	TAMPER_IN	I	Tamper detection input	N/A				
-	94	MII_MDIO	I/O	MAC/PHY management data line	N/A				
59	95	USBDN	I/O	USB data (-) bus connect	N/A				
60	96	USBDP	I/O	USB data (+) bus connect	N/A				
56	89	RESET_INn	I	External reset input	N/A				
62	100	RESET_OUTn	O	Global or System reset output	N/A				
65	104	X1_CPU	I	CPU oscillator or crystal input	N/A				
64	103	X2_CPU	O	CPU crystal connection	N/A				
27	42	X1_RTC	I	RTC oscillator or crystal input (32.768 kHz)	N/A				
26	41	X2_RTC	O	RTC crystal connection	N/A				
61	97	JRTCK	O	JTAG return clock or RTC clock	N/A				
67	107	JTRSTn	I	JTAG TAP controller reset	N/A				
68	108	JTCK	I	JTAG clock	N/A				
69	111	JTMS	I	JTAG mode select	N/A				
72	115	JTDI	I	JTAG data in	N/A				
73	117	JTDO	O	JTAG data out	N/A				
-	122	AVDD	V	ADC analog voltage source, 2.7V - 3.6V	N/A				
-	4	AVSS	G	ADC analog ground	N/A				
5	-	AVSS_VSSQ	G	Common ground point for digital I/O & analog ADC	N/A				

When other AHB bus masters (such as a DMA controller) write to SRAM, their access is never buffered. Only the CPU can make use of buffered AHB writes.

5.4 Two independent Flash memories

The STR91xF has two independent Flash memories, the larger primary Flash and the small secondary Flash. It is possible for the CPU to erase/write to one of these Flash memories while simultaneously reading from the other.

One or the other of these two Flash memories may reside at the “boot” address position of 0x0000.0000 at power-up or at reset as shown in *Figure 9*. The default configuration is that the first sector of primary Flash memory is enabled and residing at the boot position, and the secondary Flash memory is disabled. This default condition may be optionally changed as described below.

5.4.1 Default configuration

When the primary Flash resides at boot position, typical CPU initialization firmware would set the start address and size of the main Flash memory, and go on to enable the secondary Flash, define it’s start address and size. Most commonly, firmware would place the secondary Flash start address at the location just after the end of the primary Flash memory. In this case, the primary Flash is used for code storage, and the smaller secondary flash can be used for data storage (EEPROM emulation).

5.4.2 Optional configuration

Using the STR91xF device configuration software tool, or IDE from 3rd party, one can specify that the smaller secondary Flash memory is at the boot location at reset and the primary Flash is disabled. The selection of which Flash memory is at the boot location is programmed in a non-volatile Flash-based configuration bit during JTAG ISP. The boot selection choice will remain as the default until the bit is erased and re-written by the JTAG interface. The CPU cannot change this choice for boot Flash, only the JTAG interface has access.

In this case where the secondary Flash defaults to the boot location upon reset, CPU firmware would typically initialize the Flash memories the following way. The secondary Flash start address and size is specified, then the primary Flash is enabled and its start address and size is specified. The primary Flash start address would typically be located just after the final address location of the secondary Flash. This configuration is particularly well-suited for In-Application-Programming (IAP). The CPU would boot from the secondary Flash memory, initialize the system, then check the contents of the primary Flash memory (by checksum or other means). If the contents of primary Flash is OK, then CPU execution continues from either Flash memory. If the main Flash contents are incorrect, the CPU, while executing code from the secondary Flash, can download new data from any STR91xF communication channel and program into primary Flash memory. Application code then starts after the new contents of primary Flash are verified.

6.2 Operating conditions

Table 5. Operating conditions

Symbol	Parameter	Test Conditions	Value		Unit
			Min	Max	
V_{DD}	Digital CPU supply voltage		1.65	2.0	V
V_{DDQ}	Digital I/O supply voltage		2.7	3.6	V
V_{BATT}(1)	SRAM backup and RTC supply voltage		2.5	3.6	V
AV_{DD}	Analog ADC supply voltage (128-pin package)		2.7	3.6	V
AV_{REF}	Analog ADC reference voltage (128-pin package)		1.0	3.6	V
AV_{REF_AVDD}	Combined analog ADC reference and ADC supply voltage (80-pin package)		2.7	3.6	V
T_A	Ambient temperature under bias		-40	+85	C

Notes: 1 The V_{BATT} pin should be connected to V_{DDQ} if no battery is installed

6.3 LVD electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 6. LVD Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_LVD}	V_{DD} LVD Threshold		1.35	1.4	1.45	V
V_{DDQ_LVD}	V_{DDQ} LVD Threshold	(1)	2.35	2.4	2.45	V
		(2)	2.65	2.7	2.75	
V_{DD_BRN}	V_{DD} Brown Out Warning Threshold		1.6	1.65	1.7	V
V_{DDQ_BRN}	V_{DDQ} Brown Out Warning Threshold	(1)	2.6	2.65	2.7	V
		(2)	2.9	2.95	3.0	

Notes: 1 For VDDQ I/O voltage operating at 2.7 - 3.3V.

2 For VDDQ I/O voltage operating at 3.0 - 3.6V.

3 Selection of V_{DDQ} operation range is made using configuration software from ST, or IDE from 3rd parties. The default condition is V_{DDQ}=2.7V - 3.3V.

6.4 DC electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 7. DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Level	General inputs	2.0		(1)	V
		RESET and TCK inputs	$0.8V_{DDQ}$			
V_{IL}	Input Low Level	General inputs			0.8	
		RESET and TCK inputs			$0.2V_{DDQ}$	
V_{HYS}	Input Hysteresis Schmitt Trigger	General inputs	0.4			V
V_{OH}	Output High Level High current pins	I/O ports 3 and 6: Push-Pull, I_{OH} = 8mA	V_{DDQ}-0.7			V
	Output High Level Standard current pins	I/O ports 0,1,2,4,5,7,8,9: Push-Pull, I_{OH} = 4mA	V_{DDQ}-0.7			
V_{OL}	Output Low Level High current pins	I/O ports 3 and 6: Push-Pull, I_{OL} = 8mA			0.4	V
	Output Low Level Standard current pins	I/O ports 0,1,2,4,5,7,8,9: Push-Pull, I_{OL} = 4mA			0.4	

Notes: 1 Input pins are 5V tolerant, max input voltage is 5.5V

Table 9. AC electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_{MSTR}	CCU Master Clk Output		32.768		96,000	kHz
f_{CPUCLK}	CPU Core Frequency	Executing from SRAM			96	MHz
		Executing from Flash			96	MHz
f_{PCLK}	Peripheral Clock for APB				48	MHz
f_{HCLK}	Peripheral Clock for AHB				96	MHz
f_{OSC}	Clock Input		4		25	MHz
f_{FMICLK}	FMI Flash Bus clock (internal clock)				96	MHz
f_{BCLK}	External Memory Bus clock (internal clock)				66	MHz
f_{RTC}	RTC Clock		32.768			kHz
f_{EMAC}	EMAC PHY Clock		25			MHz
f_{USB}	USB Clock		48			MHz

6.6 RESET_INn and power-on-reset characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 10. RESET_INn and Power-On-Reset Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{RINMIN}	RESET_INn Valid Active Low		100			ns
t_{POR}	Power-On-Reset Condition duration	V_{DDQ},V_{DD} ramp time is less than 10ms	10			ms
t_{RSO}	RESET_OUT Duration (Watchdog reset)		one PCLK			ns

6.7 Main oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 11. Main oscillator electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$t_{STUP(OSC)}$	Oscillator Start-up Time	Stable V_{DDQ}			3	mS

6.8 RTC oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 12. RTC oscillator electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$g_{M(RTC)}$	Oscillator Start _voltage		LVD [1)]			V
$t_{STUP(RTC)}$	Oscillator Start-up Time	Stable V_{DDQ}			1	S

Notes: 1 Min oscillator start voltage is the same as low voltage detect level (2.4V or 2.7V) for VDDQ

Table 13. RTC crystal electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_O	Resonant frequency			32.768		kHz
R_S	Series resistance				40	kΩ
C_L	Load capacitance			8		pF

6.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

6.11.1 Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD}, V_{DDQ} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

Table 17. EMS data

Symbol	Parameter	Conditions	Neg.	Pos.	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=1.8V, V_{DDQ}=3.3V, T_A=+25°C, f_{OSC}/f_{CPUCLK} =4 MHz/96MHz PLL	-1(1)	>2(1)	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DDQ} pins to induce a functional disturbance	V_{DD}=1.8V, V_{DDQ}=3.3V, T_A=+25°C, f_{OSC}/f_{CPUCLK} =4 MHz/96 MHz PLL conforms to IEC 1000-4-4	-4(1)	4(1)	

1. Data based on characterization results, not tested in production.

6.11.2 Electro Magnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 18. EMI data

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPUCLK}]	Unit
				4 MHz/ 96 MHz	
S_{EMI}	Peak level	V_{DDQ}=3.3V, V_{DD}=1.8V, T_A=+25°C, LQFP128 package conforming to SAE J 1752/3	0.1MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	10	
			130 MHz to 1GHz	22	
			SAE EMI Level	4	-

Notes:

1. Data based on characterization results, not tested in production.
2. BGA and LQFP devices have similar EMI characteristics.

- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

6.11.7 Electrical Sensitivities

Symbol	Parameter	Conditions	Class [1)]
LU	Static latch-up class	T_A=+25°C	A
DLU	Dynamic latch-up class	V_{DDQ}=3.3V, V_{DD}=1.8V, f_{OSC}/f_{CPUCLK}=4 MHz/96 MHz	A

Notes:

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

6.12 External memory bus timings

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C, C_L= 30 pF unless otherwise specified.

Table 20. EMI Bus Clock Period

Symbol	Parameter	Value
t_{BCLK}	EMI Bus Clock period	1 /(f_{HCLK} x EMI_ratio)

Notes: 1 The internal EMI Bus clock signal is available externally only on LFBGA144 packages (ball M8), and not available on LQFP packages.

2 EMI_ratio =1/ 2 by default (can be programmed to be 1 by setting the proper bits in the SCU_CLKCNTR register)

Table 21. EMI read operation

Symbol	Parameter	Value		Unit
		Min	Max	
t_{RCR}	Read to CSn inactive	-1	+1	ns
t_{RP}	Read Pulse Width	(WSTRD-WSTOEN+1) x t_{BCLK} - 1	(WSTRD-WSTOEN+1) x t_{BCLK} + 1	ns
t_{RDS}	Read Data Setup Time	4		ns
t_{RDH}	Read Data Hold Time	0		ns
t_{RAS}	Read Address Setup Time	(WSTOEN) x t_{BCLK}- 1	(WSTOEN) x t_{BCLK} + 1	ns
t_{RAH}	Read Address Hold Time	0		ns
t_{AW}	ALE pulse width	(ALE_LENGTH) x t_{BCLK} - 1	(ALE_LENGTH) x t_{BCLK} + 1	ns

Symbol	Parameter	Value		Unit
		Min	Max	
t_{AAH}	Address to ALE hold time	$t_{BCLK/2}$ - 1	$t_{BCLK/2}$ + 1	ns
t_{AAS}	Address to ALE setup time	(ALE_LENGTH) x t_{BCLK} - 1		ns

Notes: 1 ALE_LENGTH = 1 by default (can be programmed to be 2 by setting the bits In the SCU_SCR0 register)

2 WSTRD = 1Fh by default (RD wait state time = WSTRD x t_{BCLK}, WSTRD can be programmed in the EMI_RCRx Register)

3 WSTOEN = 1 by default (RD assertion delay from chip select. WSTOEN can be programmed in the EMI_OECRx Register)

Figure 11. Non-mux bus (8-bit) read timings

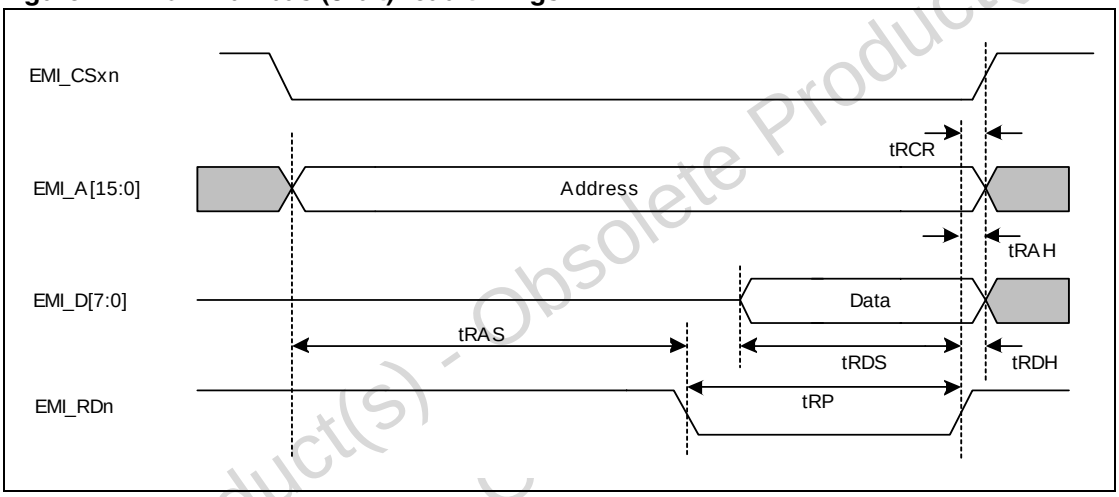


Figure 12. Mux bus (16-bit) read timings

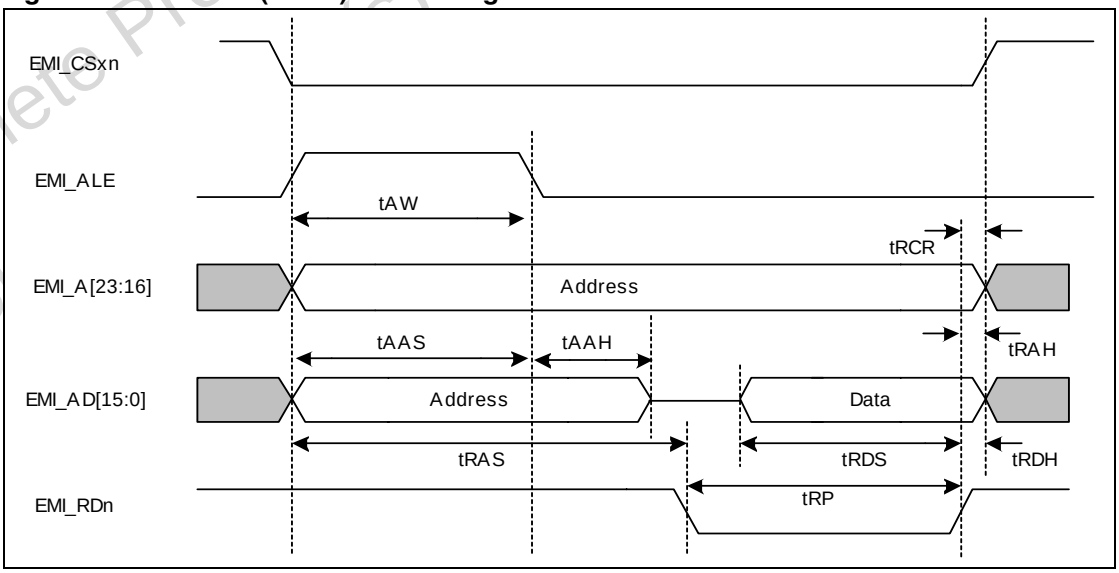


Table 22. EMI write operation

Symbol	Parameter	Test Conditions	Value		Unit
			Min	Max	
t_{WCR}	WRn to CSn inactive		$(t_{BCLK}/2)$ - 1	$(t_{BCLK}/2)$ +1	ns
t_{WP}	Write Pulse Width		(WSTWR-WSTWEN + 1) x t_{BCLK} - 1	(WSTWR-WSTWEN + 1) x t_{BCLK} + 1	ns
t_{WDS}	Write Data Setup Time (non-mux mode)		(WSTWEN + 1/2) x t_{BCLK}		ns
	Write Data Setup Time (mux mode)	ALE length=1 WSTWEN>2	(WSTWEN - 1.5) x t_{BCLK}		
		ALE length=2 WSTWEN>3	(WSTWEN - 2.5) x t_{BCLK}		
t_{WDH}	Write Data Hold Time		$(t_{BCLK}/2)$ - 1	$(t_{BCLK}/2)$ + 1	ns
t_{WAS}	Write Address Setup Time		(WSTWEN + 1/2) x t_{BCLK} -1 [4]	(WSTWEN + 1/2) x t_{BCLK} +1 [4]	ns
t_{WAH}	Write Address Hold Time		$t_{BCLK}/2$		ns
t_{AW}	ALE pulse width		(ALE_LENGTH x t_{BCLK})-1	(ALE_LENGTH x t_{BCLK}) +1	ns
t_{AAH}	Address to ALE hold time		$(t_{BCLK}/2)$ -1	$(t_{BCLK}/2)$ + 1	ns
t_{AAS}	Address to ALE setup time		(ALE_LENGTH x t_{BCLK})- 1		ns

Notes: 1 ALE_LENGTH = 1 by default (can be programmed to be 2 by setting the bits In the SCU_SCR0 register)

2 WSTWR =1Fh by default (WR wait state time = WSTWR x t_{BCLK}, WSTWR can be programmed in the EMI_WCRx Register)

3 WSTWEN= 0 by default (WR assertion delay from chip select. WSTWEN can be programmed in the EMI_WECRx Register)

4 When the CPU executes a 16-bit write to a x8 EMI bus, the second write cycle's address setup time is defined as t_{WAS}=(WSTWEN - ½) x t_{BCLK}

Figure 13. Non-Mux Bus (8-bit) write timings

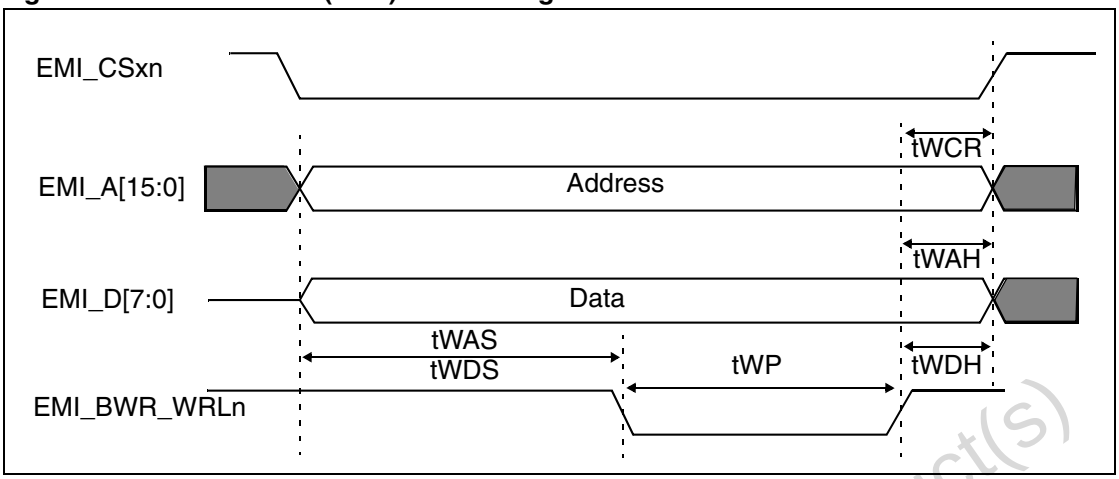
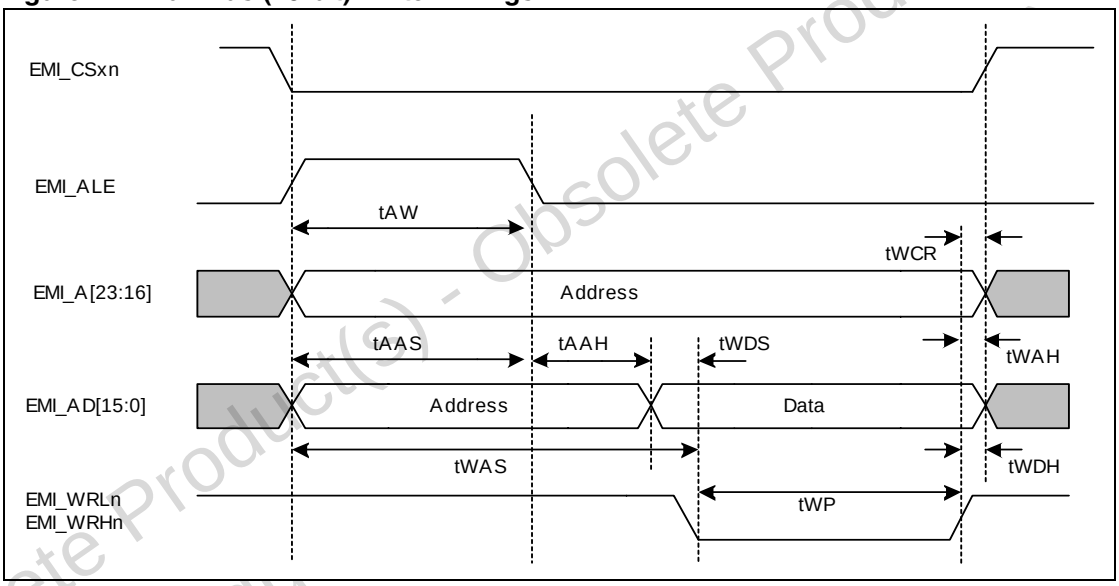


Figure 14. Mux Bus (16-bit) Write Timings



6.13 ADC electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 23. ADC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
V_{AIN}	Input Voltage Range		0		AV_{REF}	V
RES	Resolution				10	Bits
N_{CH}	Number of Input Channels				8	N
f_{ADC}	ADC Clock Frequency				25	MHz
	POR bit set to Standby mode				500	ms
	Conversion Time	f_{ADC} = 25 MHz		0.7		µs
	Throughput Rate	f_{ADC} = 25 MHz		1400		ksps
C_{IN}	Input Capacitance			5		pF
E_D	Differential Non-Linearity	[1] [2]		1	3	LSB[3]
E_L	Integral Non-Linearity	[1]		3	6	LSB
E_O	Offset Error	[1]		3	6	LSB
E_G	Gain Error	[1]		0.5	2	LSB
E_T	Absolute Error	[1]		4	6	LSB
I_{ADC}	Power Consumption			4.6	6	mA

Notes: 1 Conditions: A_{VSS} = 0 V, AV_{DD} = 3.3 V f_{ADC} = 25 MHz.

2 The A/D is monotonic, there are no missing codes.

3 1 LSB = (V_{DDA} - V_{SSA})/1024

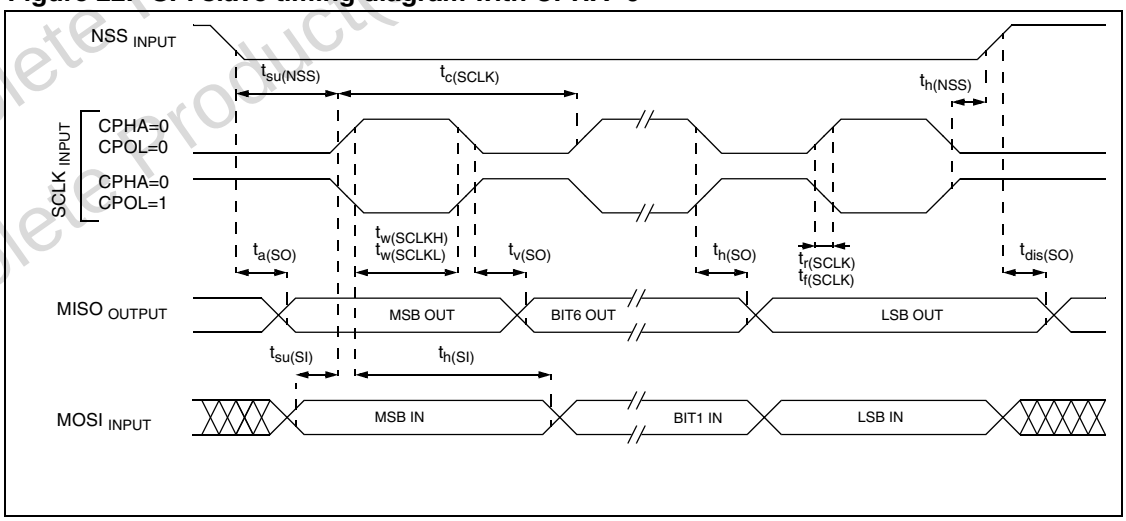
6.14.5 SPI electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 29. SPI electrical characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max	
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master		24	MHz
		Slave		4	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall times	50pF load	0.1		V/ns
$t_{su(SS)}$	SS setup time	Slave	1		t_{PCLK}
$t_{h(SS)}$	SS hold time	Slave	1		
$t_{w(SCLKH)}$ $t_{w(SCLKL)}$	SCLK high and low time	Master Slave	1		
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Slave	5		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Slave	6		
$t_{a(SO)}$	Data output access time	Slave		6	
$t_{dis(SO)}$	Data output disable time	Slave		6	
$t_{v(SO)}$	Data output valid time	Slave (after enable edge)		6	
$t_{h(SO)}$	Data output hold time		0		
$t_{v(MO)}$	Data output valid time	Master (before capture edge)	0.25		
$t_{h(MO)}$	Data output hold time		0.25		

Figure 22. SPI slave timing diagram with CPHA=0



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