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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912fw42x6

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2.5 SRAM (64K or 96K Bytes)

A 32-bit wide SRAM resides on the CPU's Data TCM (D-TCM) interface, providing single-cycle data accesses. As shown in *Figure 1*, the D-TCM shares SRAM access with the Advanced High-performance Bus (AHB). Sharing is controlled by simple arbitration logic to allow the DMA unit on the AHB to also access to the SRAM.

2.5.1 Arbitration

Zero-wait state access occurs for either the D-TCM or the AHB when only one of the two is requesting SRAM. When both request SRAM simultaneously, access is granted on an interleaved basis so neither requestor is starved, granting one 32-bit word transfer to each requestor before relinquishing SRAM to the other. When neither the D-TCM or the AHB are requesting SRAM, the arbiter leaves access granted to the most recent user (if D-TCM was last to use SRAM then the D-TCM will not have to arbitrate to get access next time).

The CPU may execute code from SRAM through the AHB. There are no wait states as long as the D-TCM is not contending for SRAM access and the AHB is not sharing bandwidth with peripheral traffic. The ARM966E-S CPU core has a small pre-fetch queue built into this instruction path through the AHB to look ahead and fetch instructions during idle bus cycles.

2.5.2 Battery backup

When a battery is connected to the designated battery backup pin (VBATT), SRAM contents are automatically preserved when the normal operating voltage on VDD pins is lost or sags below threshold. Automatic switchover to SRAM can be disabled by firmware if it is desired that the battery will power only the RTC and not the SRAM during standby.

2.6 DMA data movement

DMA channels on the Advanced High-performance Bus (AHB) take full advantage of the separate data path provided by the Harvard architecture, moving data rapidly and largely independent of the instruction path. There are two DMA units, one is dedicated to move data between the Ethernet interface and SRAM, the other DMA unit has eight programmable channels with 16 request signals to service other peripherals and interfaces (USB, SSP, I2C, UART, Timers, EMI, and external request pins). Both single word and burst DMA transfers are supported. Memory-to-memory transfers are supported in addition to memory-peripheral transfers. DMA access to SRAM is shared with D-TCM accesses, and arbitration is described in *Section 2.5.1*. Efficient DMA transfers are managed by firmware using linked list descriptor tables. Of the 16 DMA request signals, two are assigned to external inputs. The DMA unit can move data between external devices and resources inside the STR91xF through the EMI bus.

2.7 Non-volatile memories

There are two independent 32-bit wide Burst Flash memories enabling true read-while-write operation. The Flash memories are single-voltage erase/program with 20 year minimum data retention and 100K minimum erase cycles. The primary Flash memory is much larger than the secondary Flash.

Both Flash memories are blank when devices are shipped from ST. The CPU can boot only from Flash memory (configurable selection of which Flash bank).

See *Table 2* for recommended interrupt source assignments to physical IRQ interrupt channels. Interrupt source assignments are made by CPU firmware during initialization, thus establishing interrupt priorities.

Table 2. Recommended IRQ Channel assignments (set by CPU firmware)

VIC IRQ Channel	Logic Block	Interrupt Source
0 (high priority)	WatchDog	Timeout in WDT mode, Terminal Count in Counter Mode
1	CPU Firmware	Firmware generated interrupt
2	CPU Core	Debug Receive Command
3	CPU Core	Debug Transmit Command
4	TIM Timer 0	Logic OR of ICI0_0, ICI0_1, OCI0_0, OCI0_1, Timer overflow
5	TIM Timer 1	Logic OR of ICI1_0, ICI1_1, OCI1_0, OCI1_1, Timer overflow
6	TIM Timer 2	Logic OR of ICI2_0, ICI2_1, OCI2_0, OCI2_1, Timer overflow
7	TIM Timer 3	Logic OR of ICI3_0, ICI3_1, OCI3_0, OCI3_1, Timer overflow
8	USB	Logic OR of high priority USB interrupts
9	USB	Logic OR of low priority USB interrupts
10	CCU	Logic OR of all interrupts from Clock Control Unit
11	Ethernet MAC	Logic OR of Ethernet MAC interrupts via its own dedicated DMA channel.
12	DMA	Logic OR of interrupts from each of the 8 individual DMA channels
13	CAN	Logic OR of all CAN interface interrupt sources
14	IMC	Logic OR of 8 Induction Motor Control Unit interrupts
15	ADC	End of AtoD conversion interrupt
16	UART0	Logic OR of 5 interrupts from UART channel 0
17	UART1	Logic OR of 5 interrupts from UART channel 1
18	UART2	Logic OR of 5 interrupts from UART channel 2
19	I2C0	Logic OR of transmit, receive, and error interrupts of I2C channel 0
20	I2C1	Logic OR of transmit, receive, and error interrupts of I2C channel 1
21	SSP0	Logic OR of all interrupts from SSP channel 0
22	SSP1	Logic OR of all interrupts from SSP channel 1
23	BROWNOUT	LVD warning interrupt
24	RTC	Logic OR of Alarm, Tamper, or Periodic Timer interrupts
25	Wake-Up (all)	Logic OR of all 32 inputs of Wake-Up unit (30 pins, RTC, and USB Resume)
26	Wake-up Group 0	Logic OR of 8 interrupt sources: RTC, USB Resume, pins P3.2 to P3.7
27	Wake-up Group 1	Logic OR of 8 interrupts from pins P5.0 to P5.7
28	Wake-up Group 2	Logic OR of 8 interrupts from pins P6.0 to P6.7
29	Wake-up Group 3	Logic OR of 8 interrupts from pins P7.0 to P7.7
30	USB	USB Bus Resume Wake-up (also input to wake-up unit)
31 (low priority)	PFQ-BC	Special use of interrupts from Prefetch Queue and Branch Cache

2.10 Clock control unit (CCU)

The CCU generates a master clock of frequency f_{MSTR}. From this master clock the CCU also generates individually scaled and gated clock sources to each of the following functional blocks within the STR91xF.

- CPU, f_{CPUCLK}
- Advanced High-performance Bus (AHB), f_{HCLK}
- Advanced Peripheral Bus (APB), f_{PCLK}
- Flash Memory Interface (FMI), f_{FMICLK}
- External Memory Interface (EMI), f_{BCLK}
- UART Baud Rate Generators, f_{BAUD}
- USB, f_{USB}

2.10.1 Master clock sources

The master clock in the CCU (f_{MSTR}) is derived from one of three clock input sources. Under firmware control, the CPU can switch between the three CCU inputs without introducing any glitches on the master clock output. Inputs to the CCU are:

- Main Oscillator (f_{OSC}). The source for the main oscillator input is a 4 to 25 MHz external crystal connected to STR91xF pins X1_CPU and X2_CPU, or an external oscillator device connected to pin X1_CPU.
- PLL (f_{PLL}). The PLL takes the 4 to 25 MHz oscillator clock as input and generates a master clock output up to 96 MHz (programmable). By default, at power-up the master clock is sourced from the main oscillator until the PLL is ready (locked) and then the CPU may switch to the PLL source under firmware control. The CPU can switch back to the main oscillator source at any time and turn off the PLL for low-power operation. The PLL is always turned off in Sleep mode.
- RTC (f_{RTC}). A 32.768 kHz external crystal can be connected to pins X1_RTC and X2_RTC, or an external oscillator connected to pin X1_RTC to constantly run the real-time clock unit. This 32.768 kHz clock source can also be used as an input to the CCU to run the CPU in slow clock mode for reduced power.

As an option, there are a number of peripherals that do not have to receive a clock sourced from the CCU. The USB interface can receive an external clock on pin P2.7, TIM timers TIM0/TIM1 can receive an external clock on pin P2.4, and timers TIM2/TIM3 on pin P2.5.

2.11 Flexible power management

The STR91xF offers configurable and flexible power management control that allows the user to choose the best power option to fit the application. Power consumption can be dynamically managed by firmware and hardware to match the system's requirements. Power management is provided via clock control to the CPU and individual peripherals.

Clocks to the CPU and peripherals can be individually divided and gated off as needed. In addition to individual clock divisors, the CCU master clock source going to the CPU, AHB, APB, EMI, and FMI can be divided dynamically by as much as 1024 for low power operation. Additionally, the CCU may switch its input to the 32.768 kHz RTC clock at any time for low power.

The STR91xF supports the following three global power control modes:

- **Run Mode:** All clocks are on with option to gate individual clocks off via clock mask registers.
- **Idle Mode:** CPU and FMI clocks are off until an interrupt, reset, or wake-up occurs. Pre-configured clock mask registers selectively allow individual peripheral clocks to continue run during Idle Mode.
- **Sleep Mode:** All clocks off except RTC clock. Wake up unit remains powered, PLL is forced off.

A special mode is used when JTAG debug is active which never gates off any clocks even if the CPU enters Idle or Sleep mode.

2.11.1 Run mode

This is the default mode after any reset occurs. Firmware can gate off or scale any individual clock. Also available is a special Interrupt Mode which allows the CPU to automatically run full speed during an interrupt service and return back to the selected CPU clock divisor rate when the interrupt has been serviced. The advantage here is that the CPU can run at a very low frequency to conserve power until a periodic wake-up event or an asynchronous interrupt occurs at which time the CPU runs full speed immediately.

2.11.2 Idle mode

In this mode the CPU suspends code execution and the CPU and FMI clocks are turned off immediately after firmware sets the Idle Bit. Various peripherals continue to run based on the settings of the mask registers that exist just prior to entering Idle Mode. There are 3 ways to exit Idle Mode and return to Run Mode:

- Any reset (external reset pin, watchdog, low-voltage, power-up, JTAG debug command)
- Any interrupt (external, internal peripheral, RTC alarm or interval)
- Input from wake-up unit on GPIO pins

Note: It is possible to remain in Idle Mode for the majority of the time and the RTC can be programmed to periodically wake up to perform a brief task or check status.

2.11.3 Sleep mode

In this mode all clock circuits except the RTC are turned off and main oscillator input pins X1_CPU and X2_CPU are disabled. The RTC clock is required for the CPU to exit Sleep Mode. The entire chip is quiescent (except for RTC and wake-up circuitry). There are three means to exit Sleep Mode and re-start the system:

2.13 System supervisor

The STR91xF monitors several system and environmental inputs and will generate a global reset, a system reset, or an interrupt based on the nature of the input and configurable settings. A global reset clears all functions on the STR91xF, a system reset will clear all but the Clock Control Unit (CCU) settings and the system status register. At any time, firmware may reset individual on-chip peripherals. System supervisor inputs include:

- GR: CPU voltage supply (V_{DD}) drop out or brown out
- GR: I/O voltage supply (V_{DDQ}) drop out or brown out
- GR: Power-Up condition
- SR: Watchdog timer timeout
- SR: External reset pin (RESET_INn)
- SR: JTAG debug reset command

Note: GR: means the input causes Global Reset, SR: means the input causes System Reset

The CPU may read a status register after a reset event to determine if the reset was caused by a watchdog timer timeout or a voltage supply drop out. This status register is cleared only by a power up reset.

2.13.1 Supply voltage brownout

Each operating voltage source (V_{DD} and V_{DDQ}) is monitored separately by the Low Voltage Detect (LVD) circuitry. The LVD will generate an early warning interrupt to the CPU when voltage sags on either V_{DD} or V_{DDQ} voltage inputs. This is an advantage for battery powered applications because the system can perform an orderly shutdown before the batteries become too weak. The voltage trip point to cause a brown out interrupt is typically 0.25V above the LVD dropout thresholds that cause a reset.

CPU firmware may prevent all brown-out interrupts by writing to interrupt mask registers at run-time.

2.13.2 Supply voltage dropout

LVD circuitry will always cause a global reset if the CPU's V_{DD} source drops below it's fixed threshold of 1.4V.

However, the LVD trigger threshold to cause a global reset for the I/O ring's V_{DDQ} source is set to one of two different levels, depending if V_{DDQ} will be operated in the range of 2.7V to 3.3V, or 3.0V to 3.6V. If V_{DDQ} operation is at 2.7V to 3.3V, the LVD dropout trigger threshold is 2.4V. If V_{DDQ} operation is 3.0V and 3.6V, the LVD threshold is 2.7V. The choice of trigger level is made by STR91xF device configuration software from STMicroelectronics or IDE from 3rd parties, and is programmed into the STR91xF device along with other configurable items through the JTAG interface when the Flash memory is programmed.

CPU firmware may prevent some LVD resets if desired by writing a control register at run-time. Firmware may also disable the LVD completely for lowest-power operation when an external LVD device is being used.

2.13.3 Watchdog timer

The STR91xF has a 16-bit down-counter (not one of the four TIM timers) that can be used as a watchdog timer or as a general purpose free-running timer/counter. The clock source is the

Debugging requires that an external host computer, running debug software, is connected to the STR91xF target system via hardware which converts the stream of debug data and commands from the host system's protocol (USB, Ethernet, etc.) to the JTAG EmbeddedICE-RT protocol on the STR91xF. These protocol converters are commercially available and operate with debugging software tools.

The CPU may be forced into a Debug State by a breakpoint (code fetch), a watchpoint (data access), or an external debug request over the JTAG channel, at which time the CPU core and memory system are effectively stopped and isolated from the rest of the system. This is known as Halt Mode and allows the internal state of the CPU core, memory, and peripherals to be examined and manipulated. Typical debug functions are supported such as run, halt, and single-step. The EmbeddedICE-RT logic supports two hardware compare units. Each can be configured to be either a watchpoint or a breakpoint. Breakpoints can also be data-dependent.

Debugging (with some limitations) may also occur through the JTAG interface while the CPU is running full speed, known as Monitor Mode. In this case, a breakpoint or watchpoint will not force a Debug State and halt the CPU, but instead will cause an exception which can be tracked by the external host computer running monitor software. Data can be sent and received over the JTAG channel without affecting normal instruction execution. Time critical code, such as Interrupt Service Routines may be debugged real-time using Monitor Mode.

2.15.4 JTAG security bit

This is a non-volatile bit (Flash memory based), which when set will not allow the JTAG debugger or JTAG programmer to read the Flash memory contents.

Using JTAG ISP, this bit is typically programmed during manufacture of the end product to prevent unwanted future access to firmware intellectual property. The JTAG Security Bit can be cleared only by a JTAG "Full Chip Erase" command, making the STR91xF device blank and ready for programming again. The CPU can read the status of the JTAG Security Bit, but it may not change the bit value.

2.16 Embedded trace module (ARM ETM9, v. r2p2)

The ETM9 interface provides greater visibility of instruction and data flow happening inside the CPU core by streaming compressed data at a very high rate from the STR91xF though a small number of ETM9 pins to an external Trace Port Analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or other high-speed channel. Real-time instruction flow and data activity can be recorded and later formatted and displayed on the host computer running debugger software, and this software is typically integrated with the debug software used for EmbeddedICE-RT functions such as single-step, breakpoints, etc. Tracing may be triggered and filtered by many sources, such as instruction address comparators, data watchpoints, context ID comparators, and counters. State sequencing of up to three triggers is also provided. TPA hardware is commercially available and operates with debugging software tools.

The ETM9 interface is nine pins total, four of which are data lines, and all pins can be used for GPIO after tracing is no longer needed. The ETM9 interface is used in conjunction with the JTAG interface for trace configuration. When tracing begins, the ETM9 engine compresses the data by various means before broadcasting data at high speed to the TPA over the four data lines. The most common ETM9 compression technique is to only output address information when the CPU branches to a location that cannot be inferred from the source code. This means

the host computer must have a static image of the code being executed for decompressing the ETM9 data. Because of this, self-modified code cannot be traced.

2.17 Ethernet MAC interface with DMA

STR91xF devices in 128-pin packages provide an IEEE-802.3-2002 compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry standard Medium Independent Interface (MII). The STR91xF requires an external Ethernet physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the STR91xF MII port using as many as 18 signals (see pins which have signal names MII_* in *Table 3*).

The MAC corresponds to the OSI Data Link layer and the PHY corresponds to the OSI Physical layer. The STR91xF MAC is responsible for:

- Data encapsulation, including frame assembly before transmission, and frame parsing/ error detection during and after reception.
- Media access control, including initiation of frame transmission and recover from transmission failure.

The STR91xF MAC includes the following features:

- Supports 10 and 100 Mbps rates
- Tagged MAC frame support (VLAN support)
- Half duplex (CSMA/CD) and full duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. Transmit FIFO depth is 4 words (32 bits each), and the receive FIFO is 16 words deep.

A 32-bit burst DMA channel residing on the AHB is dedicated to the Ethernet MAC for high-speed data transfers, side-stepping the CPU for minimal CPU impact during transfers. This DMA channel includes the following features:

- Direct SRAM to MAC transfers of transmit frames with the related status, by descriptor chain
- Direct MAC to SRAM transfers of receive frames with the related status, by descriptor chain
- Open and Closed descriptor chain management

2.18 USB 2.0 slave device interface with DMA

The STR91xF provides a USB slave controller that implements both the OSI Physical and Data Link layers for direct bus connection by an external USB host on pins USBDP and USBPN. The USB interface detects token packets, handles data transmission and reception, and processes handshake packets as required by the USB 2.0 standard.

The USB slave interface includes the following features:

- Supports USB low and full-speed transfers (12 Mbps), certified to comply with the USB 2.0 specification
- Supports isochronous, bulk, control, and interrupt endpoints
- Configurable number of endpoints allowing a mixture of up to 20 single-buffered monodirectional endpoints or up to 10 double-buffered bidirectional endpoints
- Dedicated, dual-port 2 Kbyte USB Packet Buffer SRAM. One port of the SRAM is connected by a Packet Buffer Interface (PBI) on the USB side, and the CPU connects to the other SRAM port.
- CRC generation and checking
- NRZI encoding-decoding and bit stuffing
- USB suspend resume operations

2.18.1 Packet buffer interface (PBI)

The PBI manages a set of buffers inside the 2 Kbyte Packet Buffer, both for transmission and reception. The PBI will choose the proper buffer according to requests coming from the USB Serial Interface Engine (SIE) and locate it in the Packet SRAM according to addresses pointed by endpoint registers. The PBI will also auto-increment the address after each exchanged byte until the end of packet, keeping track of the number of exchanged bytes and preventing buffer overrun. Special support is provided by the PBI for isochronous and bulk transfers, implementing double-buffer usage which ensures there is always an available buffer for a USB packet while the CPU uses a different buffer.

2.18.2 DMA

A programmable DMA channel may be assigned by CPU firmware to service the USB interface for fast and direct transfers between the USB bus and SRAM with little CPU involvement. This DMA channel includes the following features:

- Direct USB Packet Buffer SRAM to system SRAM transfers of receive packets, by descriptor chain for bulk or isochronous endpoints.
- Direct system SRAM to USB Packet Buffer SRAM transfers of transmit packets, by descriptor chain for bulk or isochronous endpoints.
- Linked-list descriptor chain support for multiple USB packets

2.18.3 Suspend mode

CPU firmware may place the USB interface in a low-power suspend mode when required, and the USB interface will automatically wake up asynchronously upon detecting activity on the USB pins.

2.19 CAN 2.0B interface

The STR91xF provides a CAN interface complying with CAN protocol version 2.0 parts A and B. An external CAN transceiver device connected to pins CAN_RX and CAN_TX is required for connection to the physical CAN bus.

The CAN interface manages up to 32 Message Objects and Identifier Masks using a Message SRAM and a Message Handler. The Message Handler takes care of low-level CAN bus activity such as acceptance filtering, transfer of messages between the CAN bus and the Message

5 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes (2^{32}) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

5.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

5.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xF Reference manual for the address of data locations within each individual peripheral.

5.3 SRAM

The SRAM is aliased at three separate address ranges as shown in *Figure 9*. When the CPU accesses SRAM starting at 0x0400.0000, the SRAM appears on the D-TCM. When CPU access starts at 0x4000.0000, SRAM appears in the buffered AHB range. Beginning at CPU address 0x5000.0000, SRAM is in non-buffered AHB range. The SRAM size must be specified by CPU intitialization firmware writing to a control register after any reset condition. Default SRAM size is 32K bytes, with option to set to 64K bytes on STR91xFx32 devices, and to 96K bytes on STR91xFx44 devices.

6.5 AC electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 8. AC electrical characteristics

Symbol	Parameter	Test Conditions		Value			Unit
				Min	Typ	Max	
I_{DDRUN}	Run Mode Current	All peripherals on	CPU_CLK = 96MHz [1] [5]		1.7	2.3	mA/ MHz
		All peripherals off			1.3	1.6	
I_{IDLE}	Idle Mode Current	All peripherals on [2] [5]			1.14	1.7	mA/ MHz
		All peripherals off [3] [5]			0.45	0.75	mA/ MHz
I_{SLEEP}	Sleep Mode Current	LVD On [4] [5]			55	825	µA
		LVD Off [4] [5]			50	820	µA
I_{RTC_STBY}	RTC Standby Current	Measured on VBATT pin			0.3	0.9	µA
I_{SRAM_STBY}	SRAM Standby Current	Measured on VBATT pin			5	85	µA

Notes: 1 ARM core and peripherals active with all clocks on. Power can be conserved by turning off clocks to peripherals which are not required.

2 ARM core stopped and all peripheral clocks active.

3 ARM core stopped and all peripheral clocks stopped.

4 ARM core and all peripheral clocks stopped (with exception of RTC).

5 Current measured on the V_{DD} pins. V_{DDQ} current is not included.

Figure 10. Sleep Mode current vs temperature

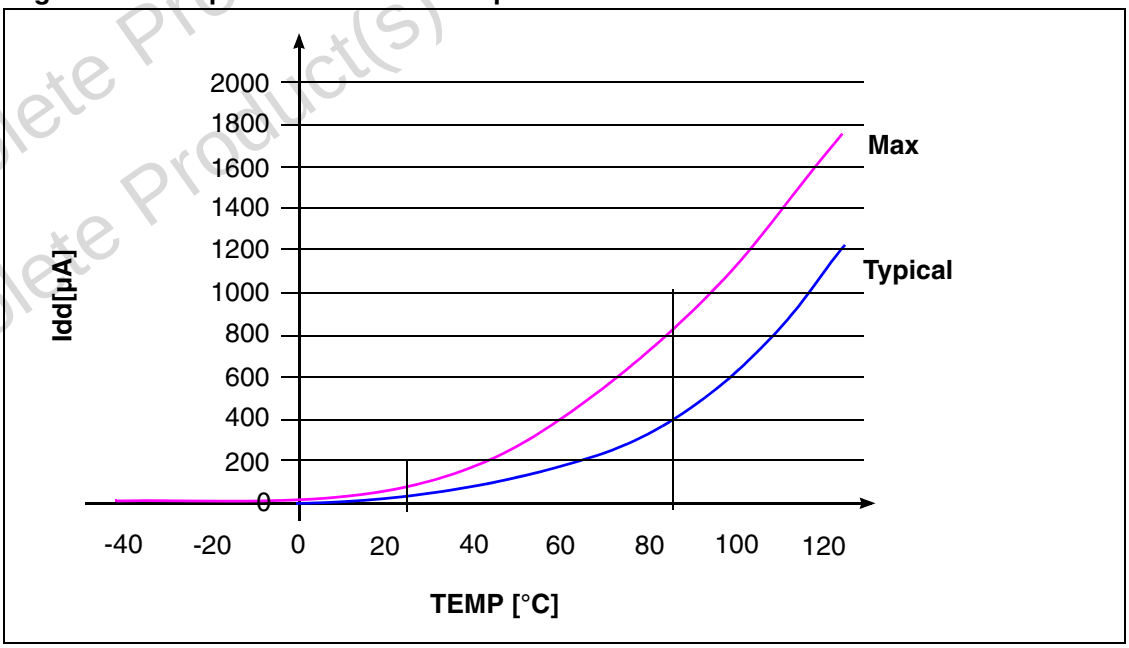

Table 9. AC electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_{MSTR}	CCU Master Clk Output		32.768		96,000	kHz
f_{CPUCLK}	CPU Core Frequency	Executing from SRAM			96	MHz
		Executing from Flash			96	MHz
f_{PCLK}	Peripheral Clock for APB				48	MHz
f_{HCLK}	Peripheral Clock for AHB				96	MHz
f_{OSC}	Clock Input		4		25	MHz
f_{FMICLK}	FMI Flash Bus clock (internal clock)				96	MHz
f_{BCLK}	External Memory Bus clock (internal clock)				66	MHz
f_{RTC}	RTC Clock		32.768			kHz
f_{EMAC}	EMAC PHY Clock		25			MHz
f_{USB}	USB Clock		48			MHz

6.6 RESET_INn and power-on-reset characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 10. RESET_INn and Power-On-Reset Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{RINMIN}	RESET_INn Valid Active Low		100			ns
t_{POR}	Power-On-Reset Condition duration	V_{DDQ},V_{DD} ramp time is less than 10ms	10			ms
t_{RSO}	RESET_OUT Duration (Watchdog reset)		one PCLK			ns

6.7 Main oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 11. Main oscillator electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$t_{STUP(OSC)}$	Oscillator Start-up Time	Stable V_{DDQ}			3	mS

6.8 RTC oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 12. RTC oscillator electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$g_{M(RTC)}$	Oscillator Start _voltage		LVD [1)]			V
$t_{STUP(RTC)}$	Oscillator Start-up Time	Stable V_{DDQ}			1	S

Notes: 1 Min oscillator start voltage is the same as low voltage detect level (2.4V or 2.7V) for VDDQ

Table 13. RTC crystal electrical characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_O	Resonant frequency			32.768		kHz
R_S	Series resistance				40	kΩ
C_L	Load capacitance			8		pF

6.9 PLL electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 14. PLL Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL}	PLL Output Clock		6.25		96	MHz
f_{OSC}	Clock Input		4		25	MHz
t_{LOCK}	PLL lock time			300	1500	µs
Δt_{JITTER}	PLL Jitter (peak to peak)			0.1	0.2	ns

Table 22. EMI write operation

Symbol	Parameter	Test Conditions	Value		Unit
			Min	Max	
t_{WCR}	WRn to CSn inactive		$(t_{BCLK}/2)$ - 1	$(t_{BCLK}/2)$ +1	ns
t_{WP}	Write Pulse Width		(WSTWR-WSTWEN + 1) x t_{BCLK} - 1	(WSTWR-WSTWEN + 1) x t_{BCLK} + 1	ns
t_{WDS}	Write Data Setup Time (non-mux mode)		(WSTWEN + 1/2) x t_{BCLK}		ns
	Write Data Setup Time (mux mode)	ALE length=1 WSTWEN>2	(WSTWEN - 1.5) x t_{BCLK}		
		ALE length=2 WSTWEN>3	(WSTWEN - 2.5) x t_{BCLK}		
t_{WDH}	Write Data Hold Time		$(t_{BCLK}/2)$ - 1	$(t_{BCLK}/2)$ + 1	ns
t_{WAS}	Write Address Setup Time		(WSTWEN + 1/2) x t_{BCLK} -1 [4]	(WSTWEN + 1/2) x t_{BCLK} +1 [4]	ns
t_{WAH}	Write Address Hold Time		$t_{BCLK}/2$		ns
t_{AW}	ALE pulse width		(ALE_LENGTH x t_{BCLK})-1	(ALE_LENGTH x t_{BCLK}) +1	ns
t_{AAH}	Address to ALE hold time		$(t_{BCLK}/2)$ -1	$(t_{BCLK}/2)$ + 1	ns
t_{AAS}	Address to ALE setup time		(ALE_LENGTH x t_{BCLK})- 1		ns

Notes: 1 ALE_LENGTH = 1 by default (can be programmed to be 2 by setting the bits In the SCU_SCR0 register)

2 WSTWR =1Fh by default (WR wait state time = WSTWR x t_{BCLK}, WSTWR can be programmed in the EMI_WCRx Register)

3 WSTWEN= 0 by default (WR assertion delay from chip select. WSTWEN can be programmed in the EMI_WECRx Register)

4 When the CPU executes a 16-bit write to a x8 EMI bus, the second write cycle's address setup time is defined as t_{WAS}=(WSTWEN - ½) x t_{BCLK}

6.14 Communication interface electrical characteristics

6.14.1 10/100 Ethernet MAC electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Ethernet MII Interface Timings

Figure 16. MII_RX_CLK and MII_TX_CLK timing diagram

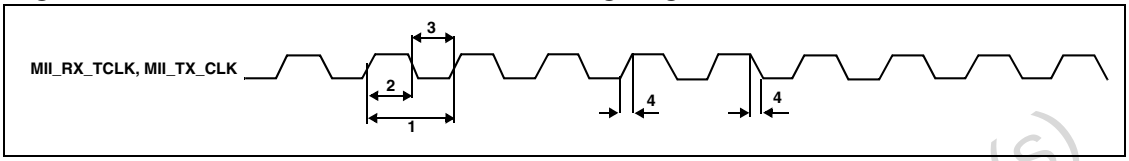

Table 24. MII_RX_CLK and MII_TX_CLK timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	t_c(CLK)	40		ns
2	Pulse duration HIGH	t_{HIGH}(CLK)	40%	60%	
3	Pulse duration LOW	t_{LOW}(CLK)	40%	60%	
4	Transition time	t_t(CLK)		1	ns

Figure 17. MDC timing diagram

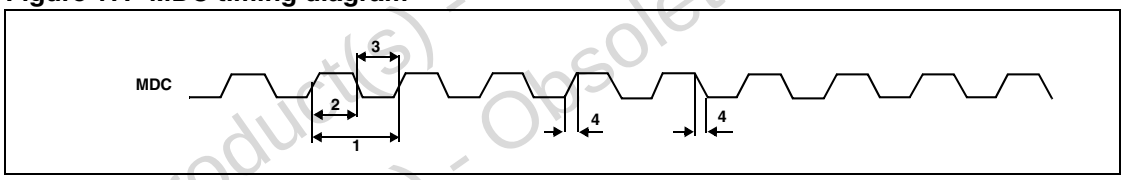

Table 25. MDC timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	t_c(MDC)	266		ns
2	Pulse duration HIGH	t_{HIGH}(MDC)	40%	60%	
3	Pulse duration LOW	t_{LOW}(MDC)	40%	60%	
4	Transition time	t_t(MDC)		1	ns

Ethernet MII management timings

Figure 18. Ethernet MII management timing diagram

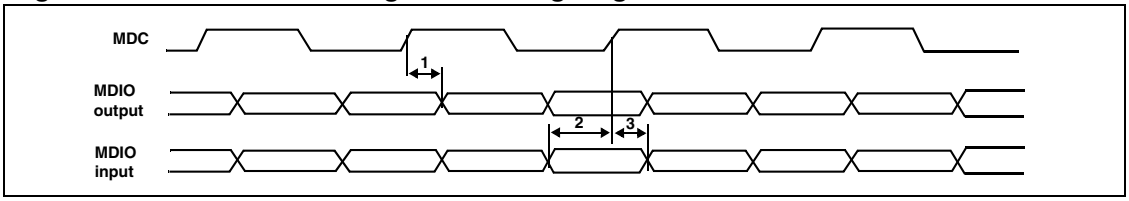

Table 26. Ethernet MII management timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	MDIO delay from rising edge of MDC	t_c(MDIO)		2.83	ns
2	MDIO setup time to rising edge of MDC	T_{su} (MDIO)	2.70		ns
3	MDIO hold time from rising edge of MDC	T_h (MDIO)	-2.03		ns

Ethernet MII transmit timings

Figure 19. Ethernet MII transmit timing diagram

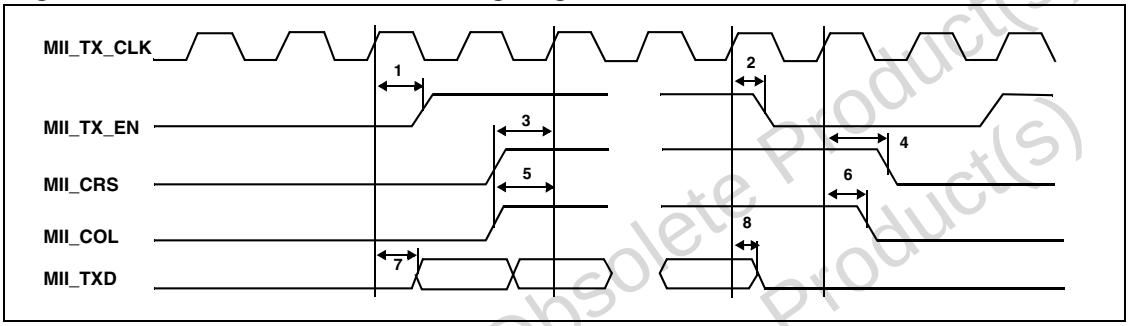

Table 27. Ethernet MII transmit timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	MII_TX_CLK high to MII_TX_EN valid	t_{VAL}(MII_TX_EN)		4.20	ns
2	MII_TX_CLK high to MII_TX_EN invalid	T_{inval}(MII_TX_EN)		4.86	ns
3	MII_CRS valid to MII_TX_CLK high	T_{su}(MII_CRS)	0.61		ns
4	MII_TX_CLK high to MII_CRS invalid	T_h(MII_CRS)	0.00		ns
5	MII_COL valid to MII_TX_CLK high	T_{su}(MII_COL)	0.81		ns
6	MII_TX_CLK high to MII_COL invalid	T_h(MII_COL)	0.00		ns
7	MII_TX_CLK high to MII_TXD valid	t_{VAL}(MII_TXD)		5.02	ns
8	MII_TXCLK high to MII_TXD invalid	T_{inval}(MII_TXD		5.02	ns

7.1 Thermal characteristics

The average chip-junction temperature, T_J must never exceed 125° C.

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories. The worst case P_{INT} of the STR91xF is 500mW ($I_{DD} \times V_{DD}$, or 250mA x 2.0V).

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 (3)$$

where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 30. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 80 - 12 x 12 mm / 0.5 mm pitch	41.5	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP128 - 14 x 14 mm / 0.4 mm pitch	38	°C/W

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