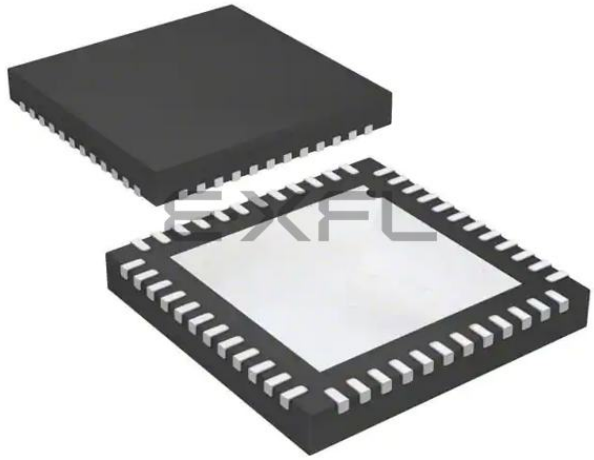

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	BLDC Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32kB)
Controller Series	STM32F031x6x7
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART
Number of I/O	16
Voltage - Supply	8V ~ 45V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stspin32f0

1 Description

The STSPIN32F0 is a System-In-Package providing an integrated solution suitable for driving three-phase BLDC motors using different driving modes.

It embeds a triple half-bridge gate driver able to drive power MOSFETs or IGBTs with a current capability of 600 mA (sink and source). The high- and low-side switches of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

An internal DC/DC buck converter provides the 3.3 V voltage suitable to supply both the MCU and external components. An internal LDO linear regulator provides the supply voltage for gate drivers.

The integrated operational amplifiers are available for the signal conditioning of the analog Hall-effect sensors and the shunt resistor signal.

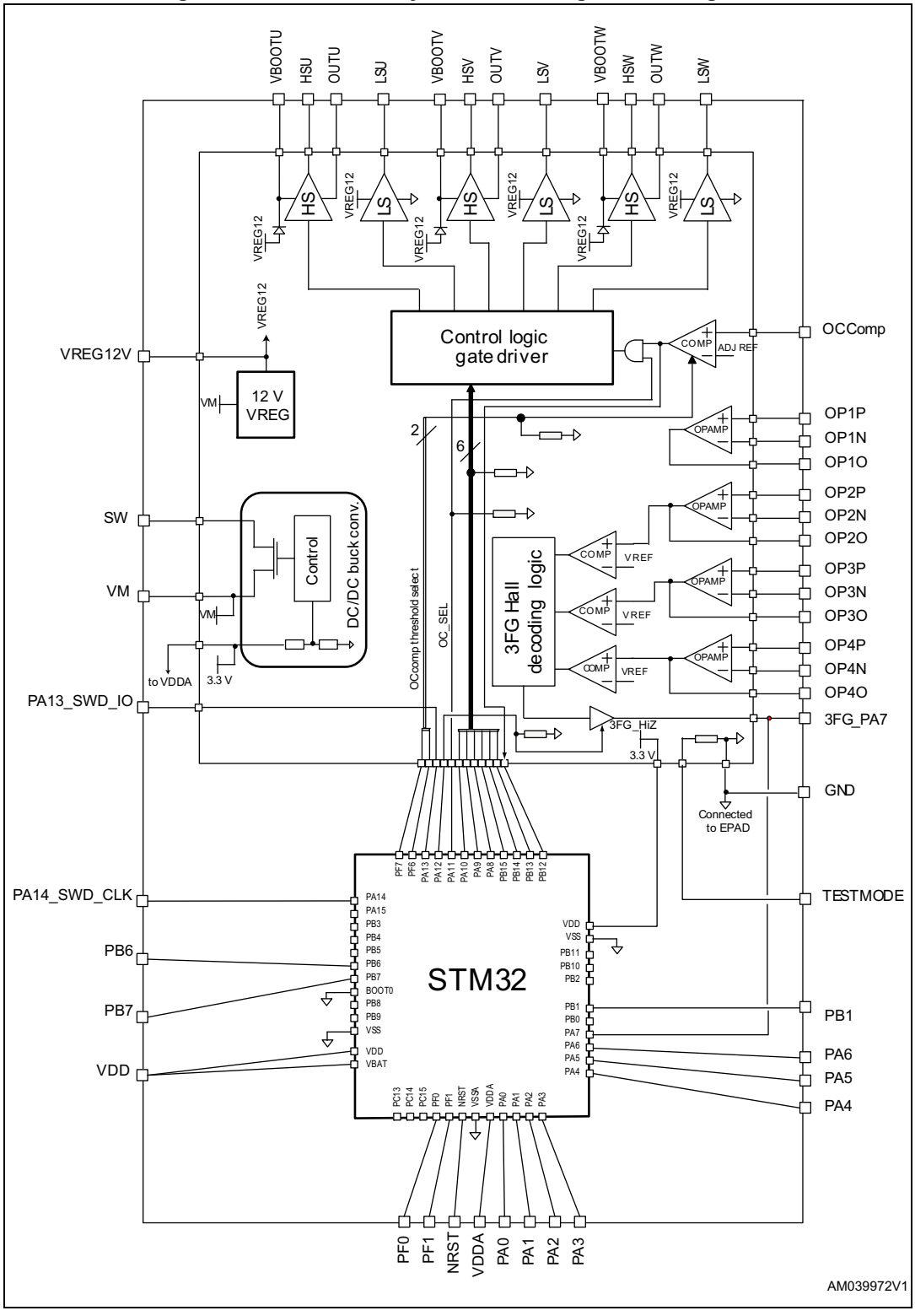
A comparator with a programmable threshold is integrated to perform the overcurrent protection.

The integrated MCU (STM32F031C6 with extended temperature range, suffix 7 version) allows performing field-oriented control, the 6-step sensorless and other advanced driving algorithm including the speed control loop. It has the write-protection and read-protection feature for the embedded Flash memory to protect against unwanted writing and/or reading.

The STSPIN32F0 device also features overtemperature and undervoltage lockout protections and can be put in the standby mode to reduce the power consumption. The device provides 16 general-purpose I/O ports (GPIO) with the 5 V tolerant capability, one 12-bit analog-to-digital converter with up to 9 channels performing conversions in a single-shot or scan modes, 5 synchronizable general-purpose timers and supports an easy to use debugging serial interface (SWD).

2 Block diagrams

Figure 1. STSPIN32F0 System-In-Package block diagram



3.2 ESD protections

Table 2. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V

3.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Power supply voltage	-	8(1)	-	45	V
dV_M/dt	Power supply voltage slope	V_M = 45 V	-	-	0.75	V/µs
V_{DDA}	DC/DC regulator output voltage	-	-	3.3	-	V
L_{SW}	Output inductance	-	-	22	-	µH
C_{DDA}	Output capacitance	-	47	-	-	µF
ESR_{DDA}	Output capacitor ESR	-	-	-	200	mΩ
V_{REG12}	Linear regulator output and gate driver supply voltage	13 < V_M < 45 V	-	12	-	V
		Shorted to VM	8(1)	-	15	
C_{REG}	Load capacitance	-	1	10	-	µF
ESR_{REG}	ESR load capacitance	-	-	-	1.2	Ω
V_{BO}	Floating supply voltage(2)	-	-	V_{REG12} - 1	15	V
V_{CP}	Comparator input voltage	-	0	-	1	V
T_j	Operating junction temperature	Analog IC	-40	-	125	°C
		MCU(3)	-40	-	125	°C

1. UVLO threshold V_{Mon_max}.
2. $V_{BO} = V_{BOOT} - V_{OUT}$.
3. See the STM32F031C6 datasheet (suffix 7 version).

3.4 Thermal data

Table 4. Thermal data(1)

Symbol	Parameter	Value	Unit
$R_{th\ (JA)}$	Thermal resistance junction to ambient	45.6	°C/W

1. Calculated by simulation with following boundary condition. The 2s2p board as per the std. JEDEC (JESD51-7) in natural convection. Board dimensions: 114.3 x 76.2 x 1.6 mm. Ambient temperature: 25 °C.

4 Electrical characteristics

Testing conditions: V_M = 15 V; V_{DD} = 3.3 V, unless otherwise specified.

Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power supply and standby mode						
I_M	V_M current consumption	V_M = 45 V; V_{DD} = 3.5 V externally supplied	-	2	2.6	mA
		Standby PF7 = '0' PF6 = '0 V_M = 45 V;V_{DD} = 3.5 V externally supplied	-	880	1100	µA
V_{MOn}	V_M UVLO turn-on threshold	V_M rising from 0 V	7.0	7.4	7.8	V
V_{MOff}	V_M UVLO turn-off threshold	V_M falling from 8 V	6.7	7.1	7.5	V
V_{MHys}	V_M UVLO threshold hysteresis	-	-	0.3	-	V
I_{DD}	V_{DD} current consumption	V_{DD} = 3.5 V externally supplied(1)	-	2.5	5	mA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	2.5	5	
I_{DDA}	V_{DDA} current consumption	V_{DD} = 3.5 V externally supplied(1)	-	615	750	µA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	80	125	
V_{DDOn}	V_{DD} UVLO turn-on threshold	V_{DD} rising from 0 V	2.5	2.65	2.8	V
V_{DDOff}	V_{DD} UVLO turn-off threshold	V_{DD} falling from 3.3 V	2.2	2.35	2.5	V
V_{DDHys}	V_{DD} UVLO threshold hysteresis	-	-	0.3	-	V
I_{REG12}	V_{REG} current consumption	V_{REG} = 13 V externally supplied, V_M = 45 V; no commutation	-	800	1200	µA
		Standby PF7 = '0' PF6 = '0' V_{REG} = 13 V externally supplied	-	800	1200	
$V_{REG12On}$	V_{REG12} UVLO turn-on threshold	V_{REG12} rising from 0 V	6.7	7.1	7.5	V
$V_{REG12Off}$	V_{REG12} UVLO turn-off threshold	V_{REG12} falling from 8 V	6.4	6.8	7.2	V
$V_{REG12Hys}$	V_{REG12} UVLO threshold hysteresis	-	-	0.25	-	V
I_{BOOT}	V_{BO} current consumption	HS on V_{BO} = 13 V	-	200	290	µA
V_{BOOn}	V_{BO} UVLO turn-on threshold	V_{BO} rising from 0 V	5.7	6.1	6.5	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Thermal protection						
T_{SD}	Thermal shut-down temperature	-	130	140	150	°C
T_{hys}	Thermal shut-down hysteresis	-	20	30	40	°C

1. The current consumption depends on the firmware loaded in the microcontroller.
2. UVLO threshold V_{Mon_max}.
3. Using the 47 µF capacitor (APXG250ARA470MF61G), 22 µH inductor (MLF1608C220KTA00), and diode 1N4448TR.
4. With 11 < V_M < 13 V the linear output voltage can be VREG12 or 'VM-VREG12,drop' depending on the linear regulator is already turned-on or not.
5. *Figure 3*.
6. MT = max. ($|t_{on(LVG)} - t_{off(LVG)}|$, $|t_{on(HVG)} - t_{off(HVG)}|$, $|t_{off(LVG)} - t_{on(HVG)}|$, $|t_{off(HVG)} - t_{on(LVG)}|$).
7. Guaranteed by design.
8. Guaranteed by I_{OUT} test.
9. See *Figure 16 on page 31*.
10. 3FG circuitry enabled. The parameter is measured on the active open-drain edge (falling edge).

Figure 3. Gate drivers timing

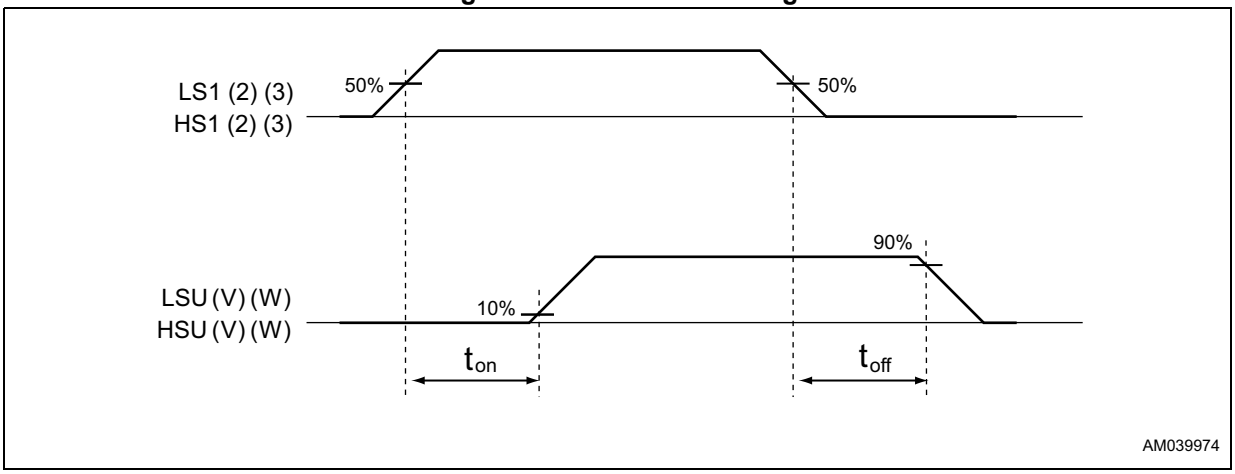


Table 7. STSPIN32F0 MCU pad mapping (continued)

MCU pad	Type	Analog IC pad	Alternate and additional functions
PB13	I/O - FT	LS1	TIM1_CH1N(1)
PB14	I/O - FT	LS2	TIM1_CH2N(1)
PB15	I/O - FT	LS3	TIM1_CH3N(1)
PA8	I/O - FT	HS1	TIM1_CH1(1)
PA9	I/O - FTf	HS2	TIM1_CH2(1)
PA10	I/O - FTf	HS3	TIM1_CH3
PA11	I/O - FT	OC_SEL	Push-pull output(1)
PA12	I/O - FT	3FG_HIZ	Push-pull output(1)
PA13_SWD_IO	I/O - FT	SWDIO_INT	IR_OUT, SWDIO
PF6	I/O - FTf	OC_TH_STBY2	Push-pull output(1)
PF7	I/O - FTf	OC_TH_STBY1	Push-pull output(1)
PA14_SWD_CLK	I/O - FT	-	USART1_TX, SWCLK
PB6	I/O - FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N
PB7	I/O - FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N
VBAT, VDD	S	VDD	Backup and digital power supply
VSS, VSSA	S	-	Ground
BOOT0	I	-	Boot memory selection (internally connected to ground)
PC13, PC14, PC15, PB0, PB2, PB10, PB11, PA15, PB3, PB4, PB5, PB8, PB9	-	-	Not connected

1. The analog IC is designed to support these GPIOs configuration only. Different configuration could cause device malfunctioning. The GPIO input configuration without pull-up or pull-down is always allowed.

Note: Each unused GPIO inside the SiP should be configured in the OUTPUT mode low level after the startup by software.

Table 8. STSPIN32F0 analog IC pad description (continued)

Pinout name	Pad name	Type	Function
-	OC_COMP_INT	Digital out	OC comparator output
-	HS1	Digital in	High-side input driver U
-	HS2	Digital in	High-side input driver V
-	HS3	Digital in	High-side input driver W
-	LS1	Digital in	Low-side input driver U
-	LS2	Digital in	Low-side input driver V
-	LS3	Digital in	Low-side input driver W
-	OC_SEL	Digital in	OC protection selection
-	3FG_HIZ	Digital in	3FG output enable
-	SWD_IO_INT	Digital in	System debug data (connected to the output through the analog IC)
-	OC_TH_STBY1	Digital in	Overcurrent threshold selection and standby input 1
-	OC_TH_STBY2	Digital in	Overcurrent threshold selection and standby input 2

If the failure event occurs on the SW pin and the I_{OVC} threshold is reached the regulator is latched off. To restart the DC/DC regulator a power-down and power-up cycle of device supply voltage (V_M) is mandatory.

If the failure event occurs on the regulator output (VDDA pin) and the voltage goes below the UVLO threshold (V_{DDOff}), the regulator restarts with a new soft-start sequence until the OC condition is removed. In this case the current in the coil is limited by $I_{SW.peak}$.

The DC/DC regulator embeds a thermal protection as described in *Section 6.1.2*.

Figure 7. DC/DC buck regulator topology

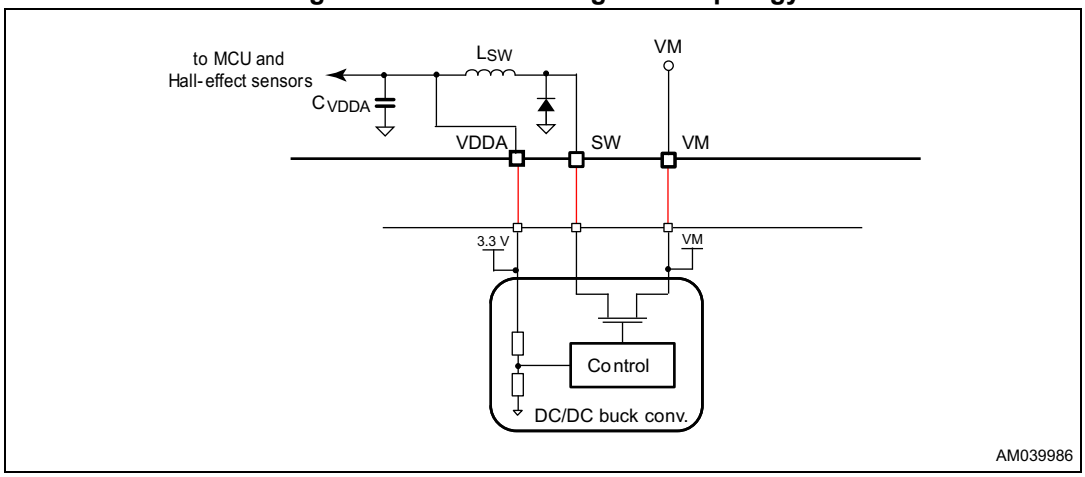
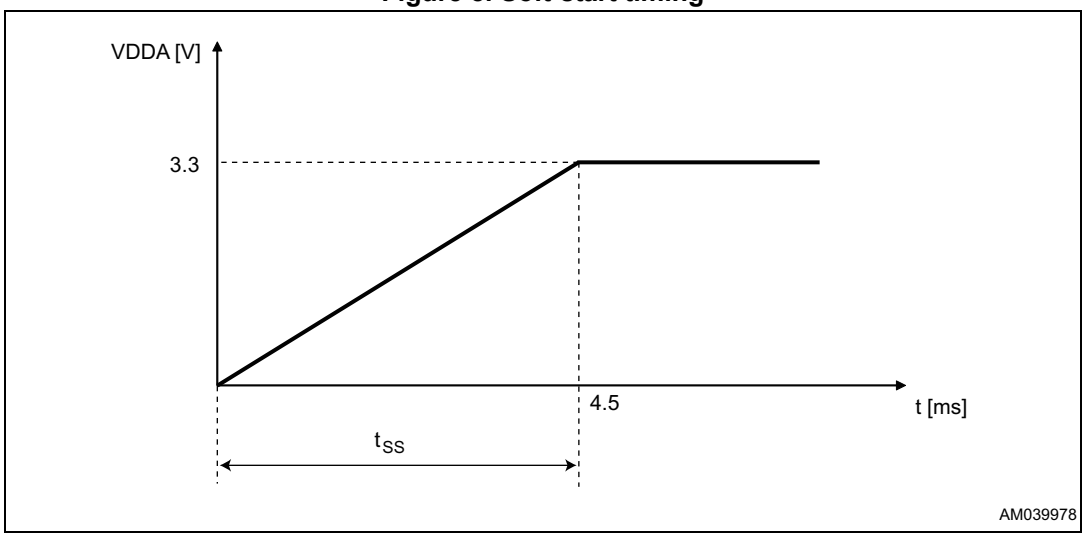


Figure 8. Soft-start timing



External optional 3.3 V supply voltage

It is possible provide externally the 3.3 V supply voltage directly on the VDDA pin. In this case, there are two possible configurations:

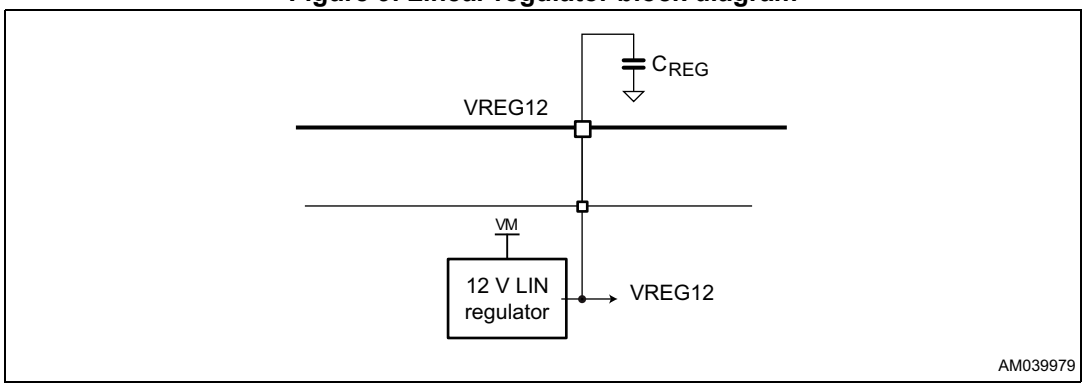
1. The SW pin floating or shorted to VM: in this case the internal power switch of the DC/DC converter continues to switch on/off according to the internal clock
2. The SW pin shorted to GND or VDD: in this case the internal power switch detects a short-circuit and it is latched off.

Note: It is not allowed to apply VDD voltage externally in case of VM < VDD.

6.3 Linear regulator

The internal 12 V linear regulator is a LDO regulator providing the supply voltage for the gate drivers section. An external capacitor connected to the VREG12 pin is required.

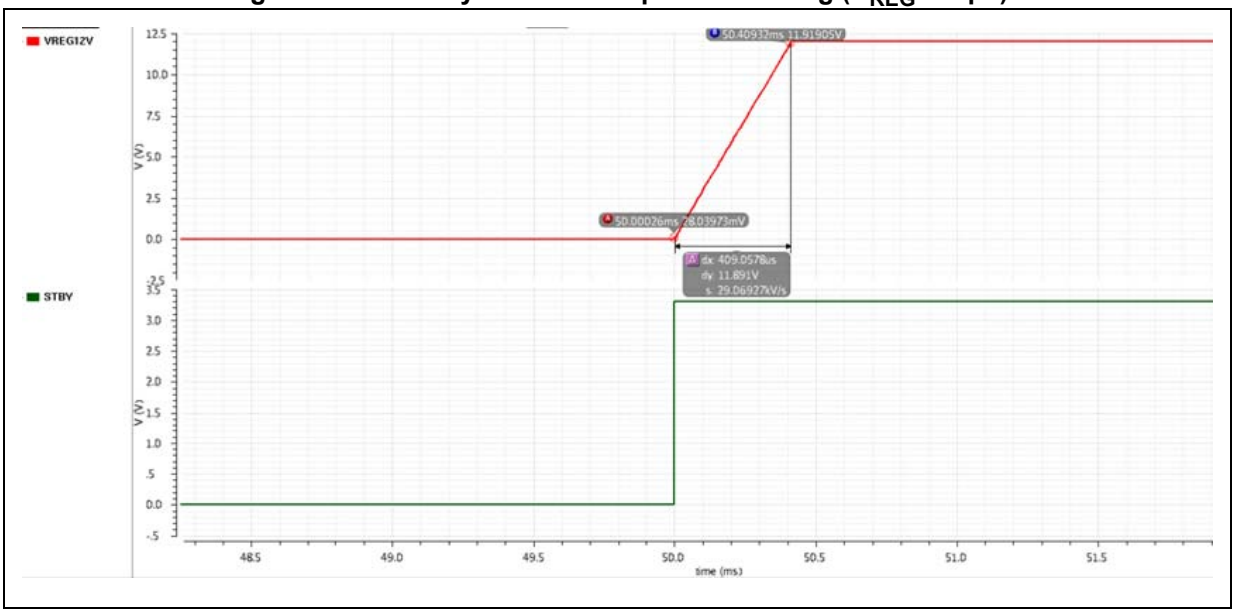
Figure 9. Linear regulator block diagram



When the VM voltage is below to 12 V, the VM pin and the linear regulator output can be shorted together providing the gate driver supply externally.

The linear regulator embeds a thermal protection as described in *Section 6.1.2*.

Figure 11. “Standby to normal” operation timing (C_{REG} = 1 µF)



Equation 1

$$t_{REG} = \frac{C_{REG} \times V_{REG12}}{I_{REG12,\,lim}}$$

6.5 Gate drivers

The STSPIN32F0 device integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs or IGBTs. The high-side section is supplied by a bootstrapped voltage technique with an integrated bootstrap diode.

All the input lines (refer to *Figure 2: Analog IC block diagram on page 6*) are connected to a pull-down resistor (60 kΩ typical value) to guarantee the low logic level during the device start-up.

The high- and low-side outputs of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

Note: All the input lines of the analog IC have an internal pull-down to guarantee the low logic level during the device start-up and when the MCU lines are not present.

6.6 Microcontroller unit

The integrated MCU is the STM32F031C6 with following main characteristics:

- Core: ARM® 32-bit Cortex™-M0 CPU, frequency up to 48 MHz
- Memories: 4kB of SRAM, 32 kB of Flash memory
- CRC calculation unit
- Up to 16 fast I/Os
- Advanced-control timer dedicated for PWM generation
- Up to 5 general purpose timers
- 12-bit ADC (up to 9 channels)
- Communication interfaces: I^2C, USART, SPI
- Serial wire debug (SWD)
- Extended temperature range: -40 to 125 °C

For more details refer to the STM32F031C6 datasheet on www.st.com

6.6.1 Memories and boot mode

The device has the following features:

- 4 Kbytes of the embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with an exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 Kbytes of the embedded Flash memory for programs and data
  - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or the boot in the RAM is selected
- Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and the boot in the RAM selection disabled.

At the startup the boot is made from the main Flash memory due to the BOOT0 MCU input internally connected to ground (see *Table 7 on page 15*). The main Flash memory is aliased in the boot memory space (0x00000000), but still accessible from its original memory space (0x08000000). In other words, the Flash memory contents can be accessed starting from the address 0x00000000 or 0x08000000.

The embedded boot loader is located in the system memory, programmed by ST during production.

6.6.2 Power management

The VDD pin is the power supply for the I/Os and the internal regulator.

The VDDA pin is the power supply for the ADC, reset blocks, RCs and PLL. The V_{DDA} voltage can be generated through the internal DC/DC buck converter, otherwise it is possible to provide externally the supply voltage directly on the VDDA pin.

Note: ***The VDDA voltage level must be always greater or equal to the VDD voltage level and must be established first.***

The MCU has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in the reset mode when the monitored supply voltage is below a specified threshold.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The MCU supports three low-power modes to achieve the best compromise between low-power consumption, short start-up time and available wake-up sources:

- **Sleep mode**
  In the sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake-up the CPU when an interrupt/event occurs.
- **Stop mode**
  The stop mode achieves very low-power consumption while retaining the content of the SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in the normal or in the low-power mode.
  The device can be woken-up from the stop mode by any of the EXTI lines (one of the 16 external lines, the PVD output, RTC, I^2C1 or USART1).
- **Standby mode**
  The standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering the standby mode, SRAM and register contents are lost except for registers in the RTC domain and standby circuitry.
  The device exits the standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

6.6.3 High-speed external clock source

The high-speed external (HSE) clock can be generated from the external clock signal or supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator (see *Figure 13*).

The external clock signal has to respect the I/O characteristics and follows the recommended clock input waveform (refer to *Figure 12*).

Figure 12. HSE clock source timing diagram

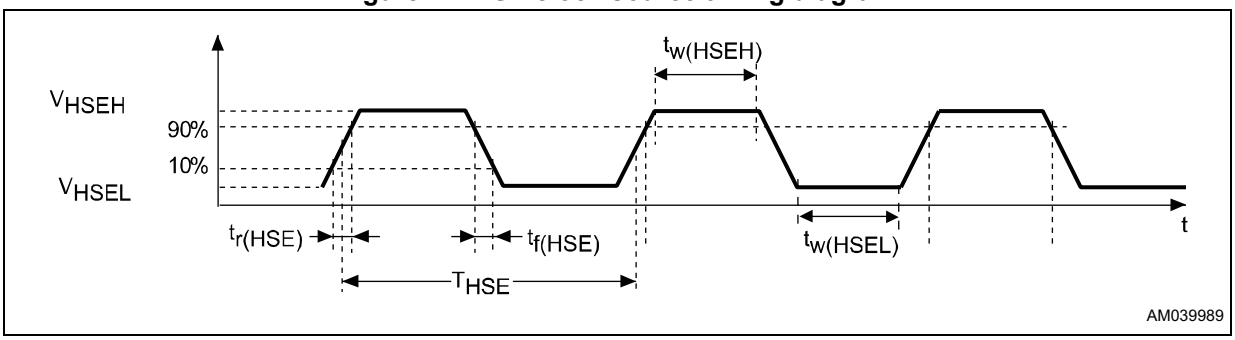
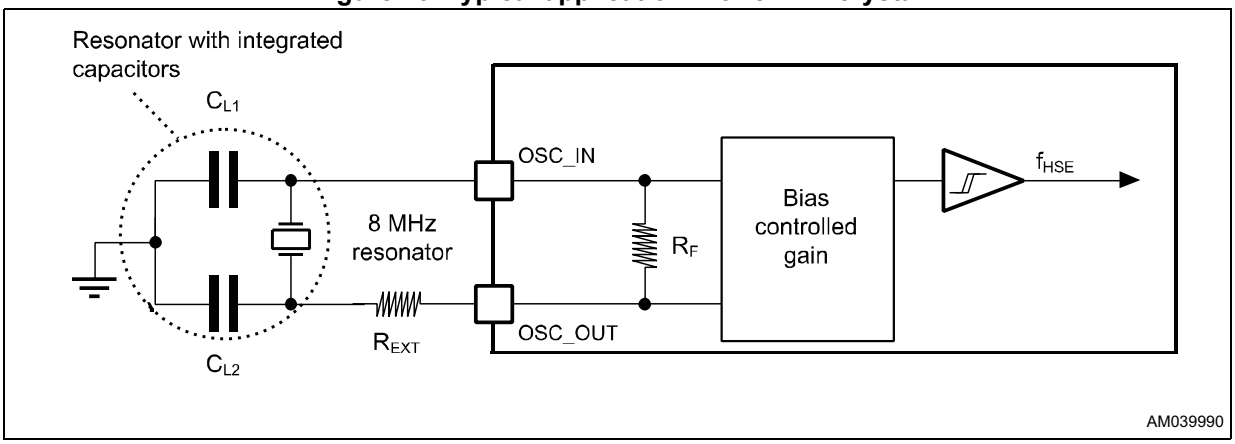


Figure 13. Typical application with 8 MHz crystal



In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The R_{EXT} value depends on the crystal characteristics (refer to the crystal resonator manufacturer for more details on them).

Figure 15. Comparator

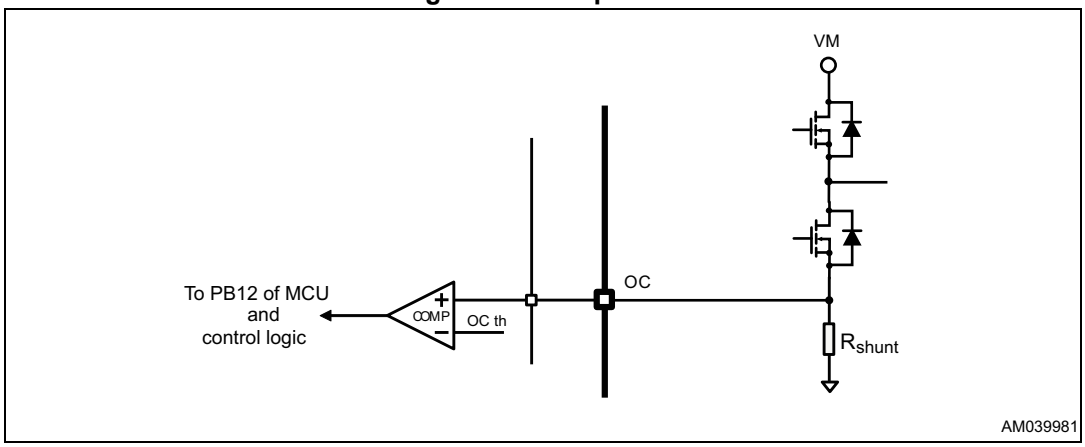


Table 11. OC protection selection

OC_SEL (PA11)	Function
0	OC comparator output signal is visible only to MCU (default)
1	OC comparator output signal is visible to MCU and also acts on gate driver control logic

Table 12. OC threshold values

OC_TH_STBY2 (PF6)	OC_TH_STBY1 (PF7)	OC threshold [mV]	Note
0	0	N.A.	Standby mode (see *Section 6.4 on page 23*)
0	1	100	-
1	0	250	-
1	1	500	-

When the overcurrent condition disappears, the latched overcurrent signal is released only after all the high-side outputs are kept low for at least $t_{OCrelease}$ time. (Refer to *Figure 16*).

Figure 17. 3FG circuitry

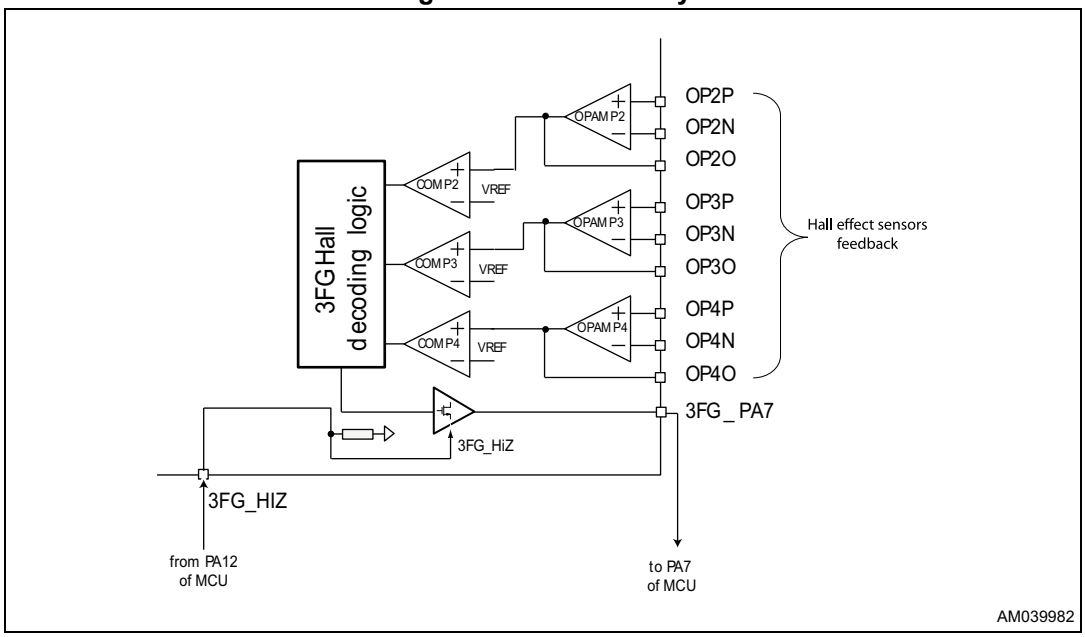
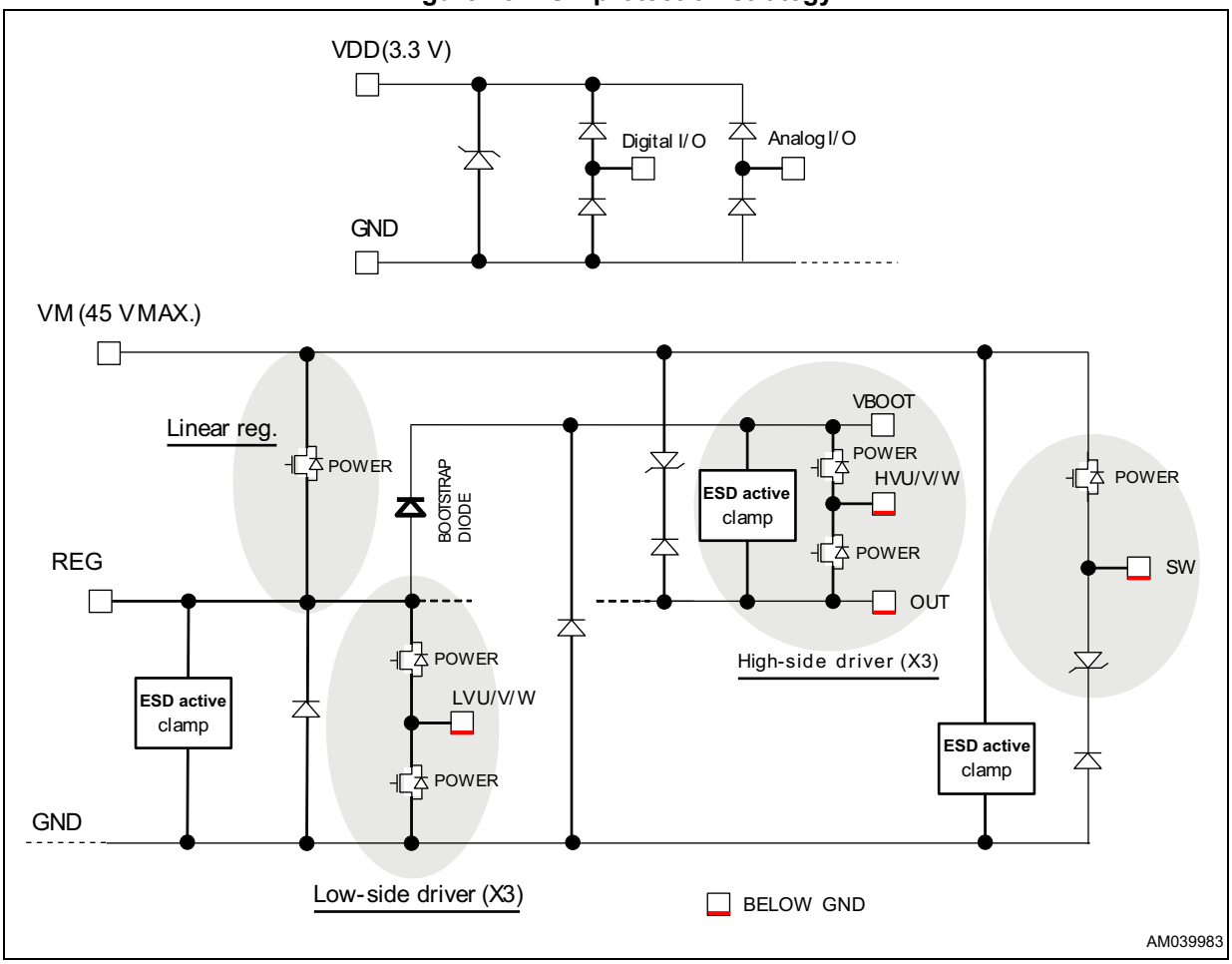


Table 14. 3FG output truth table (refer to *Figure 17*)

COMP4 output	COMP3 output	COMP2 output	3FG pin (PA7)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

6.11 ESD protection strategy

Figure 18. ESD protection strategy

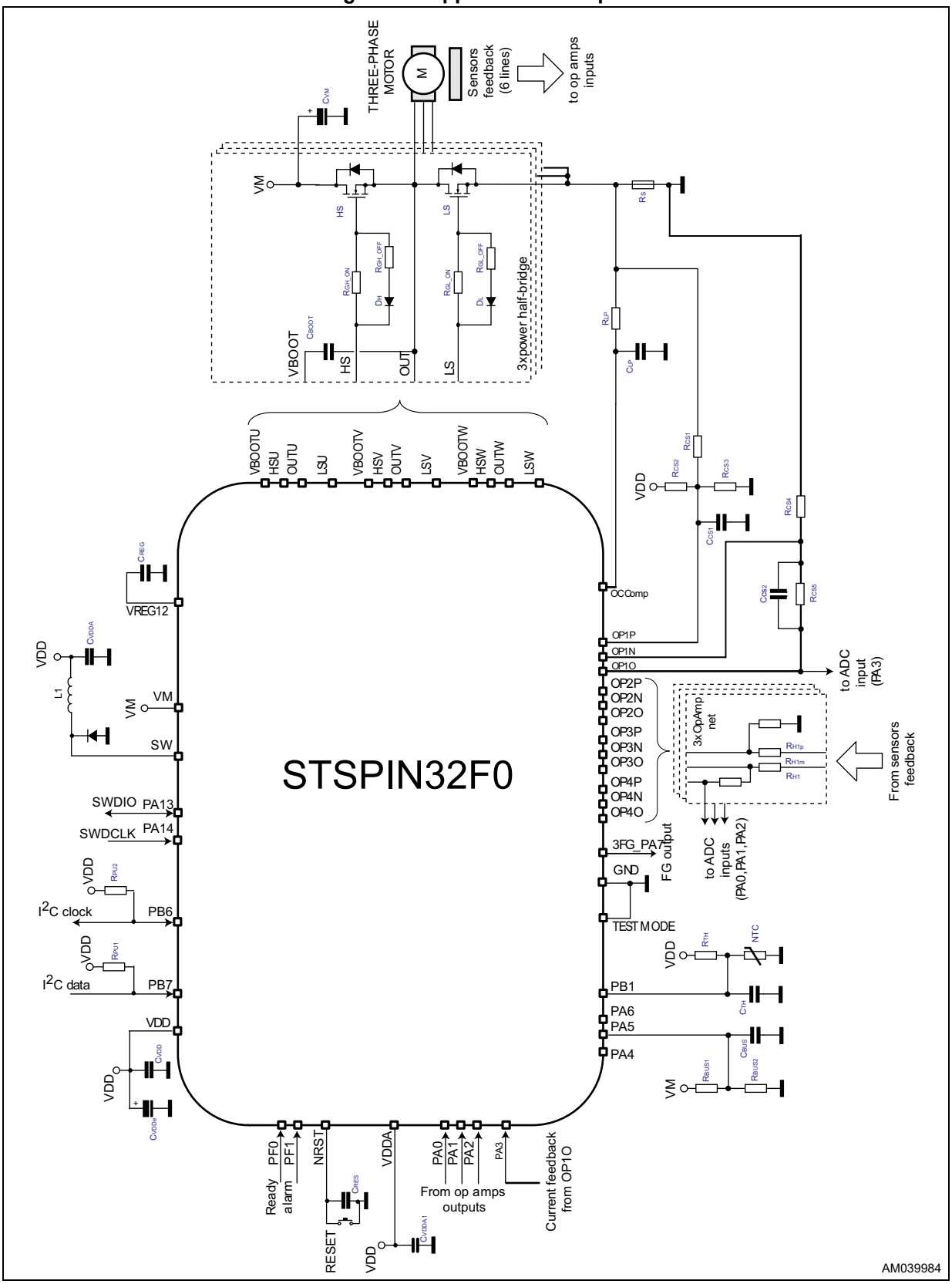


7 Application example

Figure 19 shows an application example using the STSPIN32F0 device to drive a three-phase motor with single shunt configuration and analog Hall-effect sensors feedback. The others features implemented are:

- VDD (3.3 V) power supply internally generated via DC/DC regulator
- VREG12 (12 V) power supply internally generated via LDO linear regulator
- I^2C serial interface (PB6 and PB7)
- Serial wire debug ports (PA13_SWD_IO, PA14_SWD_CLK)
- Ready and alarm lines (PF0, PF1)
- Reset dedicated pin
- Overcurrent protection using internal comparator
- Current sensing using internal operation amplifier (op amp 1) and ADC (PA3)
- 3FG generation using internal op amps, comparators and Hall decoding logic circuitry (op amp2, 3, 4 and relative comparators)
- Hall-effect sensors feedback management with op amps and ADC (op amp2, 3, 4 and PA0, PA1, PA2)
- Bus voltage compensation using internal ADC (PA4)
- Application temperature monitoring using internal ADC (PB1)

Figure 19. Application example



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

A customized VFQFPN48 7 x 7 package is proposed. A smaller EPAD, internally connected to the ground pin, is desired to place through holes on the bottom of the package.

Lead plating is Nickel/Palladium/Gold (Ni/Pd/Au).