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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

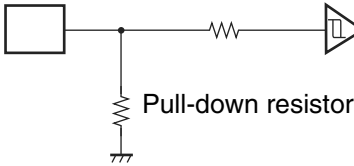
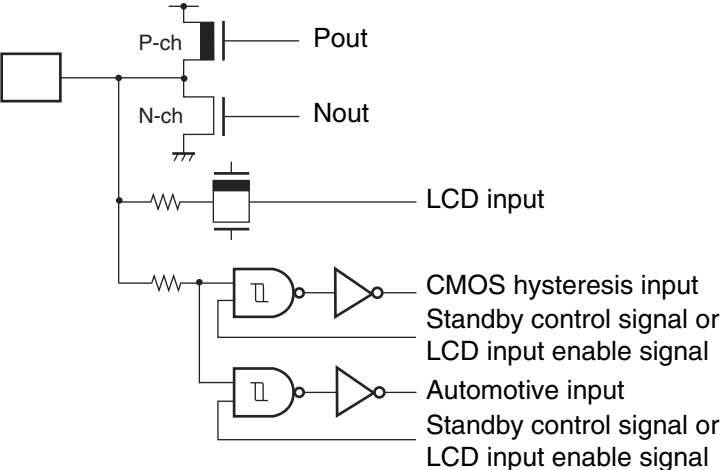
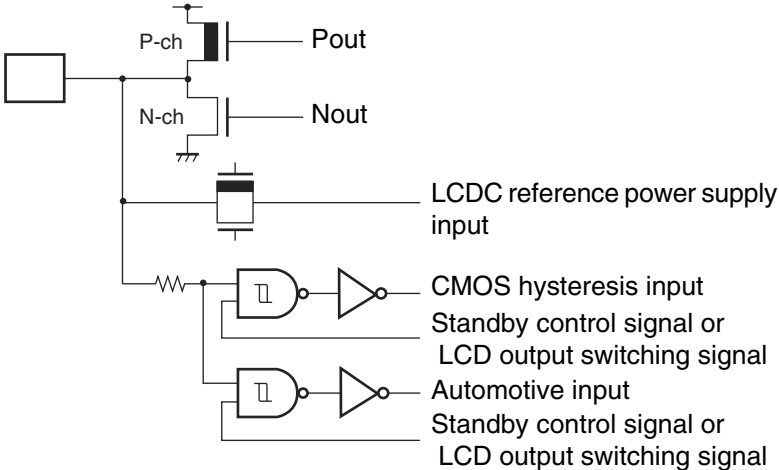
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-115e1

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Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μ F capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

Type	Circuit	Remarks
E	 Pull-down resistor CMOS hysteresis input	Input-only pin (with pull-down resistance) - Attached pull-down resistance: approx. 50 kΩ - CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Note: The MD2 pin of the evaluation products uses this circuit type.
F	 P-ch Pout N-ch Nout LCD input CMOS hysteresis input Standby control signal or LCD input enable signal Automotive input Standby control signal or LCD input enable signal	LCD output common general-purpose port - CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) - Hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) - Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
G	 P-ch Pout N-ch Nout LCDC reference power supply input CMOS hysteresis input Standby control signal or LCD output switching signal Automotive input Standby control signal or LCD output switching signal	LCDC reference power supply common general-purpose port - CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) - CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) - Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)

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- **Serial communication**

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H , 00000B _H	(Disabled)				
00000C _H	Port C data register	PDRC	R/W	Port C	XXXXXXXX _B
00000D _H	Port D data register	PDRD	R/W	Port D	XXXXXXXX _B
00000E _H	Port E data register	PDRE	R/W	Port E	XXXXXXXX _B
00000F _H	(Disabled)				
000010 _H	Port 0 direction register	DDR0	R/W	Port 0	00000000 _B
000011 _H	Port 1 direction register	DDR1	R/W	Port 1	XX000000 _B
000012 _H	Port 2 direction register	DDR2	R/W	Port 2	000000XX _B
000013 _H	Port 3 direction register	DDR3	R/W	Port 3	00000000 _B
000014 _H	Port 4 direction register	DDR4	R/W	Port 4	00000000 _B
000015 _H	Port 5 direction register	DDR5	R/W	Port 5	00000000 _B
000016 _H	Port 6 direction register	DDR6	R/W	Port 6	00000000 _B
000017 _H	Port 7 direction register	DDR7	R/W	Port 7	00000000 _B
000018 _H	Port 8 direction register	DDR8	R/W	Port 8	00000000 _B
000019 _H	Port 9 direction register	DDR9	R/W	Port 9	X0000000 _B
00001A _H	Analog input enable	ADER6	R/W	Port 6, A/D	11111111 _B
00001B _H	(Disabled)				
00001C _H	Port C direction register	DDRC	R/W	Port C	00000000 _B
00001D _H	Port D direction register	DDRD	R/W	Port D	X0000000 _B
00001E _H	Port E direction register	DDRE	R/W	Port E	XXXXX000 _B
00001F _H	(Disabled)				
000020 _H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0 _B
000021 _H	Higher A/D control status register	ADCS1	R/W		0000000X _B
000022 _H	Lower A/D control status register	ADCR0	R		00000000 _B
000023 _H	Higher A/D data register	ADCR1	R		XXXXXX00 _B

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MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024 _H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXX _B
000025 _H			R/W		XXXXXXXX _B
000026 _H	Timer data register	TCDT	R/W		00000000 _B
000027 _H			R/W		00000000 _B
000028 _H	Lower timer control status register	TCCSL	R/W		00000000 _B
000029 _H	Higher timer control status register	TCCSH	R/W		01-00000 _B
00002A _H	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000 _B
00002B _H	Higher PPG0 control status register	PCNTH0	R/W		00000001 _B
00002C _H	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000 _B
00002D _H	Higher PPG1 control status register	PCNTH1	R/W		00000001 _B
00002E _H	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000 _B
00002F _H	Higher PPG2 control status register	PCNTH2	R/W		00000001 _B
000030 _H	External interrupt enable	ENIR	R/W	External interrupt	00000000 _B
000031 _H	External interrupt request	EIRR	R/W		00000000 _B
000032 _H	Lower external interrupt level	ELVRL	R/W		00000000 _B
000033 _H	Higher external interrupt level	ELVRH	R/W		00000000 _B
000034 _H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000 _B
000035 _H	Serial control register 0	SCR0	R/W, W		00000000 _B
000036 _H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000 _B
000037 _H	Serial status register 0	SSR0	R/W, R		00001000 _B
000038 _H	Extended communication control register 0	ECCR0	R/W, R		000000XX _B
000039 _H	Extended status control register 0	ESCR0	R/W		00000100 _B
00003A _H	Baud rate generator register 00	BGR00	R/W		00000000 _B
00003B _H	Baud rate generator register 01	BGR01	R/W, R		00000000 _B
00003C _H to 00003F _H	(Disabled)				
000040 _H to 00004F _H	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
000050 _H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000 _B
000051 _H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000 _B
000052 _H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
000053 _H					XXXXXXXX _B

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MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
000083 _H	(Disabled)				
000084 _H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	000000X0 _B
000085 _H	(Disabled)				
000086 _H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	000000X0 _B
000087 _H	(Disabled)				
000088 _H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXXX111 _B
000089 _H	(Disabled)				
00008A _H	A/D setting register 0	ADSR0	R/W	A/D converter	00000000 _B
00008B _H	A/D setting register 1	ADSR1	R/W		00000000 _B
00008C _H	Port input level select 0	PIL0	R/W	Port input level select	00000000 _B
00008D _H	Port input level select 1	PIL1	R/W		XXXX0000 _B
00008E _H	Port input level select 2	PIL2	R/W		XXXX0000 _B
00008F _H to 00009D _H	(Disabled)				
00009E _H	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0X _B
00009F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	XXXXXXXX0 _B
0000A0 _H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000 _B
0000A1 _H	Clock select register	CKSCR	R/W, R		11111100 _B
0000A2 _H to 0000A7 _H	(Disabled)				
0000A8 _H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXXX111 _B
0000A9 _H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100 _B
0000AA _H	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000 _B
0000AB _H to 0000AD _H	(Disabled)				
0000AE _H	Flash memory control status register	FMCS	R/W	Flash interface	000X0000 _B
0000AF _H	(Disabled)				

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111 _B
0000B1 _H	Interrupt control register 01	ICR01	R/W		00000111 _B
0000B2 _H	Interrupt control register 02	ICR02	R/W		00000111 _B
0000B3 _H	Interrupt control register 03	ICR03	R/W		00000111 _B
0000B4 _H	Interrupt control register 04	ICR04	R/W		00000111 _B
0000B5 _H	Interrupt control register 05	ICR05	R/W		00000111 _B
0000B6 _H	Interrupt control register 06	ICR06	R/W		00000111 _B
0000B7 _H	Interrupt control register 07	ICR07	R/W		00000111 _B
0000B8 _H	Interrupt control register 08	ICR08	R/W		00000111 _B
0000B9 _H	Interrupt control register 09	ICR09	R/W		00000111 _B
0000BA _H	Interrupt control register 10	ICR10	R/W		00000111 _B
0000BB _H	Interrupt control register 11	ICR11	R/W		00000111 _B
0000BC _H	Interrupt control register 12	ICR12	R/W		00000111 _B
0000BD _H	Interrupt control register 13	ICR13	R/W		00000111 _B
0000BE _H	Interrupt control register 14	ICR14	R/W		00000111 _B
0000BF _H	Interrupt control register 15	ICR15	R/W		00000111 _B
0000C0 _H to 0000C3 _H	(Disabled)				
0000C4 _H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000 _B
0000C5 _H	Serial control register 1	SCR1	R/W, W		00000000 _B
0000C6 _H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000 _B
0000C7 _H	Serial status register 1	SSR1	R/W, R		00001000 _B
0000C8 _H	Extended communication control register 1	ECCR1	R/W, R		000000XX _B
0000C9 _H	Extended status control register 1	ESCR1	R/W		00000100 _B
0000CA _H	Baud rate generator register 10	BGR10	R/W		00000000 _B
0000CB _H	Baud rate generator register 11	BGR11	R/W, R		00000000 _B
0000CC _H	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0 _B
0000CD _H	Middle watch timer control register	WTCRM	R/W		00000000 _B
0000CE _H	Higher watch timer control register	WTCRH	R/W		XXXXXX00 _B
0000CF _H	Sub clock control register	PSCCR	W	Sub clock	XXXX0000 _B
0000D0 _H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000 _B
0000D1 _H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXXX _B
0000D2 _H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000 _B
0000D3 _H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XX _B

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MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000D4 _H	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000 _B
0000D5 _H	Higher timer control status register 2	TMCSR2H	R/W		XXX10000 _B
0000D6 _H	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000 _B
0000D7 _H	Higher timer control status register 3	TMCSR3H	R/W		XXX10000 _B
0000D8 _H	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000 _B
0000D9 _H	Higher sound control register 1	SGCRH1	R/W		0XXXX100 _B
0000DA _H	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000 _B
0000DB _H	Higher PPG3 control status register	PCNTH3	R/W		00000001 _B
0000DC _H	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000 _B
0000DD _H	Higher PPG4 control status register	PCNTH4	R/W		00000001 _B
0000DE _H	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000 _B
0000DF _H	Higher PPG5 control status register	PCNTH5	R/W		00000001 _B
0000E0 _H	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000 _B
0000E1 _H	Serial control register 2	SCR2	R/W, W		00000000 _B
0000E2 _H	Reception/transmission data register 2	RDR2/ TDR2	R/W		00000000 _B
0000E3 _H	Serial status register 2	SSR2	R/W, R		00001000 _B
0000E4 _H	Extended communication control register 2	ECCR2	R/W, R		000000XX _B
0000E5 _H	Extended status control register 2	ESCR2	R/W		00000100 _B
0000E6 _H	Baud rate generator register 20	BGR20	R/W		00000000 _B
0000E7 _H	Baud rate generator register 21	BGR21	R/W, R		00000000 _B
0000E8 _H	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000 _B
0000E9 _H	Serial control register 3	SCR3	R/W, W		00000000 _B
0000EA _H	Reception/transmission data register 3	RDR3/ TDR3	R/W		00000000 _B
0000EB _H	Serial status register 3	SSR3	R/W, R		00001000 _B
0000EC _H	Extended communication control register 3	ECCR3	R/W, R		000000XX _B
0000ED _H	Extended status control register 3	ESCR3	R/W		00000100 _B
0000EE _H	Baud rate generator register 30	BGR30	R/W		00000000 _B
0000EF _H	Baud rate generator register 31	BGR31	R/W, R		00000000 _B
001FF0 _H	Program address detection register 0	PADR0	R/W	Address match detection	XXXXXXXX _B
001FF1 _H	Program address detection register 1	PADR0	R/W		XXXXXXXX _B
001FF2 _H	Program address detection register 2	PADR0	R/W		XXXXXXXX _B
001FF3 _H	Program address detection register 3	PADR1	R/W		XXXXXXXX _B
001FF4 _H	Program address detection register 4	PADR1	R/W		XXXXXXXX _B
001FF5 _H	Program address detection register 5	PADR1	R/W		XXXXXXXX _B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003970 _H to 003973 _H	(Disabled)				
003974 _H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXX _B
003975 _H	Amplitude data register 1	SGAR1	R/W		00000000 _B
003976 _H	Decrement grade register 1	SGDR1	R/W		XXXXXXXX _B
003977 _H	Tone count register 1	SGTR1	R/W		XXXXXXXX _B
003978 _H to 00397F _H	(Disabled)				
003980 _H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXX _B
003981 _H					XXXXXXXX _B
003982 _H	PWM2 compare register 0	PWC20	R/W		XXXXXXXX _B
003983 _H					XXXXXXXX _B
003984 _H	PWM1 select register 0	PWS10	R/W		00000000 _B
003985 _H	PWM2 select register 0	PWS20	R/W		X0000000 _B
003986 _H , 003987 _H	(Disabled)				
003988 _H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXX _B
003989 _H					XXXXXXXX _B
00398A _H	PWM2 compare register 1	PWC21	R/W		XXXXXXXX _B
00398B _H					XXXXXXXX _B
00398C _H	PWM1 select register 1	PWS11	R/W		00000000 _B
00398D _H	PWM2 select register 1	PWS21	R/W		X0000000 _B
00398E _H , 00398F _H	(Disabled)				
003990 _H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXX _B
003991 _H					XXXXXXXX _B
003992 _H	PWM2 compare register 2	PWC22	R/W		XXXXXXXX _B
003993 _H					XXXXXXXX _B
003994 _H	PWM1 select register 2	PWS12	R/W		00000000 _B
003995 _H	PWM2 select register 2	PWS22	R/W		X0000000 _B
003996 _H , 003997 _H	(Disabled)				

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MB90920 Series

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Interrupt source	EI ² OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
UART 1 RX	◎	#37	25 _H	FFFF68 _H	ICR13	0000BD _H *1	High ↑
UART 1 TX	△	#38	26 _H	FFFF64 _H			
UART 0 RX	◎	#39	27 _H	FFFF60 _H	ICR14	0000BE _H *1	↓ Low
UART 0 TX	△	#40	28 _H	FFFF5C _H			
Flash memory status	×	#41	29 _H	FFFF58 _H	ICR15	0000BF _H *1	
Delay interrupt generator module	×	#42	2A _H	FFFF54 _H			

◎ : Usable, and has expanded intelligent I/O services (EI²OS) stop function

○ : Usable

△ : Usable when interrupt sources sharing ICR are not in use

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*1 : • Peripheral functions that share the ICR register have the same interrupt level.

• If the expanded intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.

• When the expanded intelligent I/O service (EI²OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2 : Priority applies when interrupts of the same level are generated.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	AV _{CC} = V _{CC} *2
	AVRH	V _{SS} – 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH*2
	DV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	DV _{CC} = V _{CC} *2
Input voltage*1	V _I	V _{SS} – 0.3	V _{CC} + 0.3	V	*3
Output voltage*1	V _O	V _{SS} – 0.3	V _{CC} + 0.3	V	
Maximum clamp current	I _{CLAMP}	– 4	+ 4	mA	*7
Total maximum clamp current	Σ I _{CLAMP}	—	40	mA	*7
“L” level maximum output current*4	I _{OL1}	—	15	mA	Except P70 to P77 and P80 to P87
	I _{OL2}	—	40	mA	P70 to P77 and P80 to P87
“L” level average output current*5	I _{OLAV1}	—	4	mA	Except P70 to P77 and P80 to P87
	I _{OLAV2}	—	30	mA	P70 to P77 and P80 to P87
“L” level maximum total output current	ΣI _{OL1}	—	100	mA	Except P70 to P77 and P80 to P87
	ΣI _{OL2}	—	330	mA	P70 to P77 and P80 to P87
“L” level average total output current	ΣI _{OLAV1}	—	50	mA	Except P70 to P77 and P80 to P87
	ΣI _{OLAV2}	—	250	mA	P70 to P77 and P80 to P87
“H” level maximum output current	I _{OH1} *4	—	–15	mA	Except P70 to P77 and P80 to P87
	I _{OH2} *4	—	–40	mA	P70 to P77 and P80 to P87
“H” level average output current	I _{OHAV1} *5	—	–4	mA	Except P70 to P77 and P80 to P87
	I _{OHAV2} *5	—	–30	mA	P70 to P77 and P80 to P87
“H” level maximum total output current	ΣI _{OH1}	—	–100	mA	Except P70 to P77 and P80 to P87
	ΣI _{OH2}	—	–330	mA	P70 to P77 and P80 to P87
“H” level average total output current	ΣI _{OHAV1} *6	—	–50	mA	Except P70 to P77 and P80 to P87
	ΣI _{OHAV2} *6	—	–250	mA	P70 to P77 and P80 to P87
Power consumption	P _D	—	625	mW	
Operating temperature	T _A	– 40	+ 105	°C	
Storage temperature	T _{STG}	– 55	+ 150	°C	

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : AV_{CC}, AVRH must not exceed V_{CC}, and AVRH must not exceed AV_{CC}.

When using an evaluation product, DV_{CC} must not exceed V_{CC} (however, DV_{CC} can be set to a higher voltage than V_{CC} when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, I_{CLAMP} is the applicable rating instead of V_I.

*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

(Continued)

MB90920 Series

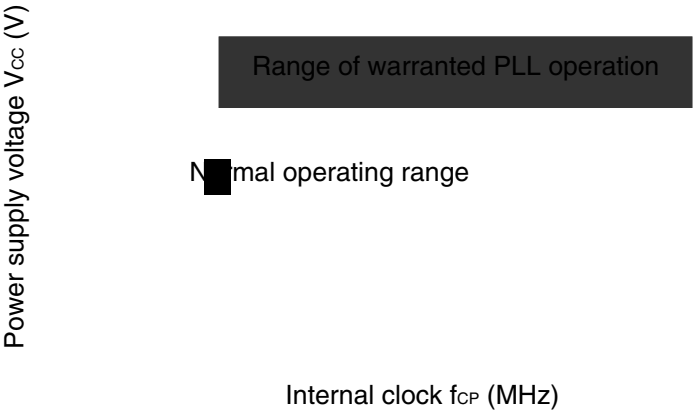
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	$V_{CC} = DV_{CC} = AV_{CC} = 5.5 \text{ V}$, $V_{SS} < V_I < V_{CC}$	—	—	10	μA	
Input capacitance 1	C_{IN1}	All pins except V_{CC} , V_{SS} , DV_{CC} , DV_{SS} , AV_{CC} , AV_{SS} , C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	k Ω	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	k Ω	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -30.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 4.0 \text{ mA}$	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 30.0 \text{ mA}$	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -30.0 \text{ mA}$, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 30.0 \text{ mA}$, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	k Ω	Evaluation product
				8.75	12.5	17.0	k Ω	Flash memory product

(Continued)

• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage



- Notes :
- For PLL 1 × only, use with $t_{CP} = 4$ MHz or greater.
 - Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

(Continued)

(4) UART0/1/2/3 (LIN/SCI)

- Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0 \text{ V} \pm 10 \%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}			0	—	ns
Serial clock “L” pulse width	t _{SLSH}	SCK0 to SCK3	External shift clock mode output pin C _L = 80 pF + 1TTL	3 t _{CP} – t _R	—	ns
Serial clock “H” pulse width	t _{SHSL}			t _{CP} + 10	—	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t _{CP} + 60	ns
Valid SIN → SCK ↑	t _{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXE}			t _{CP} + 30	—	ns
SCK ↓ time	t _F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t _R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.

• Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t _{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXI}			0	—	ns
Serial clock “H” pulse width	t _{SHSL}	SCK0 to SCK3	External shift clock mode output pin C _L = 80 pF + 1TTL	3 t _{CP} – t _R	—	ns
Serial clock “L” pulse width	t _{SLSH}			t _{CP} + 10	—	ns
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t _{CP} + 60	ns
Valid SIN → SCK ↓	t _{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXE}			t _{CP} + 30	—	ns
SCK ↓ time	t _F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t _R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in "MB90920 series hardware manual".

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to "(1) Clock timing".

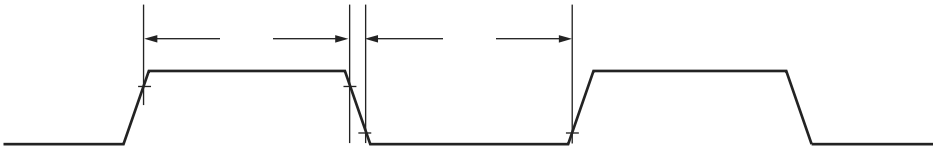
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t _{TIWH} t _{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t _{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

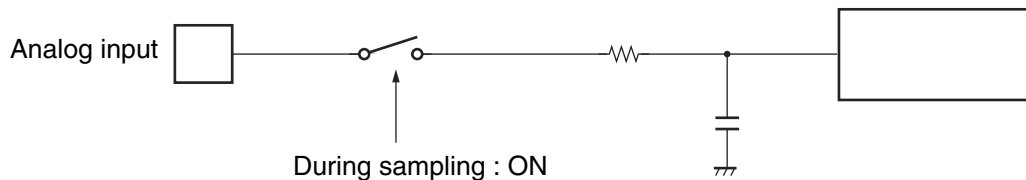
- Timer input timing



• Notes on the external impedance and sampling time of analog inputs

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

	R	C
$4.5\text{ V} \leq \text{AVcc} \leq 5.5\text{ V}$	2.6 k Ω (Max)	8.5 pF (Max)
$4.0\text{ V} \leq \text{AVcc} \leq 4.5\text{ V}$	12.1 k Ω (Max)	8.5 pF (Max)

MB90V920-101/102

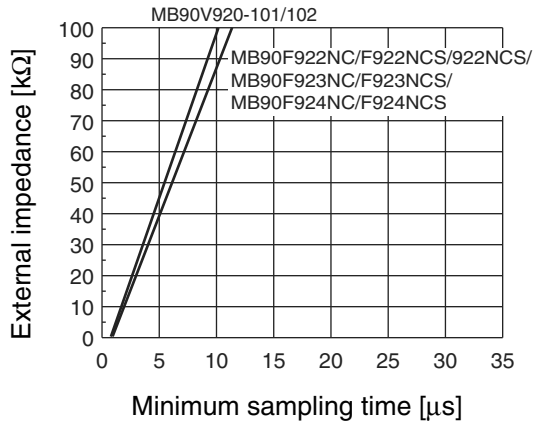
$4.5\text{ V} \leq \text{AVcc} \leq 5.5\text{ V}$	2.0 k Ω (Max)	14.4 pF (Max)
$4.0\text{ V} \leq \text{AVcc} \leq 4.5\text{ V}$	8.2 k Ω (Max)	14.4 pF (Max)

Note : The values are reference values.

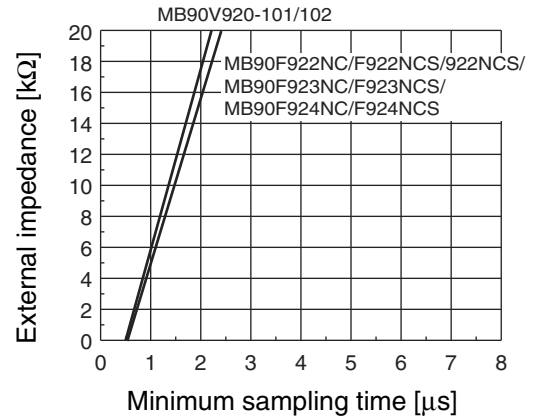
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- The relationship between the external impedance and minimum sampling time
- At $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

(External impedance = 0 k Ω to 100 k Ω)

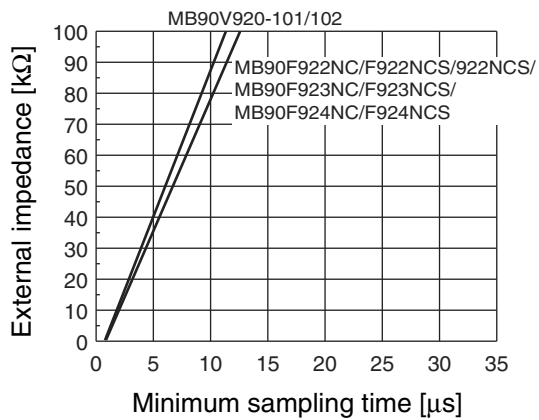


(External impedance = 0 k Ω to 20 k Ω)

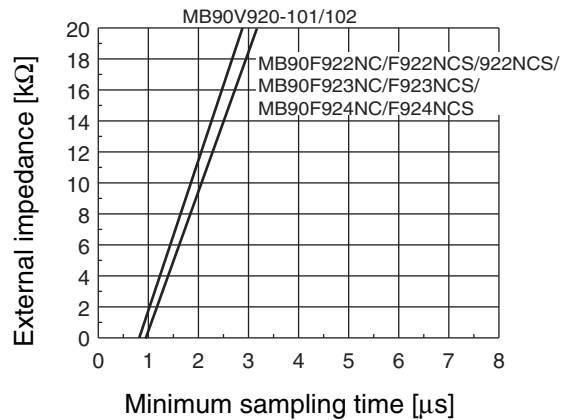


- At $4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$

(External impedance = 0 k Ω to 100 k Ω)



(External impedance = 0 k Ω to 20 k Ω)



- About errors

As $|AV_{RH} - AV_{SS}|$ becomes smaller, the relative errors grow larger.

MEMO

MB90920 Series

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