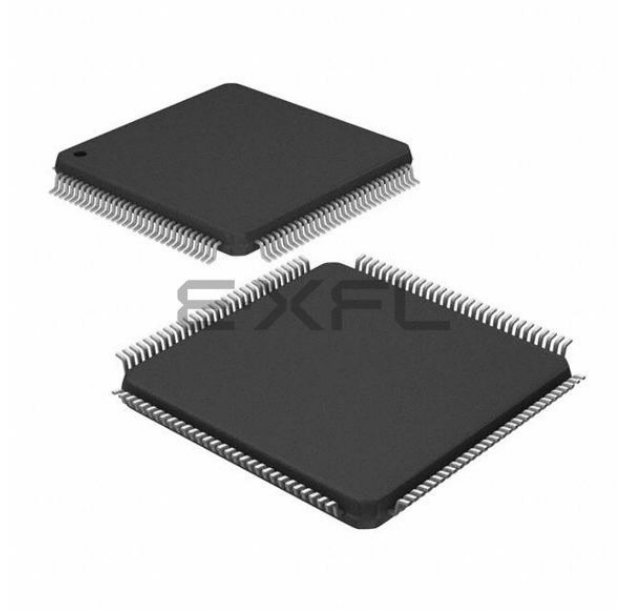
Infineon Technologies - MB90922NCSPMC-GS-127E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-127e1

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

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Pin no.	Pin name	I/O circuit type*1	Function
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin
52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin

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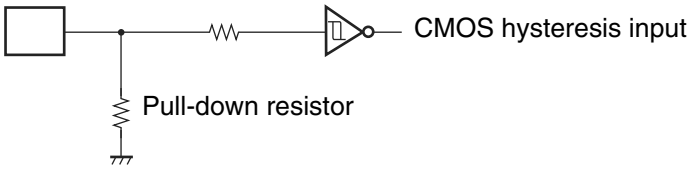
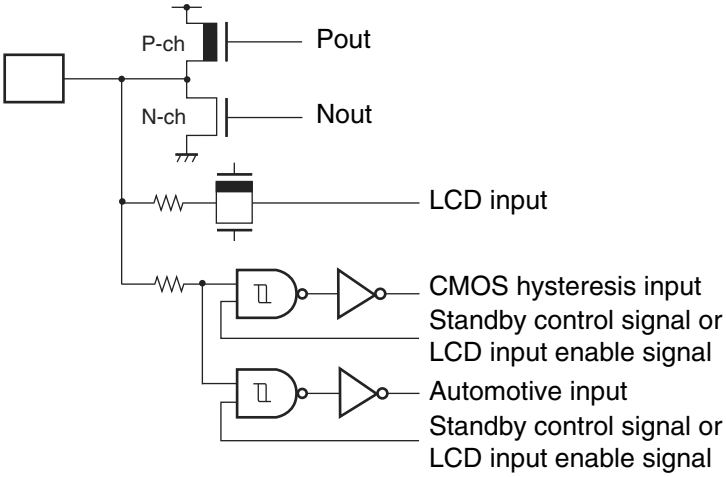
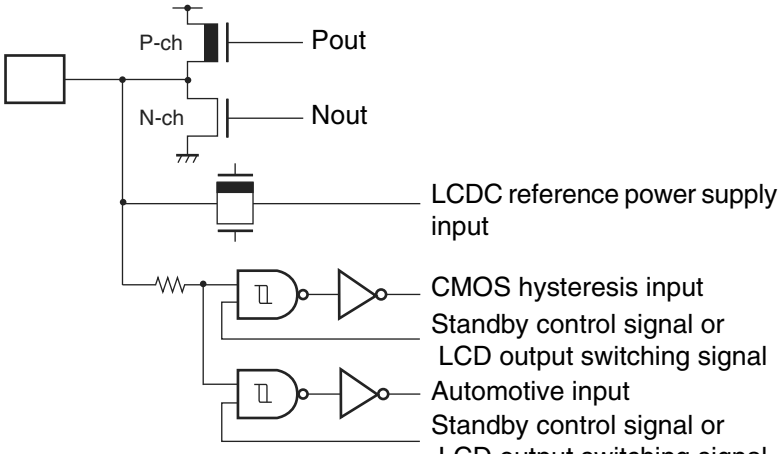
Type	Circuit	Remarks
E		Input-only pin (with pull-down resistance) • Attached pull-down resistance: approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.
F		LCD output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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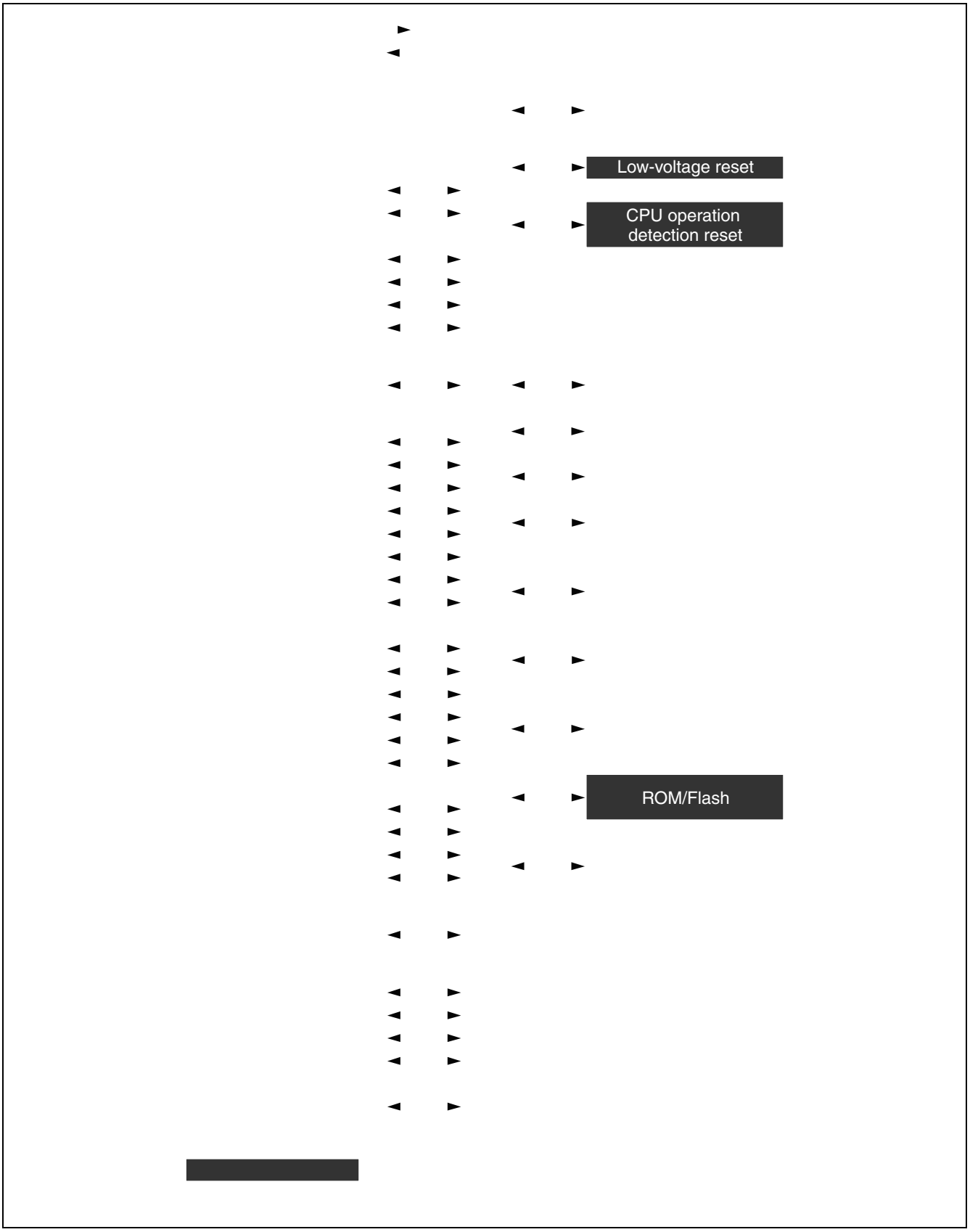
■ BLOCK DIAGRAM



Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000054H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000B
000055H	Higher timer control status register 1	TMCSR1H	R/W		XXX10000B
000056H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
000057H					XXXXXXXXB
000058H	LCD output control register 1	LOCR1	R/W	LCDC	11111111B
000059H	LCD output control register 2	LOCR2	R/W		00000000B
00005AH	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	00000000B
00005BH	Higher sound control register 0	SGCRH0	R/W		0XXXX100B
00005CH	Frequency data register 0	SGFR0	R/W		XXXXXXXXB
00005DH	Amplitude data register 0	SGAR0	R/W		00000000B
00005EH	Decrement grade register 0	SGDR0	R/W		XXXXXXXXB
00005FH	Tone count register 0	SGTR0	R/W		XXXXXXXXB
000060H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXXB
000061H					XXXXXXXXB
000062H	Input capture register 1	IPCP1	R		XXXXXXXXB
000063H					XXXXXXXXB
000064H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXXB
000065H					XXXXXXXXB
000066H	Input capture register 3	IPCP3	R		XXXXXXXXB
000067H					XXXXXXXXB
000068H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000B
000069H	Input capture edge register 0/1	ICE01	R/W		XXX0X0XXB
00006AH	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000B
00006BH	Input capture edge register 2/3	ICE23	R/W		XXXXXXXXB
00006CH	Lower LCD control register	LCRL	R/W	LCD controller/ driver	00010000B
00006DH	Higher LCD control register	LCRH	R/W		00000000B
00006EH	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	00111000B
00006FH	ROM mirror	ROMM	W	ROM mirror	XXXXXXX1B
000070H to 00007FH	Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS"				
000080H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	000000X0B
000081H	(Disabled)				
000082H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	000000X0B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003700H to 0037FFH	Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS"				
003800H to 0038FFH	Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS"				
003900H to 00391FH	(Disabled)				
003920H	PPG0 down counter register	PDCR0	R	16-bit PPG0	11111111B
003921H					11111111B
003922H	PPG0 cycle setting register	PCSR0	W		11111111B
003923H					11111111B
003924H	PPG0 duty setting register	PDUT0	W	16-bit PPG0	00000000B
003925H					00000000B
003926H	PPG0 output division setting register	PPGDIV0	R/W, R		11111100B
003927H	(Disabled)				
003928H	PPG1 down counter register	PDCR1	R	16-bit PPG1	11111111B
003929H					11111111B
00392AH	PPG1 cycle setting register	PCSR1	W		11111111B
00392BH					11111111B
00392CH	PPG1 duty setting register	PDUT1	W		00000000B
00392DH					00000000B
00392EH	PPG1output division setting register	PPGDIV1	R/W, R		11111100B
00392FH	(Disabled)				
003930H	PPG2 down counter register	PDCR2	R	16-bit PPG2	11111111B
003931H					11111111B
003932H	PPG2 cycle setting register	PCSR2	W		11111111B
003933H					11111111B
003934H	PPG2 duty setting register	PDUT2	W		00000000B
003935H					00000000B
003936H	PPG2 output division setting register	PPGDIV2	R/W, R		11111100B
003937H to 00393FH	(Disabled)				
003940H	Input capture register 4	IPCP4	R	Input capture 4/5	XXXXXXXXB
003941H					XXXXXXXXB
003942H	Input capture register 5	IPCP5	R		XXXXXXXXB
003943H					XXXXXXXXB

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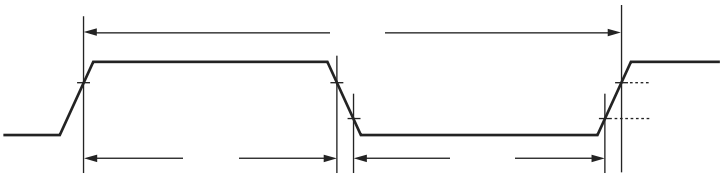
4. AC Characteristics

(1) Clock timing

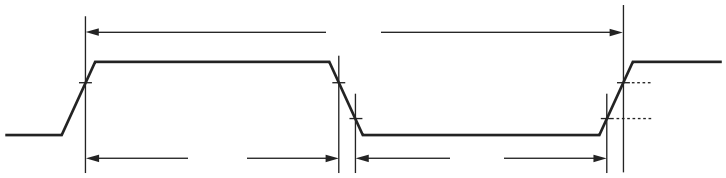
(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

• X0, X1 clock timing



• X0A, X1A clock timing



(2) Reset input

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

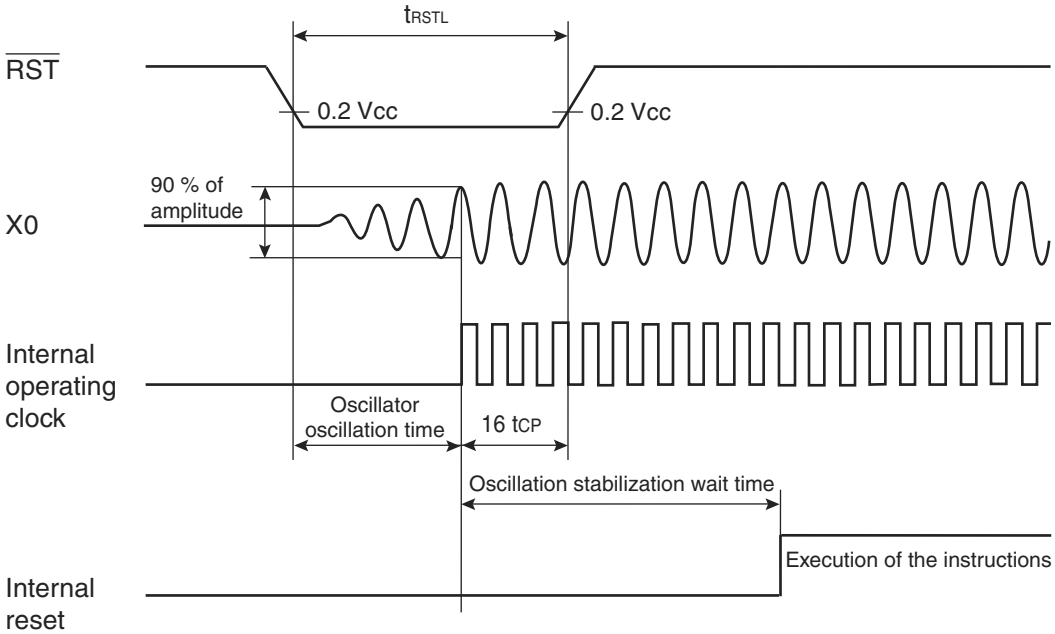
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	During normal operation
			Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	In time-base timer mode

*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

Note : t_{CP} is the internal operating clock cycle time. (Unit : ns)

• During normal operation

• In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



(4) UART0/1/2/3 (LIN/SCI)

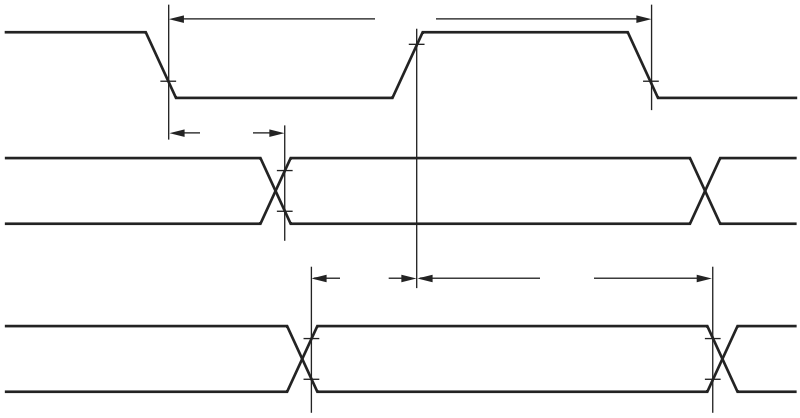
- **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

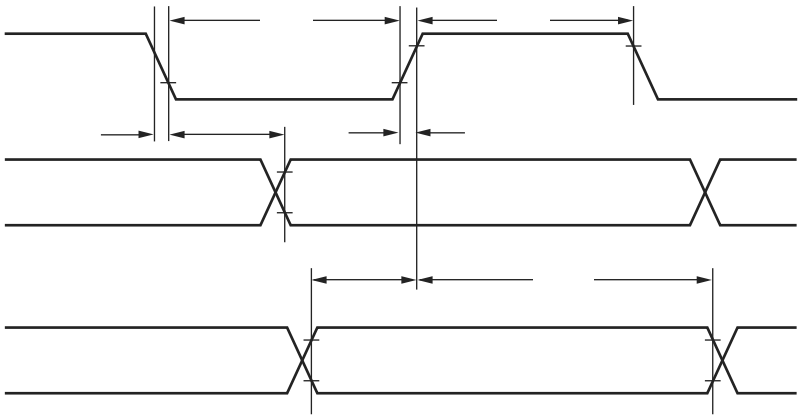
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}			t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Internal shift clock mode



- External shift clock mode



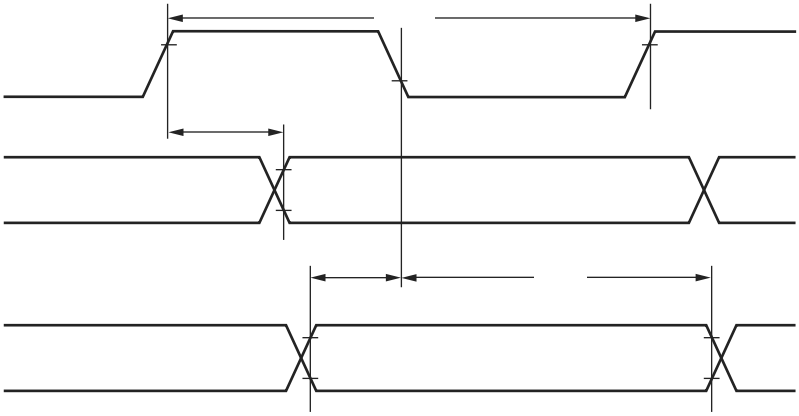
• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

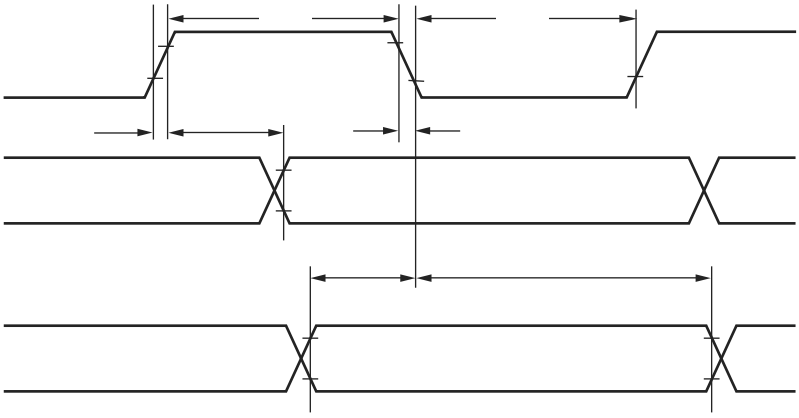
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}			t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Internal shift clock mode



- External shift clock mode

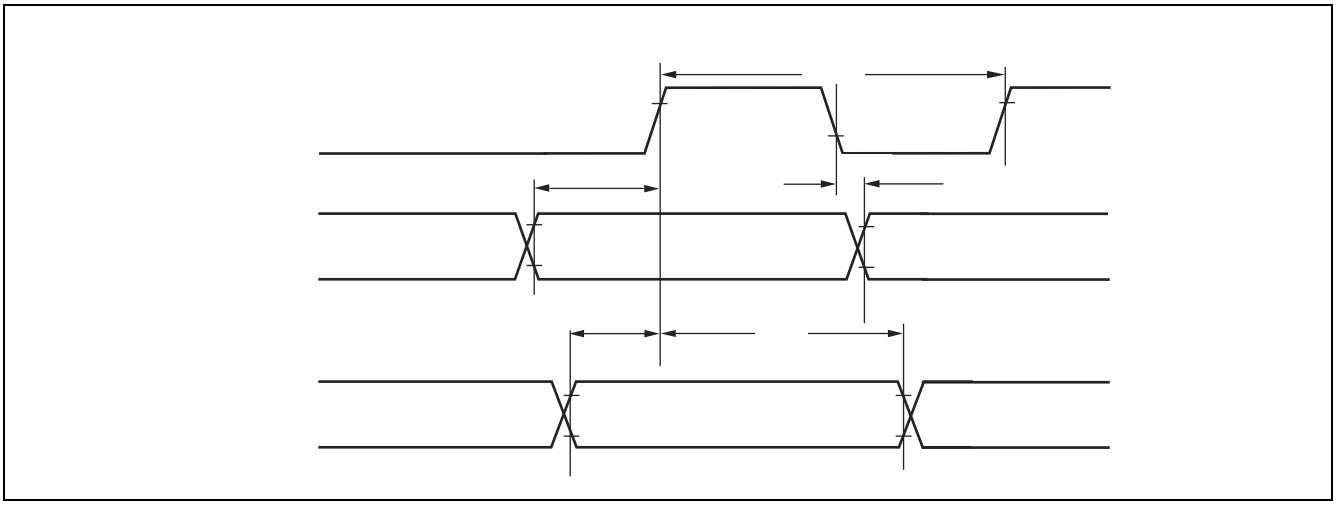


• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.



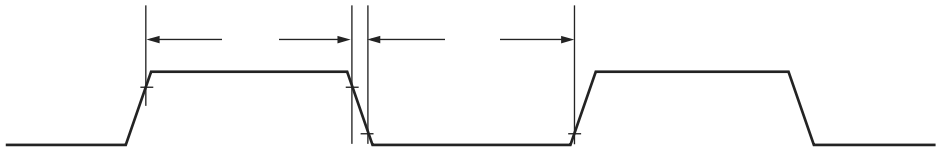
(6) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

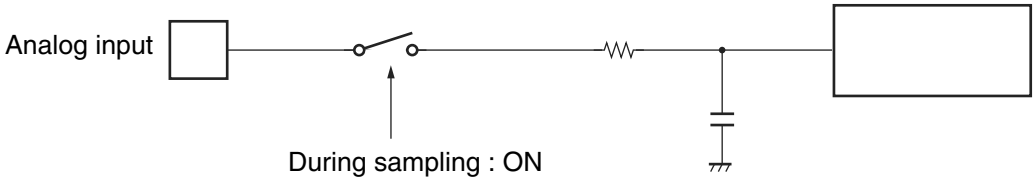
- Trigger input timing



• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	12.1 kΩ (Max)	8.5 pF (Max)

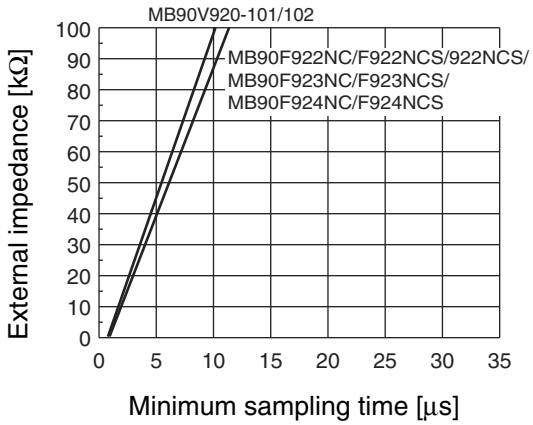
MB90V920-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

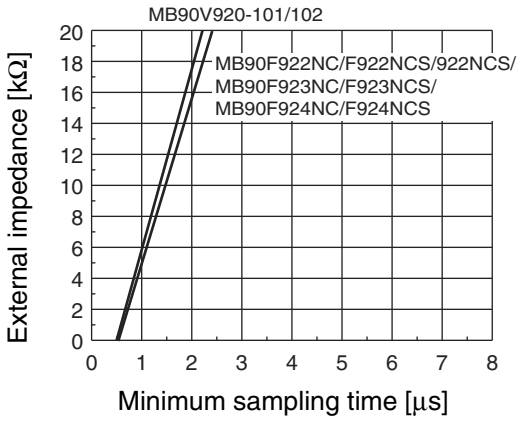
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

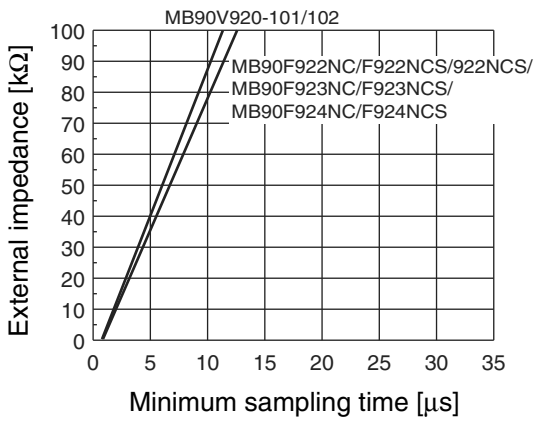


(External impedance = 0 kΩ to 20 kΩ)

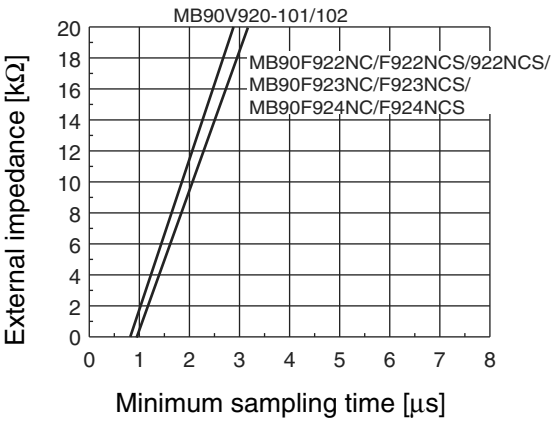


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; • Serial communication • Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970$_H$”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR

The vertical lines marked in the left side of the page show the changes.