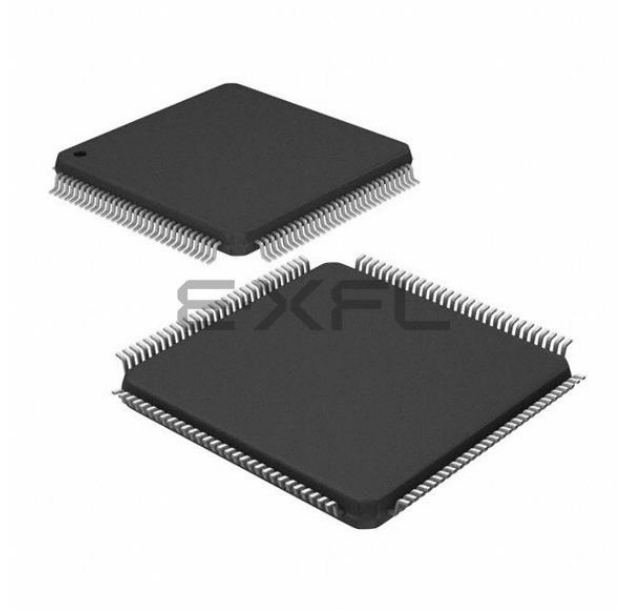
Infineon Technologies - MB90922NCSPMC-GS-130E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-130e1

(Continued)

- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at f_{CP} = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin

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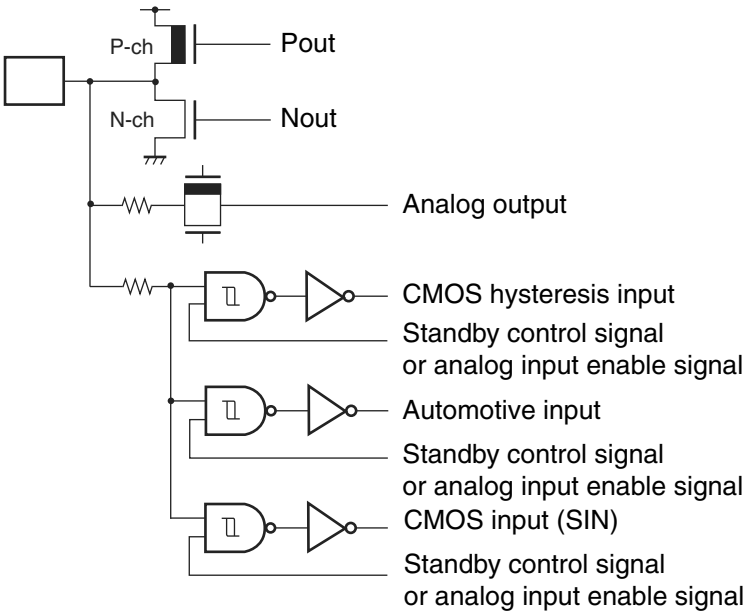
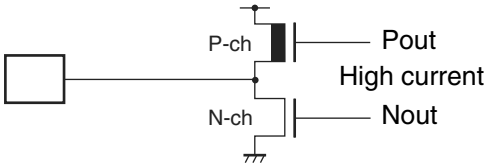
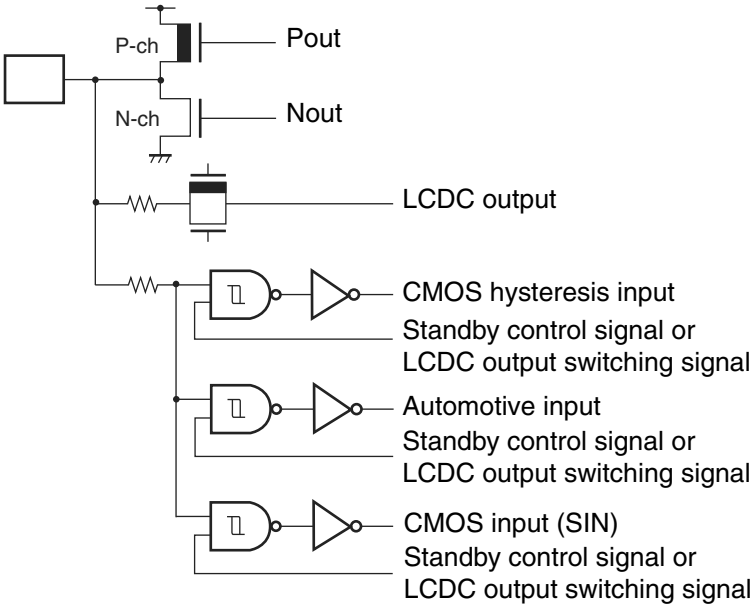
Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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• **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

• **Crystal oscillator circuit**

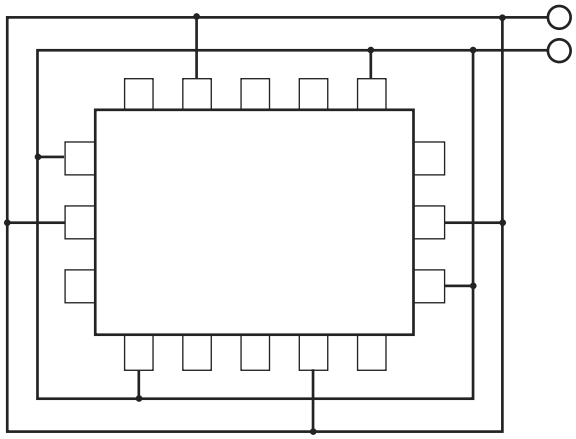
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



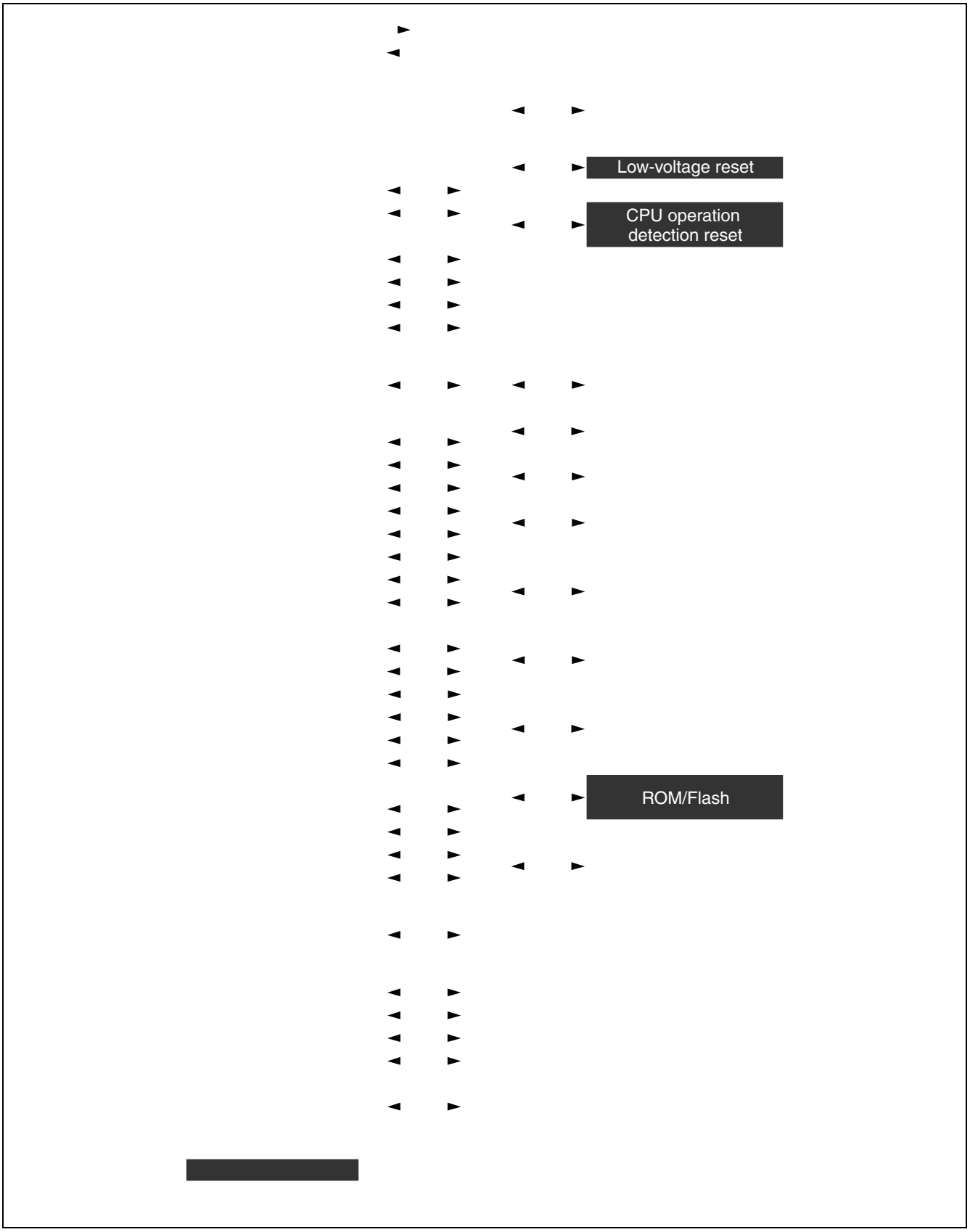
Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

• **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ BLOCK DIAGRAM



■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH, 00000BH	(Disabled)				
00000CH	Port C data register	PDRC	R/W	Port C	XXXXXXXXB
00000DH	Port D data register	PDRD	R/W	Port D	XXXXXXXXB
00000EH	Port E data register	PDRE	R/W	Port E	XXXXXXXXB
00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 direction register	DDR1	R/W	Port 1	XX000000B
000012H	Port 2 direction register	DDR2	R/W	Port 2	000000XXB
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 direction register	DDR9	R/W	Port 9	X0000000B
00001AH	Analog input enable	ADER6	R/W	Port 6, A/D	11111111B
00001BH	(Disabled)				
00001CH	Port C direction register	DDRC	R/W	Port C	00000000B
00001DH	Port D direction register	DDRD	R/W	Port D	X0000000B
00001EH	Port E direction register	DDRE	R/W	Port E	XXXXX000B
00001FH	(Disabled)				
000020H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0B
000021H	Higher A/D control status register	ADCS1	R/W		0000000XB
000022H	Lower A/D control status register	ADCR0	R		00000000B
000023H	Higher A/D data register	ADCR1	R		XXXXXX00B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003970H to 003973H	(Disabled)				
003974H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXXB
003975H	Amplitude data register 1	SGAR1	R/W		00000000B
003976H	Decrement grade register 1	SGDR1	R/W		XXXXXXXXB
003977H	Tone count register 1	SGTR1	R/W		XXXXXXXXB
003978H to 00397FH	(Disabled)				
003980H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXXB
003981H					XXXXXXXXB
003982H	PWM2 compare register 0	PWC20	R/W		XXXXXXXXB
003983H					XXXXXXXXB
003984H	PWM1 select register 0	PWS10	R/W		00000000B
003985H	PWM2 select register 0	PWS20	R/W		X0000000B
003986H, 003987H	(Disabled)				
003988H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXXB
003989H					XXXXXXXXB
00398AH	PWM2 compare register 1	PWC21	R/W		XXXXXXXXB
00398BH					XXXXXXXXB
00398CH	PWM1 select register 1	PWS11	R/W		00000000B
00398DH	PWM2 select register 1	PWS21	R/W		X0000000B
00398EH, 00398FH	(Disabled)				
003990H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXXB
003991H					XXXXXXXXB
003992H	PWM2 compare register 2	PWC22	R/W		XXXXXXXXB
003993H					XXXXXXXXB
003994H	PWM1 select register 2	PWS12	R/W		00000000B
003995H	PWM2 select register 2	PWS22	R/W		X0000000B
003996H, 003997H	(Disabled)				

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■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

List of Message Buffers (ID Registers)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00H to 003A1FH	003B00H to 003B1FH	003700H to 00371FH	003800H to 00381FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003B20H	003720H	003820H	ID register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
003A21H	003B21H	003721H	003821H				
003A22H	003B22H	003722H	003822H				XXXXX---B XXXXXXXXB
003A23H	003B23H	003723H	003823H				
003A24H	003B24H	003724H	003824H	ID register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
003A25H	003B25H	003725H	003825H				
003A26H	003B26H	003726H	003826H				XXXXX---B XXXXXXXXB
003A27H	003B27H	003727H	003827H				
003A28H	003B28H	003728H	003828H	ID register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
003A29H	003B29H	003729H	003829H				
003A2AH	003B2AH	00372AH	00382AH				XXXXX---B XXXXXXXXB
003A2BH	003B2BH	00372BH	00382BH				
003A2CH	003B2CH	00372CH	00382CH	ID register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
003A2DH	003B2DH	00372DH	00382DH				
003A2EH	003B2EH	00372EH	00382EH				XXXXX---B XXXXXXXXB
003A2FH	003B2FH	00372FH	00382FH				
003A30H	003B30H	003730H	003830H	ID register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
003A31H	003B31H	003731H	003831H				
003A32H	003B32H	003732H	003832H				XXXXX---B XXXXXXXXB
003A33H	003B33H	003733H	003833H				
003A34H	003B34H	003734H	003834H	ID register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
003A35H	003B35H	003735H	003835H				
003A36H	003B36H	003736H	003836H				XXXXX---B XXXXXXXXB
003A37H	003B37H	003737H	003837H				
003A38H	003B38H	003738H	003838H	ID register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
003A39H	003B39H	003739H	003839H				
003A3AH	003B3AH	00373AH	00383AH				XXXXX---B XXXXXXXXB
003A3BH	003B3BH	00373BH	00383BH				
003A3CH	003B3CH	00373CH	00383CH	ID register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
003A3DH	003B3DH	00373DH	00383DH				
003A3EH	003B3EH	00373EH	00383EH				XXXXX---B XXXXXXXXB
003A3FH	003B3FH	00373FH	00383FH				

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(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCDC leakage current	I_{LCDC}	V0 to V3, COMm (m = 0 to 3) , SEGn, (n = 00 to 31)	—	—	—	5.0	µA	
LCD output impedance	Rvcom	COMn (n = 0 to 3)	—	—	—	4.5	kΩ	
	Rvseg	SEGn (n = 00 to 31)	—	—	—	17	kΩ	

* : Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

4. AC Characteristics

(1) Clock timing

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

(4) UART0/1/2/3 (LIN/SCI)

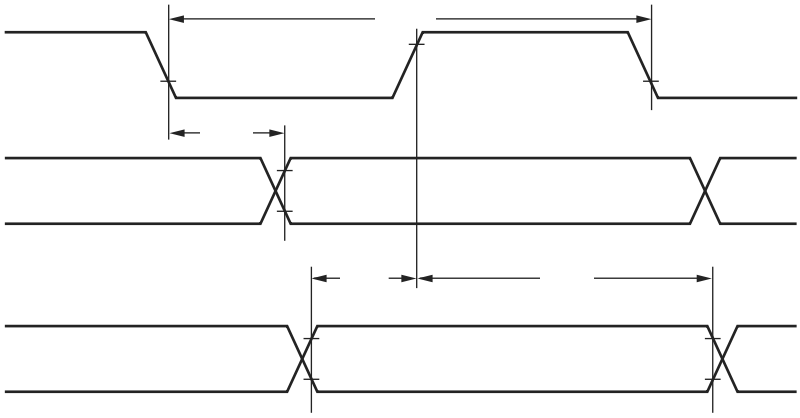
- **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

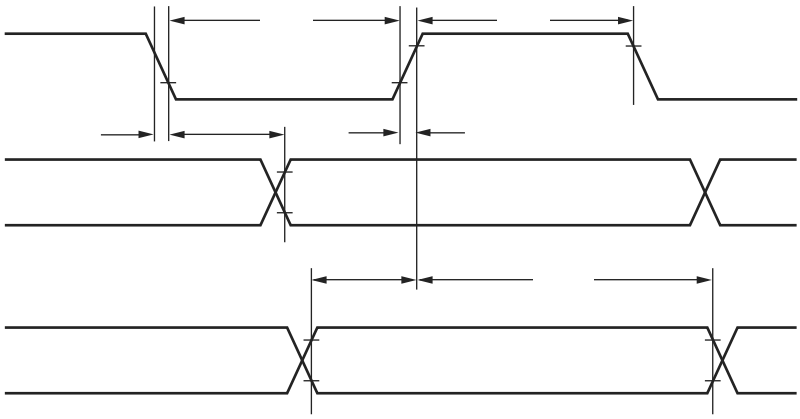
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}			t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Internal shift clock mode



- External shift clock mode



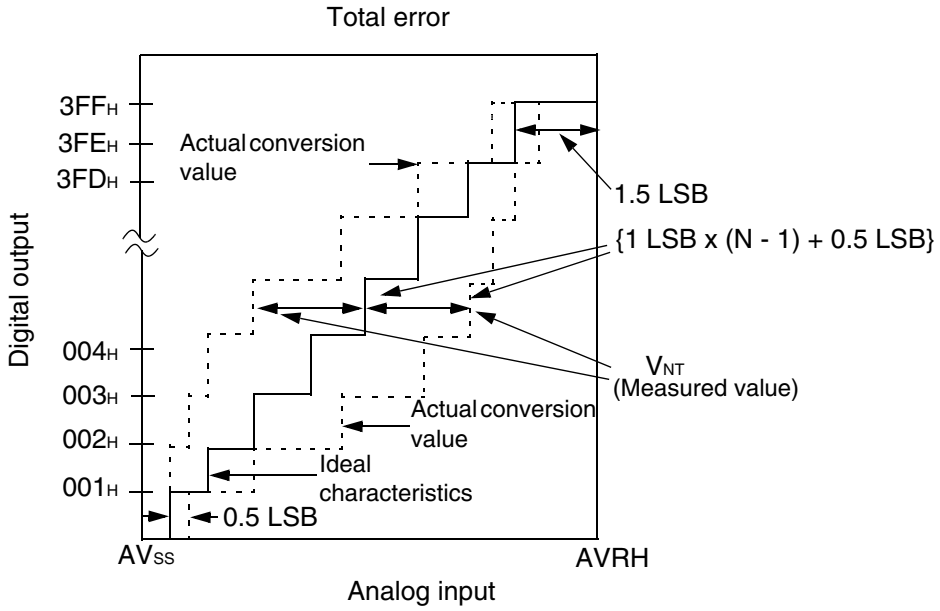
(2) Definition of terms

Resolution : Analog changes that are identifiable by the A/D converter.

Non-Linear error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ←→ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111") from actual conversion characteristics.

Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.

Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

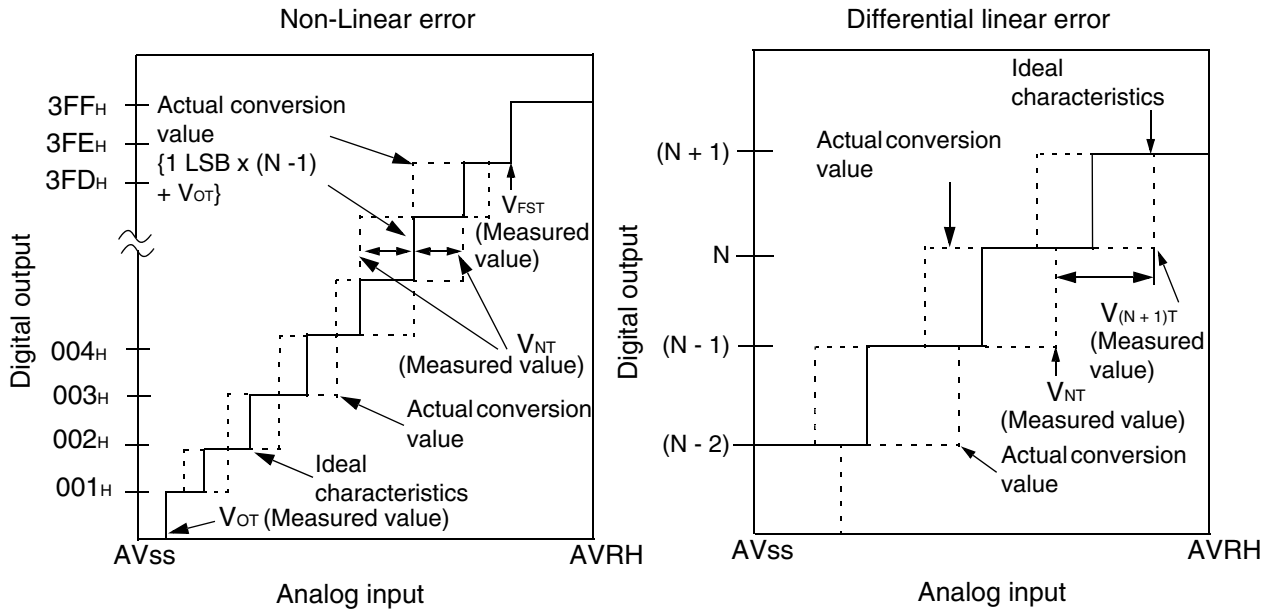
V_{OT} (Ideal) = AVss + 0.5 LSB [V]

V_{FST} (Ideal) = AVRH − 1.5 LSB [V]

V_{NT} : Voltage when the digital output changes from (N - 1) to N

(Continued)

(Continued)



$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

6. Flash Memory Program/Erase Characteristics

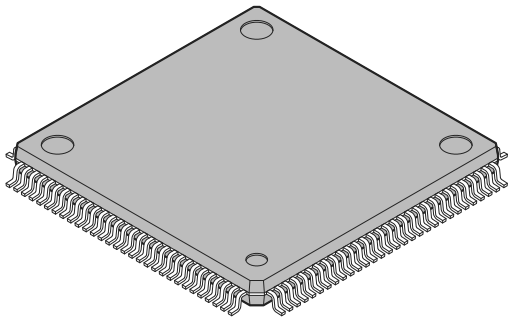
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	0.9	3.6	s	Excludes pre-programming before erase
Word (16-bit width) programming time		—	23	370	µs	Excludes system-level overhead
Chip programming time	T_A = + 25 °C, V_{CC} = 5.0 V	—	3.4	55	s	
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ ORDERING INFORMATION

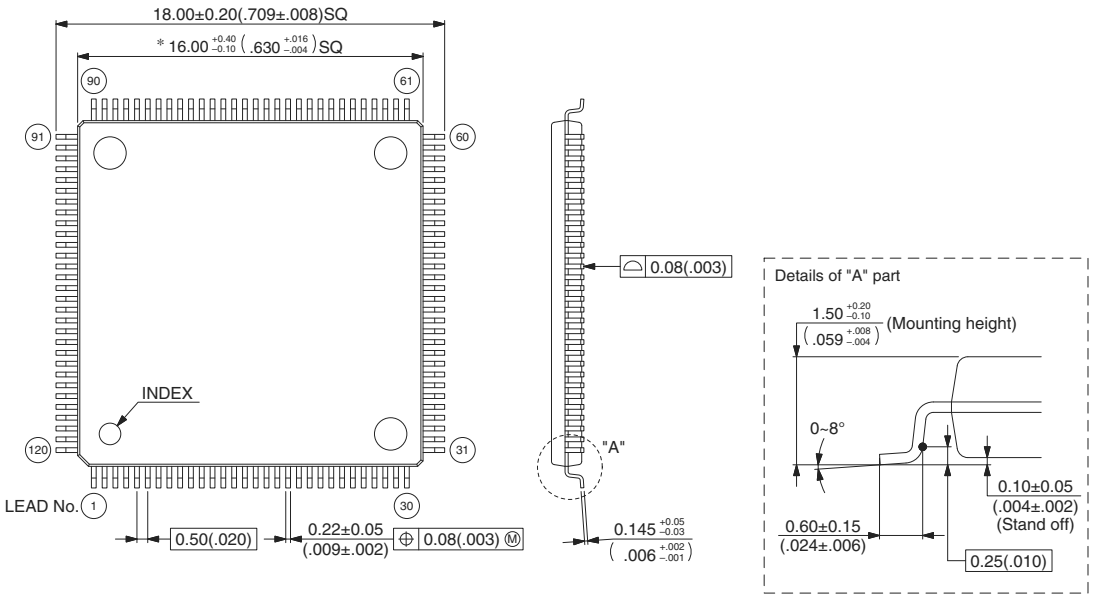
Part number	Package	Remarks
MB90F922NCPMC MB90F922NCSPMC MB90922NCSPMC MB90F923NCPMC MB90F923NCSPMC MB90F924NCPMC MB90F924NCSPMC	120-pin plastic LQFP (FPT-120P-M21)	
MB90V920-101CR MB90V920-102CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; • Serial communication • Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970$_H$”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR

The vertical lines marked in the left side of the page show the changes.