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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-134e1

16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

**MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/
MB90F924NC/F924NCS/V920-101/V920-102**

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
Built-in PLL clock frequency multiplication circuit.
Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
Detects rising, falling, or both edges.
16-bit capture register × 8
The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

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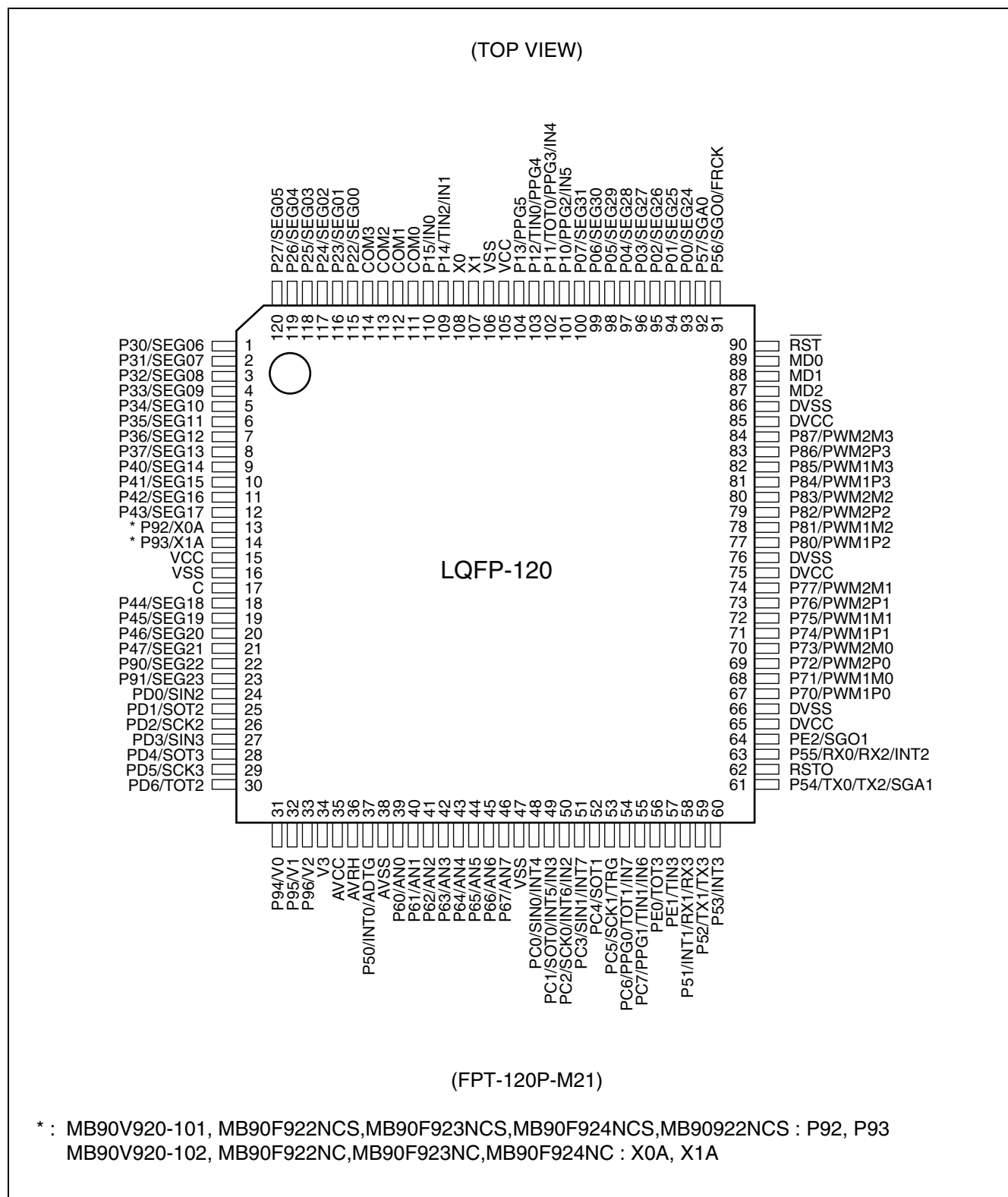
For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevise.fujitsu.com/micom/en-support/>

MB90920 Series

PIN ASSIGNMENT



- **Serial communication**

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024 _H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXX _B
000025 _H			R/W		XXXXXXXX _B
000026 _H	Timer data register	TCDT	R/W		00000000 _B
000027 _H			R/W		00000000 _B
000028 _H	Lower timer control status register	TCCSL	R/W		00000000 _B
000029 _H	Higher timer control status register	TCCSH	R/W		01-00000 _B
00002A _H	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000 _B
00002B _H	Higher PPG0 control status register	PCNTH0	R/W		00000001 _B
00002C _H	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000 _B
00002D _H	Higher PPG1 control status register	PCNTH1	R/W		00000001 _B
00002E _H	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000 _B
00002F _H	Higher PPG2 control status register	PCNTH2	R/W		00000001 _B
000030 _H	External interrupt enable	ENIR	R/W	External interrupt	00000000 _B
000031 _H	External interrupt request	EIRR	R/W		00000000 _B
000032 _H	Lower external interrupt level	ELVRL	R/W		00000000 _B
000033 _H	Higher external interrupt level	ELVRH	R/W		00000000 _B
000034 _H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000 _B
000035 _H	Serial control register 0	SCR0	R/W, W		00000000 _B
000036 _H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000 _B
000037 _H	Serial status register 0	SSR0	R/W, R		00001000 _B
000038 _H	Extended communication control register 0	ECCR0	R/W, R		000000XX _B
000039 _H	Extended status control register 0	ESCR0	R/W		00000100 _B
00003A _H	Baud rate generator register 00	BGR00	R/W		00000000 _B
00003B _H	Baud rate generator register 01	BGR01	R/W, R		00000000 _B
00003C _H to 00003F _H	(Disabled)				
000040 _H to 00004F _H	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
000050 _H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000 _B
000051 _H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000 _B
000052 _H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
000053 _H					XXXXXXXX _B

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Address	Register name	Symbol	Read/write	Resource name	Initial value
000054 _H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000 _B
000055 _H	Higher timer control status register 1	TMCSR1H	R/W		XXX10000 _B
000056 _H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX _B
000057 _H					XXXXXXXX _B
000058 _H	LCD output control register 1	LOCR1	R/W	LCDC	11111111 _B
000059 _H	LCD output control register 2	LOCR2	R/W		00000000 _B
00005A _H	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	00000000 _B
00005B _H	Higher sound control register 0	SGCRH0	R/W		0XXXX100 _B
00005C _H	Frequency data register 0	SGFR0	R/W		XXXXXXXX _B
00005D _H	Amplitude data register 0	SGAR0	R/W		00000000 _B
00005E _H	Decrement grade register 0	SGDR0	R/W		XXXXXXXX _B
00005F _H	Tone count register 0	SGTR0	R/W		XXXXXXXX _B
000060 _H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXX _B
000061 _H					XXXXXXXX _B
000062 _H	Input capture register 1	IPCP1	R		XXXXXXXX _B
000063 _H					XXXXXXXX _B
000064 _H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXX _B
000065 _H					XXXXXXXX _B
000066 _H	Input capture register 3	IPCP3	R		XXXXXXXX _B
000067 _H					XXXXXXXX _B
000068 _H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000 _B
000069 _H	Input capture edge register 0/1	ICE01	R/W		XXX0X0XX _B
00006A _H	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000 _B
00006B _H	Input capture edge register 2/3	ICE23	R/W		XXXXXXXX _B
00006C _H	Lower LCD control register	LCRL	R/W	LCD controller/ driver	00010000 _B
00006D _H	Higher LCD control register	LCRH	R/W		00000000 _B
00006E _H	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	00111000 _B
00006F _H	ROM mirror	ROMM	W	ROM mirror	XXXXXXXX1 _B
000070 _H to 00007F _H	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
000080 _H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	000000X0 _B
000081 _H	(Disabled)				
000082 _H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	000000X0 _B

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MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000D4 _H	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000 _B
0000D5 _H	Higher timer control status register 2	TMCSR2H	R/W		XXX10000 _B
0000D6 _H	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000 _B
0000D7 _H	Higher timer control status register 3	TMCSR3H	R/W		XXX10000 _B
0000D8 _H	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000 _B
0000D9 _H	Higher sound control register 1	SGCRH1	R/W		0XXXX100 _B
0000DA _H	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000 _B
0000DB _H	Higher PPG3 control status register	PCNTH3	R/W		00000001 _B
0000DC _H	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000 _B
0000DD _H	Higher PPG4 control status register	PCNTH4	R/W		00000001 _B
0000DE _H	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000 _B
0000DF _H	Higher PPG5 control status register	PCNTH5	R/W		00000001 _B
0000E0 _H	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000 _B
0000E1 _H	Serial control register 2	SCR2	R/W, W		00000000 _B
0000E2 _H	Reception/transmission data register 2	RDR2/ TDR2	R/W		00000000 _B
0000E3 _H	Serial status register 2	SSR2	R/W, R		00001000 _B
0000E4 _H	Extended communication control register 2	ECCR2	R/W, R		000000XX _B
0000E5 _H	Extended status control register 2	ESCR2	R/W		00000100 _B
0000E6 _H	Baud rate generator register 20	BGR20	R/W		00000000 _B
0000E7 _H	Baud rate generator register 21	BGR21	R/W, R		00000000 _B
0000E8 _H	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000 _B
0000E9 _H	Serial control register 3	SCR3	R/W, W		00000000 _B
0000EA _H	Reception/transmission data register 3	RDR3/ TDR3	R/W		00000000 _B
0000EB _H	Serial status register 3	SSR3	R/W, R		00001000 _B
0000EC _H	Extended communication control register 3	ECCR3	R/W, R		000000XX _B
0000ED _H	Extended status control register 3	ESCR3	R/W		00000100 _B
0000EE _H	Baud rate generator register 30	BGR30	R/W		00000000 _B
0000EF _H	Baud rate generator register 31	BGR31	R/W, R		00000000 _B
001FF0 _H	Program address detection register 0	PADR0	R/W	Address match detection	XXXXXXXX _B
001FF1 _H	Program address detection register 1	PADR0	R/W		XXXXXXXX _B
001FF2 _H	Program address detection register 2	PADR0	R/W		XXXXXXXX _B
001FF3 _H	Program address detection register 3	PADR1	R/W		XXXXXXXX _B
001FF4 _H	Program address detection register 4	PADR1	R/W		XXXXXXXX _B
001FF5 _H	Program address detection register 5	PADR1	R/W		XXXXXXXX _B

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MB90920 Series

Address	Register name	Symbol	Read/write	Resource name	Initial value
003944 _H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXX _B
003945 _H					XXXXXXXX _B
003946 _H	Input capture register 7	IPCP7	R		XXXXXXXX _B
003947 _H					XXXXXXXX _B
003948 _H to 00394F _H	(Disabled)				
003950 _H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXX _B
003951 _H					XXXXXXXX _B
003952 _H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXX _B
003953 _H					XXXXXXXX _B
003954 _H to 003957 _H	(Disabled)				
003958 _H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXX _B
003959 _H					XXXXXXXX _B
00395A _H					XXXXXXXX _B
00395B _H	Second data register	WTSR	R/W		XX000000 _B
00395C _H	Minute data register	WTMR	R/W		XX000000 _B
00395D _H	Hour data register	WTHR	R/W		XXX00000 _B
00395E _H	Day data register	WTDR	R/W		00X00001 _B
00395F _H	(Disabled)				
003960 _H	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXX _B
003961 _H					XXXXXXXX _B
003962 _H					XXXXXXXX _B
003963 _H					XXXXXXXX _B
003964 _H					XXXXXXXX _B
003965 _H					XXXXXXXX _B
003966 _H					XXXXXXXX _B
003967 _H					XXXXXXXX _B
003968 _H					XXXXXXXX _B
003969 _H					XXXXXXXX _B
00396A _H					XXXXXXXX _B
00396B _H					XXXXXXXX _B
00396C _H					XXXXXXXX _B
00396D _H					XXXXXXXX _B
00396E _H					XXXXXXXX _B
00396F _H					XXXXXXXX _B

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MB90920 Series

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003998 _H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXX _B
003999 _H					XXXXXXXX _B
00399A _H	PWM2 compare register 3	PWC23	R/W		XXXXXXXX _B
00399B _H					XXXXXXXX _B
00399C _H	PWM1 select register 3	PWS13	R/W		00000000 _B
00399D _H	PWM2 select register 3	PWS23	R/W		X0000000 _B
00399E _H to 0039A5 _H	(Disabled)				
0039A6 _H	Flash write control register 0	FWR0	R/W	Flash I/F	00000000 _B
0039A7 _H	Flash write control register 1	FWR1			00000000 _B
0039A8 _H to 0039BF _H	(Disabled)				
0039C0 _H to 0039DF _H	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0039E0 _H to 0039FF _H	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				
003A00 _H to 003AFF _H	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003B00 _H to 003BFF _H	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003C00 _H to 003CFF _H	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003D00 _H to 003DFF _H	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003E00 _H to 003EFF _H	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
003F00 _H to 003FFF _H	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				

List of Message Buffers (ID Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00 _H to 003A1F _H	003B00 _H to 003B1F _H	003700 _H to 00371F _H	003800 _H to 00381F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003B20 _H	003720 _H	003820 _H	ID register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
003A21 _H	003B21 _H	003721 _H	003821 _H				XXXXXX--- _B XXXXXXXX _B
003A22 _H	003B22 _H	003722 _H	003822 _H				
003A23 _H	003B23 _H	003723 _H	003823 _H				
003A24 _H	003B24 _H	003724 _H	003824 _H	ID register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
003A25 _H	003B25 _H	003725 _H	003825 _H				XXXXXX--- _B XXXXXXXX _B
003A26 _H	003B26 _H	003726 _H	003826 _H				
003A27 _H	003B27 _H	003727 _H	003827 _H				
003A28 _H	003B28 _H	003728 _H	003828 _H	ID register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
003A29 _H	003B29 _H	003729 _H	003829 _H				XXXXXX--- _B XXXXXXXX _B
003A2A _H	003B2A _H	00372A _H	00382A _H				
003A2B _H	003B2B _H	00372B _H	00382B _H				
003A2C _H	003B2C _H	00372C _H	00382C _H	ID register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
003A2D _H	003B2D _H	00372D _H	00382D _H				XXXXXX--- _B XXXXXXXX _B
003A2E _H	003B2E _H	00372E _H	00382E _H				
003A2F _H	003B2F _H	00372F _H	00382F _H				
003A30 _H	003B30 _H	003730 _H	003830 _H	ID register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
003A31 _H	003B31 _H	003731 _H	003831 _H				XXXXXX--- _B XXXXXXXX _B
003A32 _H	003B32 _H	003732 _H	003832 _H				
003A33 _H	003B33 _H	003733 _H	003833 _H				
003A34 _H	003B34 _H	003734 _H	003834 _H	ID register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
003A35 _H	003B35 _H	003735 _H	003835 _H				XXXXXX--- _B XXXXXXXX _B
003A36 _H	003B36 _H	003736 _H	003836 _H				
003A37 _H	003B37 _H	003737 _H	003837 _H				
003A38 _H	003B38 _H	003738 _H	003838 _H	ID register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
003A39 _H	003B39 _H	003739 _H	003839 _H				XXXXXX--- _B XXXXXXXX _B
003A3A _H	003B3A _H	00373A _H	00383A _H				
003A3B _H	003B3B _H	00373B _H	00383B _H				
003A3C _H	003B3C _H	00373C _H	00383C _H	ID register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
003A3D _H	003B3D _H	00373D _H	00383D _H				XXXXXX--- _B XXXXXXXX _B
003A3E _H	003B3E _H	00373E _H	00383E _H				
003A3F _H	003B3F _H	00373F _H	00383F _H				

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MB90920 Series

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Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40 _H	003B40 _H	003740 _H	003840 _H	ID register 8	IDR8	R/W	XXXXXXXX _B XXXXXXXX _B
003A41 _H	003B41 _H	003741 _H	003841 _H				XXXXXX--- _B XXXXXXXX _B
003A42 _H	003B42 _H	003742 _H	003842 _H				
003A43 _H	003B43 _H	003743 _H	003843 _H				
003A44 _H	003B44 _H	003744 _H	003844 _H	ID register 9	IDR9	R/W	XXXXXXXX _B XXXXXXXX _B
003A45 _H	003B45 _H	003745 _H	003845 _H				XXXXXX--- _B XXXXXXXX _B
003A46 _H	003B46 _H	003746 _H	003846 _H				
003A47 _H	003B47 _H	003747 _H	003847 _H				
003A48 _H	003B48 _H	003748 _H	003848 _H	ID register 10	IDR10	R/W	XXXXXXXX _B XXXXXXXX _B
003A49 _H	003B49 _H	003749 _H	003849 _H				XXXXXX--- _B XXXXXXXX _B
003A4A _H	003B4A _H	00374A _H	00384A _H				
003A4B _H	003B4B _H	00374B _H	00384B _H				
003A4C _H	003B4C _H	00374C _H	00384C _H	ID register 11	IDR11	R/W	XXXXXXXX _B XXXXXXXX _B
003A4D _H	003B4D _H	00374D _H	00384D _H				XXXXXX--- _B XXXXXXXX _B
003A4E _H	003B4E _H	00374E _H	00384E _H				
003A4F _H	003B4F _H	00374F _H	00384F _H				
003A50 _H	003B50 _H	003750 _H	003850 _H	ID register 12	IDR12	R/W	XXXXXXXX _B XXXXXXXX _B
003A51 _H	003B51 _H	003751 _H	003851 _H				XXXXXX--- _B XXXXXXXX _B
003A52 _H	003B52 _H	003752 _H	003852 _H				
003A53 _H	003B53 _H	003753 _H	003853 _H				
003A54 _H	003B54 _H	003754 _H	003854 _H	ID register 13	IDR13	R/W	XXXXXXXX _B XXXXXXXX _B
003A55 _H	003B55 _H	003755 _H	003855 _H				XXXXXX--- _B XXXXXXXX _B
003A56 _H	003B56 _H	003756 _H	003856 _H				
003A57 _H	003B57 _H	003757 _H	003857 _H				
003A58 _H	003B58 _H	003758 _H	003858 _H	ID register 14	IDR14	R/W	XXXXXXXX _B XXXXXXXX _B
003A59 _H	003B59 _H	003759 _H	003859 _H				XXXXXX--- _B XXXXXXXX _B
003A5A _H	003B5A _H	00375A _H	00385A _H				
003A5B _H	003B5B _H	00375B _H	00385B _H				
003A5C _H	003B5C _H	00375C _H	00385C _H	ID register 15	IDR15	R/W	XXXXXXXX _B XXXXXXXX _B
003A5D _H	003B5D _H	00375D _H	00385D _H				XXXXXX--- _B XXXXXXXX _B
003A5E _H	003B5E _H	00375E _H	00385E _H				
003A5F _H	003B5F _H	00375F _H	00385F _H				

List of Message Buffers (Data register)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A80 _H to 003A87 _H	003B80 _H to 003B87 _H	003780 _H to 003787 _H	003880 _H to 003887 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
003A88 _H to 003A8F _H	003B88 _H to 003B8F _H	003788 _H to 00378F _H	003888 _H to 00388F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003B90 _H to 003B97 _H	003790 _H to 003797 _H	003890 _H to 003897 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003B98 _H to 003B9F _H	003798 _H to 00379F _H	003898 _H to 00389F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003BA0 _H to 003BA7 _H	0037A0 _H to 0037A7 _H	0038A0 _H to 0038A7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003BA8 _H to 003BAF _H	0037A8 _H to 0037AF _H	0038A8 _H to 0038AF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003BB0 _H to 003BB7 _H	0037B0 _H to 0037B7 _H	0038B0 _H to 0038B7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003BB8 _H to 003BBF _H	0037B8 _H to 0037BF _H	0038B8 _H to 0038BF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003BC0 _H to 003BC7 _H	0037C0 _H to 0037C7 _H	0038C0 _H to 0038C7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003BC8 _H to 003BCF _H	0037C8 _H to 0037CF _H	0038C8 _H to 0038CF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003BD0 _H to 003BD7 _H	0037D0 _H to 0037D7 _H	0038D0 _H to 0038D7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003BD8 _H to 003BDF _H	0037D8 _H to 0037DF _H	0038D8 _H to 0038DF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003BE0 _H to 003BE7 _H	0037E0 _H to 0037E7 _H	0038E0 _H to 0038E7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003BE8 _H to 003BEF _H	0037E8 _H to 0037EF _H	0038E8 _H to 0038EF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003BF0 _H to 003BF7 _H	0037F0 _H to 0037F7 _H	0038F0 _H to 0038F7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003BF8 _H to 003BFF _H	0037F8 _H to 0037FF _H	0038F8 _H to 0038FF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI ² OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08 _H	FFFFDC _H	—	—	High ↑ ↓ Low
INT9 instruction	×	#09	09 _H	FFFFD8 _H	—	—	
Exception processing	×	#10	0A _H	FFFFD4 _H	—	—	
CAN0 received/CAN2 received	×	#11	0B _H	FFFFD0 _H	ICR00	0000B0 _H *1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	0C _H	FFFFCC _H			
CAN1 received/CAN3 received	×	#13	0D _H	FFFFC8 _H	ICR01	0000B1 _H *1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	0E _H	FFFFC4 _H			
Input capture 0	△	#15	0F _H	FFFFC0 _H	ICR02	0000B2 _H *1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10 _H	FFFFBC _H			
Reload timer 0	△	#17	11 _H	FFFFB8 _H	ICR03	0000B3 _H *1	
Reload timer 2	△	#18	12 _H	FFFFB4 _H			
Input capture 1	△	#19	13 _H	FFFFB0 _H	ICR04	0000B4 _H *1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14 _H	FFFFAC _H			
Input capture 2	△	#21	15 _H	FFFFA8 _H	ICR05	0000B5 _H *1	
Reload timer 3	△	#22	16 _H	FFFFA4 _H			
Input capture 3/4/5/6/7	△	#23	17 _H	FFFFA0 _H	ICR06	0000B6 _H *1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18 _H	FFFF9C _H			
PPG timer 0	△	#25	19 _H	FFFF98 _H	ICR07	0000B7 _H *1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1A _H	FFFF94 _H			
PPG timer 1	△	#27	1B _H	FFFF90 _H	ICR08	0000B8 _H *1	
Reload timer 1	△	#28	1C _H	FFFF8C _H			
PPG timer 2/3/4/5	○	#29	1D _H	FFFF88 _H	ICR09	0000B9 _H *1	
Real time watch timer watch timer (sub clock)	×	#30	1E _H	FFFF84 _H			
Free-run timer overflow/clear	×	#31	1F _H	FFFF80 _H	ICR10	0000BA _H *1	
A/D converter conversion complete	○	#32	20 _H	FFFF7C _H			
Sound generator 0/1	×	#33	21 _H	FFFF78 _H	ICR11	0000BB _H *1	
Time-base timer	×	#34	22 _H	FFFF74 _H			
UART2 RX	○	#35	23 _H	FFFF70 _H	ICR12	0000BC _H *1	
UART2 TX	△	#36	24 _H	FFFF6C _H			

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	AV _{CC} = V _{CC} *2
	AVRH	V _{SS} – 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH*2
	DV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	DV _{CC} = V _{CC} *2
Input voltage*1	V _I	V _{SS} – 0.3	V _{CC} + 0.3	V	*3
Output voltage*1	V _O	V _{SS} – 0.3	V _{CC} + 0.3	V	
Maximum clamp current	I _{CLAMP}	– 4	+ 4	mA	*7
Total maximum clamp current	Σ I _{CLAMP}	—	40	mA	*7
“L” level maximum output current*4	I _{OL1}	—	15	mA	Except P70 to P77 and P80 to P87
	I _{OL2}	—	40	mA	P70 to P77 and P80 to P87
“L” level average output current*5	I _{OLAV1}	—	4	mA	Except P70 to P77 and P80 to P87
	I _{OLAV2}	—	30	mA	P70 to P77 and P80 to P87
“L” level maximum total output current	ΣI _{OL1}	—	100	mA	Except P70 to P77 and P80 to P87
	ΣI _{OL2}	—	330	mA	P70 to P77 and P80 to P87
“L” level average total output current	ΣI _{OLAV1}	—	50	mA	Except P70 to P77 and P80 to P87
	ΣI _{OLAV2}	—	250	mA	P70 to P77 and P80 to P87
“H” level maximum output current	I _{OH1} *4	—	–15	mA	Except P70 to P77 and P80 to P87
	I _{OH2} *4	—	–40	mA	P70 to P77 and P80 to P87
“H” level average output current	I _{OHAV1} *5	—	–4	mA	Except P70 to P77 and P80 to P87
	I _{OHAV2} *5	—	–30	mA	P70 to P77 and P80 to P87
“H” level maximum total output current	ΣI _{OH1}	—	–100	mA	Except P70 to P77 and P80 to P87
	ΣI _{OH2}	—	–330	mA	P70 to P77 and P80 to P87
“H” level average total output current	ΣI _{OHAV1} *6	—	–50	mA	Except P70 to P77 and P80 to P87
	ΣI _{OHAV2} *6	—	–250	mA	P70 to P77 and P80 to P87
Power consumption	P _D	—	625	mW	
Operating temperature	T _A	– 40	+ 105	°C	
Storage temperature	T _{STG}	– 55	+ 150	°C	

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : AV_{CC}, AVRH must not exceed V_{CC}, and AVRH must not exceed AV_{CC}.

When using an evaluation product, DV_{CC} must not exceed V_{CC} (however, DV_{CC} can be set to a higher voltage than V_{CC} when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, I_{CLAMP} is the applicable rating instead of V_I.

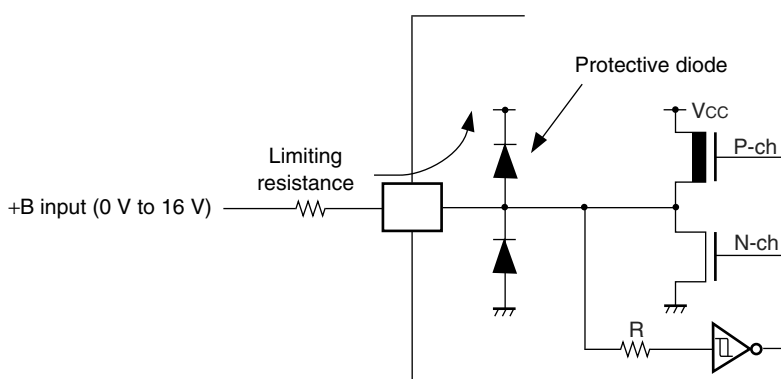
*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

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- *5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.
- *6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.
- *7 :
 - Applicable to pins: P10 to P15, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PC0 to PC7, PD0 to PD6, PE0 to PE2
 - Use within recommended operating conditions.
 - Use at DC voltage (current) .
 - The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
 - Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
 - Care must be taken not to leave +B input pins open.
 - Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
 - Sample recommended circuit :

- Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90920 Series

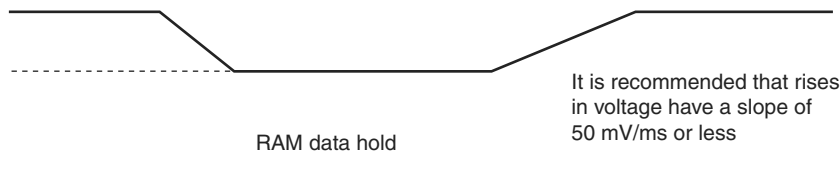
(3) Power-on reset

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	VCC	—	0.05	30	ms	
Power off time	t_{OFF}			1	—	ms	Waiting time until power-on



Note : Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



(4) UART0/1/2/3 (LIN/SCI)

- Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0 \text{ V} \pm 10 \%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}			0	—	ns
Serial clock “L” pulse width	t _{SLSH}	SCK0 to SCK3	External shift clock mode output pin C _L = 80 pF + 1TTL	3 t _{CP} − t _R	—	ns
Serial clock “H” pulse width	t _{SHSL}			t _{CP} + 10	—	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t _{CP} + 60	ns
Valid SIN → SCK ↑	t _{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXE}			t _{CP} + 30	—	ns
SCK ↓ time	t _F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t _R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.

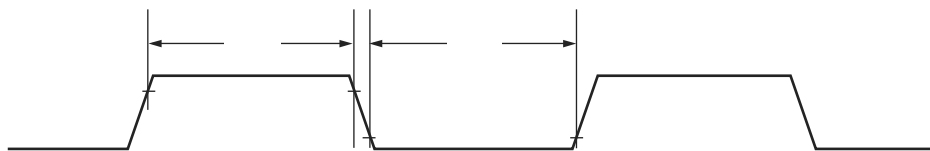
(6) Trigger input timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} , t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	$t_{CP} + 200$	—	ns	

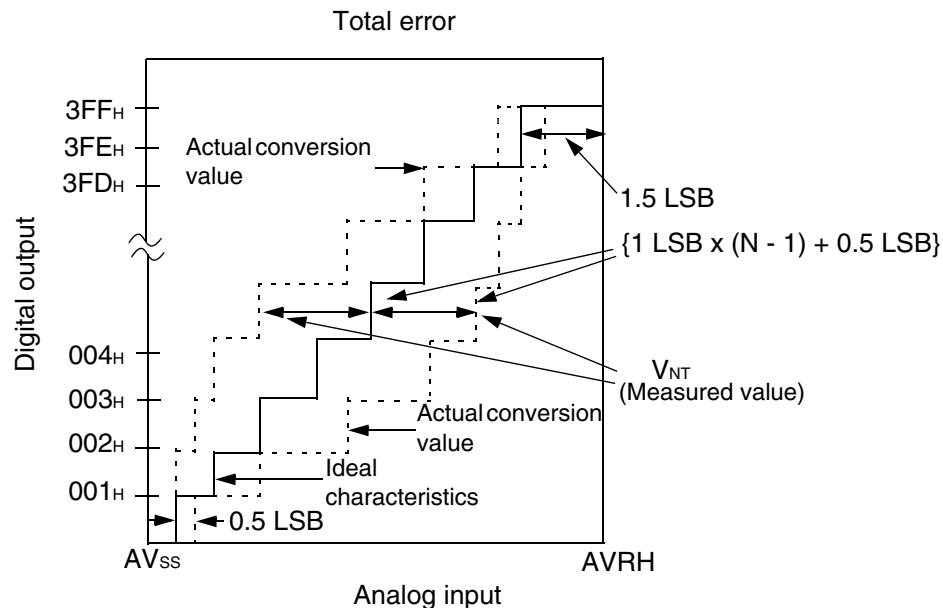
Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.

- Trigger input timing



(2) Definition of terms

- Resolution : Analog changes that are identifiable by the A/D converter.
- Non-Linear error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” $\longleftrightarrow$ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” $\longleftrightarrow$ “11 1111 1111”) from actual conversion characteristics.
- Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.
- Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB (Ideal)} = \frac{AVRH - AVss}{1024} \quad [\text{V}]$$

N : A/D converter digital output value

$$V_{OT} \text{ (Ideal)} = AVss + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} \text{ (Ideal)} = AVRH - 1.5 \text{ LSB} \quad [\text{V}]$$

VNT : Voltage when the digital output changes from (N - 1) to N

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MB90920 Series

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F922NCPMC MB90F922NCSPMC MB90922NCSPMC MB90F923NCPMC MB90F923NCSPMC MB90F924NCPMC MB90F924NCSPMC	120-pin plastic LQFP (FPT-120P-M21)	
MB90V920-101CR MB90V920-102CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

MEMO