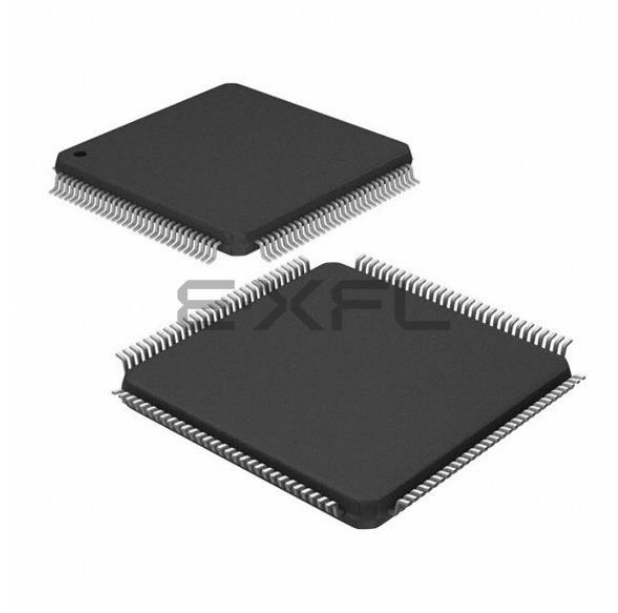
Infineon Technologies - MB90922NCSPMC-GS-136E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-136e1

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type*1	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	$\overline{\text{RST}}$	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

(Continued)

■ HANDLING DEVICES

• Strictly observe maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC}, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

• Supply voltage stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

• Precautions when turning the power on

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μs.

• Handling unused pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

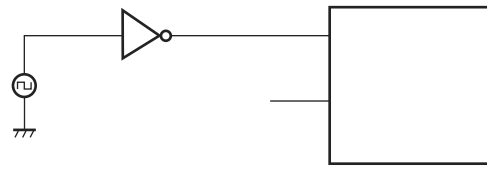
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

• Handling A/D converter power supply pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

• Notes on using an external clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

• **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

• **Crystal oscillator circuit**

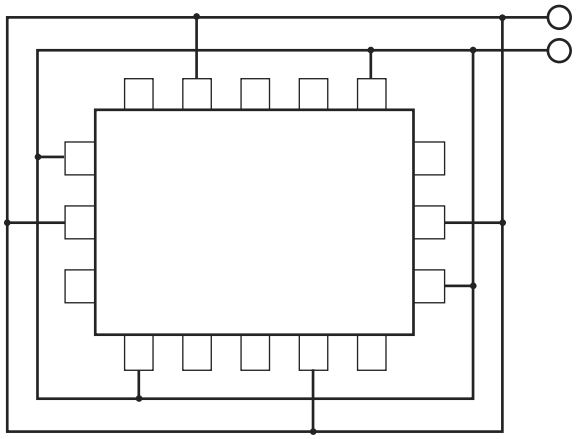
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

• **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

- **Handling the power supply for high-current output buffer pins** (DV_{CC}, DV_{SS})

  - **Flash memory products and MASK ROM products (MB90F922NC/F922NCS/922NCS/F923NC/ F923NCS/F924NC/F924NCS)**

    In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is isolated from the digital power supply (V_{CC}).
    Therefore, DVcc can therefore be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is supplied before the digital power supply (V_{CC}), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply (V_{CC}) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

  - **Evaluation product** (**MB90V920-101**/**MB90V920-102**)

    In the evaluation products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is not isolated from the digital power supply (V_{CC}). Therefore, DV_{CC} must therefore be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) must always be applied after the digital power supply (V_{CC}) has been connected, and disconnected before the digital power supply (Vcc) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).
    Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

- **Pull-up/pull-down resistors**

MB90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

- **Precautions when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

- **Notes on operating when the external clock is stopped**

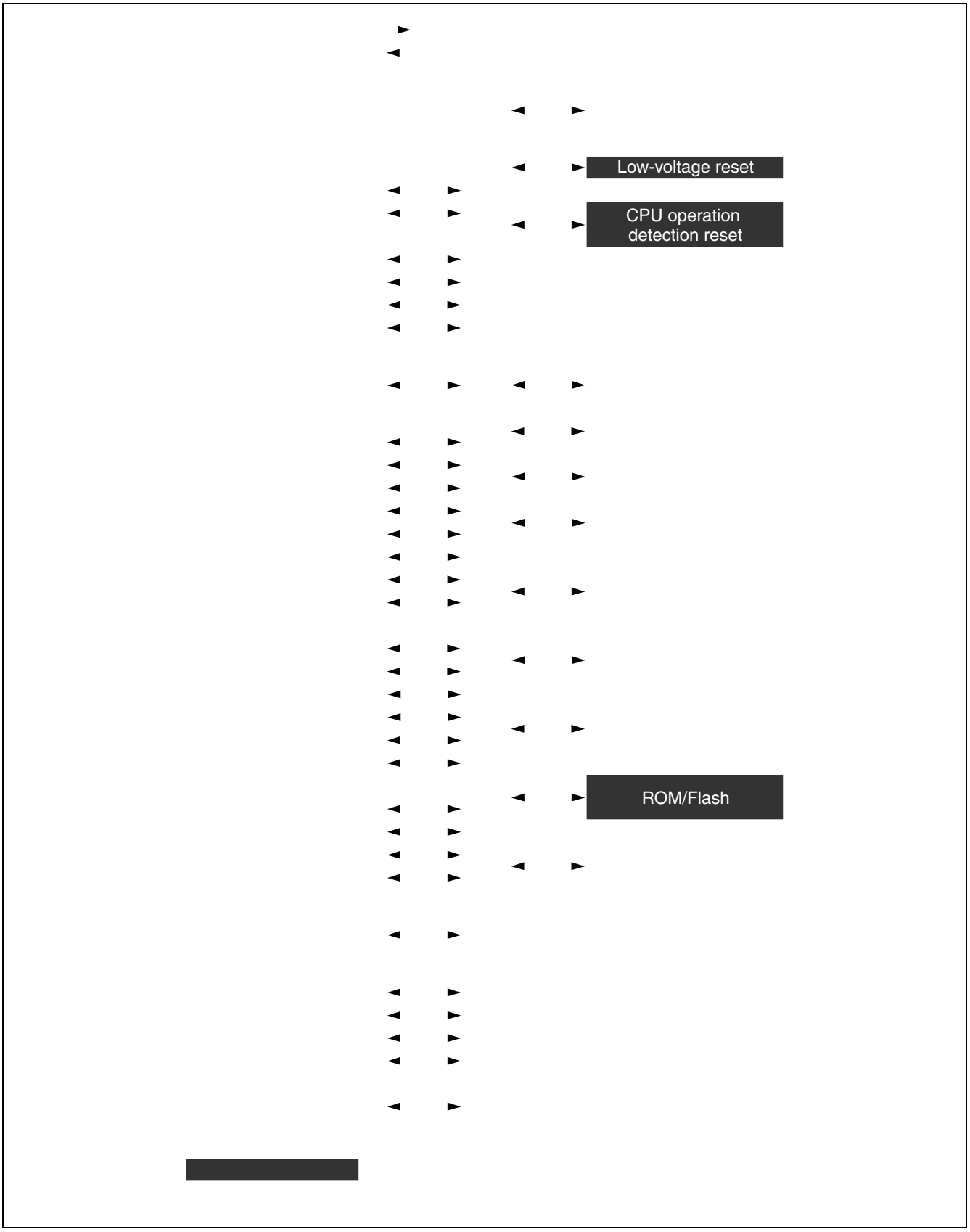
The MB90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

- **Flash memory security function**

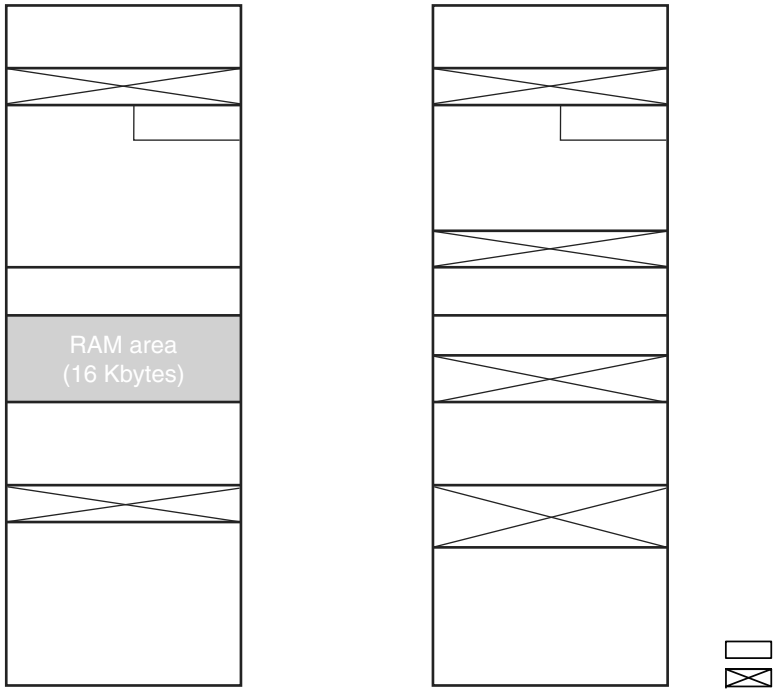
A security bit is located within the Flash memory region. The security function is activated by writing the protection code 01_H to the security bit.
Do not write the value 01_H to this address if you are not using the security function.
Please refer to following table for the address of the security bit.

	Flash memory size	Address for security bit
MB90F922NC MB90F922NCS	Built-in 2 Mbits Flash Memory	$FC0001_H$
MB90F923NCS	Built-in 3 Mbits Flash Memory	$F80001_H$
MB90F924NCS	Built-in 4 Mbits Flash Memory	$F80001_H$

■ BLOCK DIAGRAM



■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000083H	(Disabled)				
000084H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	000000X0B
000085H	(Disabled)				
000086H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	000000X0B
000087H	(Disabled)				
000088H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXX111B
000089H	(Disabled)				
00008AH	A/D setting register 0	ADSR0	R/W	A/D converter	00000000B
00008BH	A/D setting register 1	ADSR1	R/W		00000000B
00008CH	Port input level select 0	PIL0	R/W	Port input level select	00000000B
00008DH	Port input level select 1	PIL1	R/W		XXXX0000B
00008EH	Port input level select 2	PIL2	R/W		XXXX0000B
00008FH to 00009DH	(Disabled)				
00009EH	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0XB
00009FH	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	XXXXXXX0B
0000A0H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000B
0000A1H	Clock select register	CKSCR	R/W, R		11111100B
0000A2H to 0000A7H	(Disabled)				
0000A8H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111B
0000A9H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100B
0000AAH	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000B
0000ABH to 0000ADH	(Disabled)				
0000AEH	Flash memory control status register	FMCS	R/W	Flash interface	000X0000B
0000AFH	(Disabled)				

(Continued)

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

List of Message Buffers (ID Registers)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00H to 003A1FH	003B00H to 003B1FH	003700H to 00371FH	003800H to 00381FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003B20H	003720H	003820H	ID register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
003A21H	003B21H	003721H	003821H				
003A22H	003B22H	003722H	003822H				XXXXX---B XXXXXXXXB
003A23H	003B23H	003723H	003823H				
003A24H	003B24H	003724H	003824H	ID register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
003A25H	003B25H	003725H	003825H				
003A26H	003B26H	003726H	003826H				XXXXX---B XXXXXXXXB
003A27H	003B27H	003727H	003827H				
003A28H	003B28H	003728H	003828H	ID register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
003A29H	003B29H	003729H	003829H				
003A2AH	003B2AH	00372AH	00382AH				XXXXX---B XXXXXXXXB
003A2BH	003B2BH	00372BH	00382BH				
003A2CH	003B2CH	00372CH	00382CH	ID register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
003A2DH	003B2DH	00372DH	00382DH				
003A2EH	003B2EH	00372EH	00382EH				XXXXX---B XXXXXXXXB
003A2FH	003B2FH	00372FH	00382FH				
003A30H	003B30H	003730H	003830H	ID register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
003A31H	003B31H	003731H	003831H				
003A32H	003B32H	003732H	003832H				XXXXX---B XXXXXXXXB
003A33H	003B33H	003733H	003833H				
003A34H	003B34H	003734H	003834H	ID register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
003A35H	003B35H	003735H	003835H				
003A36H	003B36H	003736H	003836H				XXXXX---B XXXXXXXXB
003A37H	003B37H	003737H	003837H				
003A38H	003B38H	003738H	003838H	ID register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
003A39H	003B39H	003739H	003839H				
003A3AH	003B3AH	00373AH	00383AH				XXXXX---B XXXXXXXXB
003A3BH	003B3BH	00373BH	00383BH				
003A3CH	003B3CH	00373CH	00383CH	ID register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
003A3DH	003B3DH	00373DH	00383DH				
003A3EH	003B3EH	00373EH	00383EH				XXXXX---B XXXXXXXXB
003A3FH	003B3FH	00373FH	00383FH				

(Continued)

List of Message Buffers (DLC Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A60H	003B60H	003760H	003860H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003B61H	003761H	003861H				
003A62H	003B62H	003762H	003862H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003B63H	003763H	003863H				
003A64H	003B64H	003764H	003864H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003B65H	003765H	003865H				
003A66H	003B66H	003766H	003866H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003B67H	003767H	003867H				
003A68H	003B68H	003768H	003868H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003B69H	003769H	003869H				
003A6AH	003B6AH	00376AH	00386AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003B6BH	00376BH	00386BH				
003A6CH	003B6CH	00376CH	00386CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003B6DH	00376DH	00386DH				
003A6EH	003B6EH	00376EH	00386EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003B6FH	00376FH	00386FH				
003A70H	003B70H	003770H	003870H	DLC register 8	DLCR8	R/W	----XXXXB
003A71H	003B71H	003771H	003871H				
003A72H	003B72H	003772H	003872H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003B73H	003773H	003873H				
003A74H	003B74H	003774H	003874H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003B75H	003775H	003875H				
003A76H	003B76H	003776H	003876H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003B77H	003777H	003877H				
003A78H	003B78H	003778H	003878H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003B79H	003779H	003879H				
003A7AH	003B7AH	00377AH	00387AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003B7BH	00377BH	00387BH				
003A7CH	003B7CH	00377CH	00387CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003B7DH	00377DH	00387DH				
003A7EH	003B7EH	00377EH	00387EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003B7FH	00377FH	00387FH				

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
CAN0 received/CAN2 received	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	0CH	FFFFCCH			
CAN1 received/CAN3 received	×	#13	0DH	FFFFC8H	ICR01	0000B1H*1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	0EH	FFFFC4H			
Input capture 0	△	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10H	FFFFBCH			
Reload timer 0	△	#17	11H	FFFFB8H	ICR03	0000B3H*1	
Reload timer 2	△	#18	12H	FFFFB4H			
Input capture 1	△	#19	13H	FFFFB0H	ICR04	0000B4H*1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14H	FFFFACH			
Input capture 2	△	#21	15H	FFFFA8H	ICR05	0000B5H*1	
Reload timer 3	△	#22	16H	FFFFA4H			
Input capture 3/4/5/6/7	△	#23	17H	FFFFA0H	ICR06	0000B6H*1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18H	FFFF9CH			
PPG timer 0	△	#25	19H	FFFF98H	ICR07	0000B7H*1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1AH	FFFF94H			
PPG timer 1	△	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Reload timer 1	△	#28	1CH	FFFF8CH			
PPG timer 2/3/4/5	○	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Real time watch timer watch timer (sub clock)	×	#30	1EH	FFFF84H			
Free-run timer overflow/clear	×	#31	1FH	FFFF80H	ICR10	0000BAH *1	
A/D converter conversion complete	○	#32	20H	FFFF7CH			
Sound generator 0/1	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Time-base timer	×	#34	22H	FFFF74H			
UART2 RX	○	#35	23H	FFFF70H	ICR12	0000BCH*1	
UART2 TX	△	#36	24H	FFFF6CH			Low

(Continued)

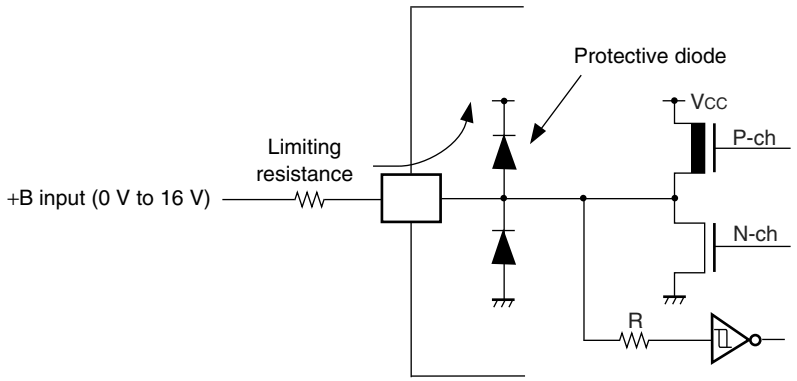
(Continued)

*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit



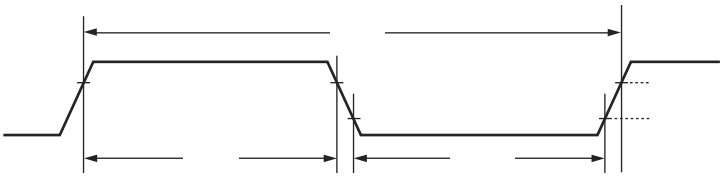
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

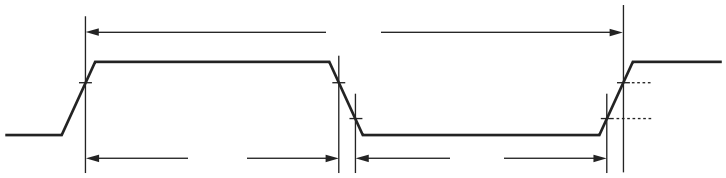
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = –30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product

(Continued)

• X0, X1 clock timing



• X0A, X1A clock timing



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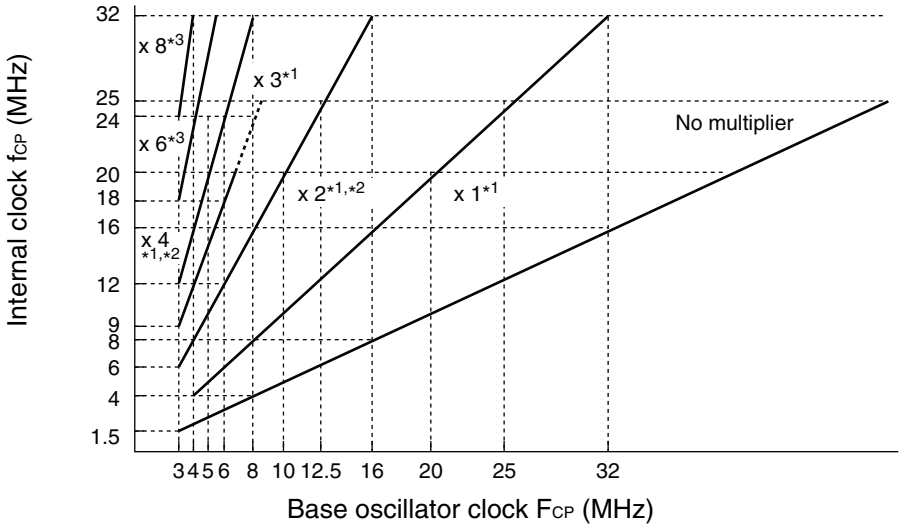
Base oscillator frequency vs. Internal operating clock frequency



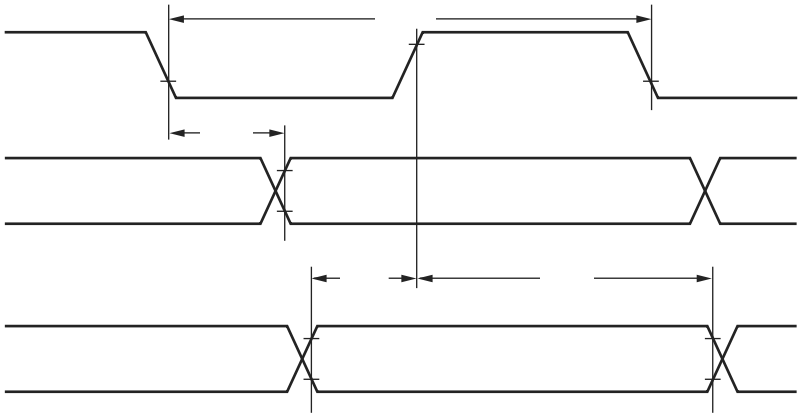
*1 : When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example] When using a base oscillator frequency of 24 MHz at PLL × 1 :
CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4,CS2 bit = "1"
[Example] When using a base oscillator frequency of 6 MHz at PLL × 3 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, the following settings are also supported.
PLL × 2 : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4 : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

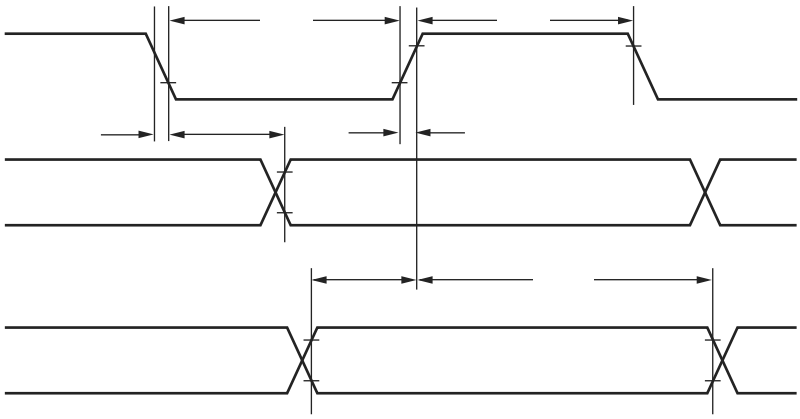
*3 : When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example] When using a base oscillator frequency of 4 MHz at PLL × 6 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"
[Example] When using a base oscillator frequency of 3 MHz at PLL × 8 :
CKSCR register : CS1 bit = "1", CS0 bit = "1"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

- Internal shift clock mode



- External shift clock mode

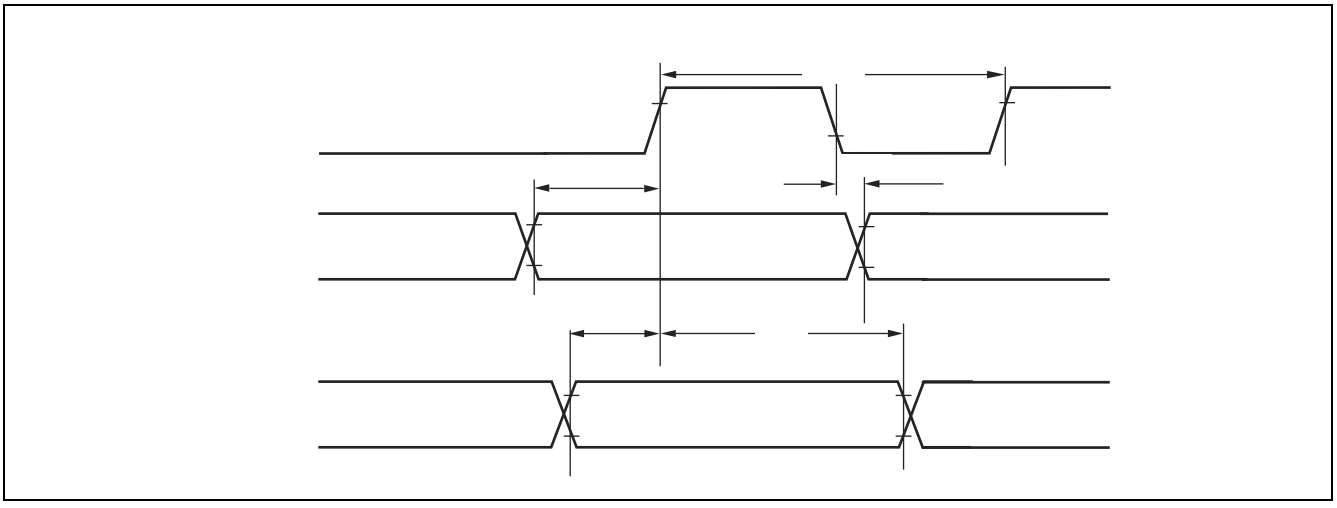


• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.



6. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	0.9	3.6	s	Excludes pre-programming before erase
Word (16-bit width) programming time		—	23	370	µs	Excludes system-level overhead
Chip programming time	T_A = + 25 °C, V_{CC} = 5.0 V	—	3.4	55	s	
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

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Edited: Sales Promotion Department