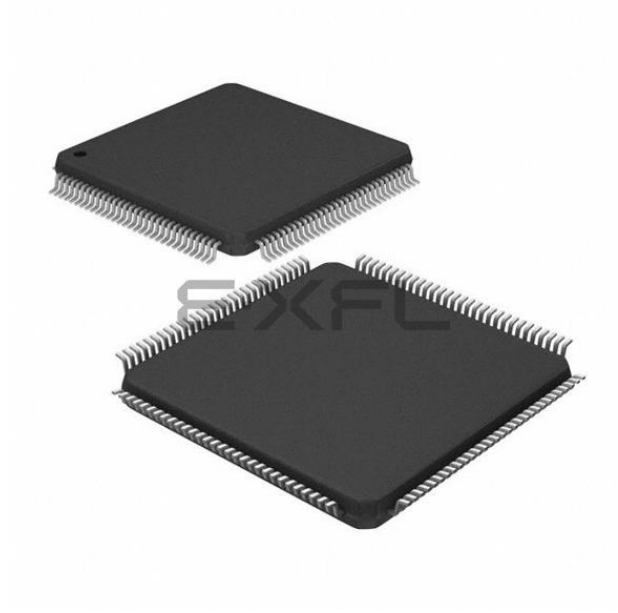
Infineon Technologies - MB90922NCSPMC-GS-137E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-137e1

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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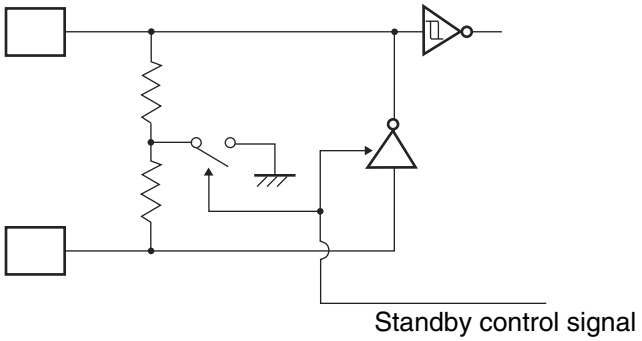
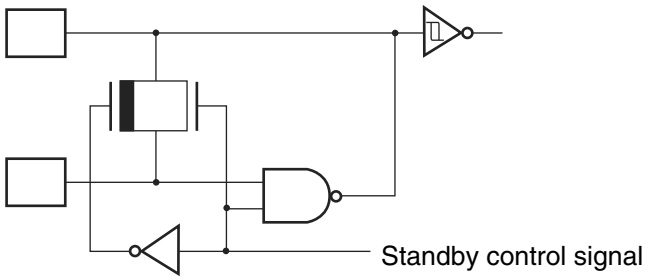
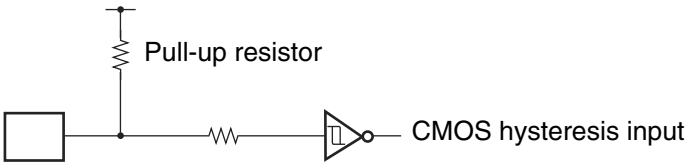
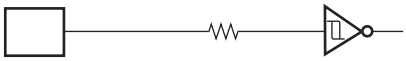
- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at f_{CP} = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance : approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) • Attached pull-up resistor : approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.

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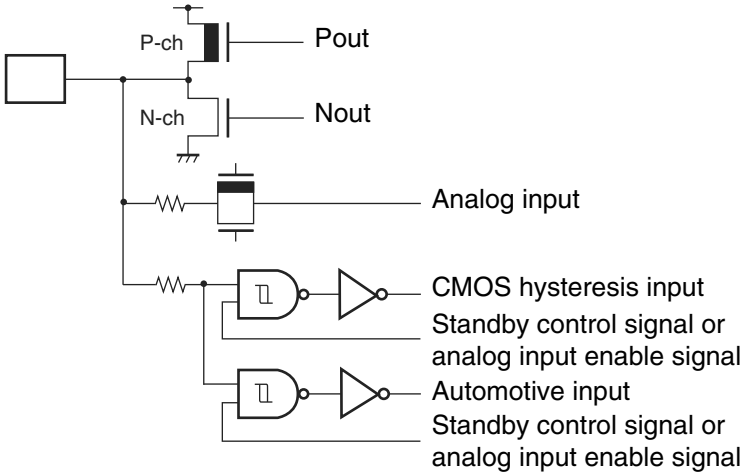
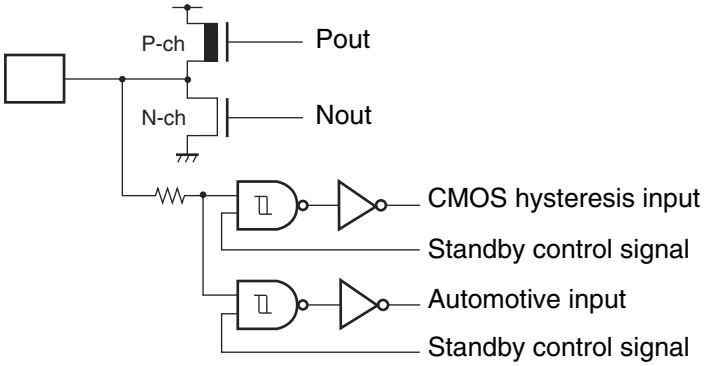
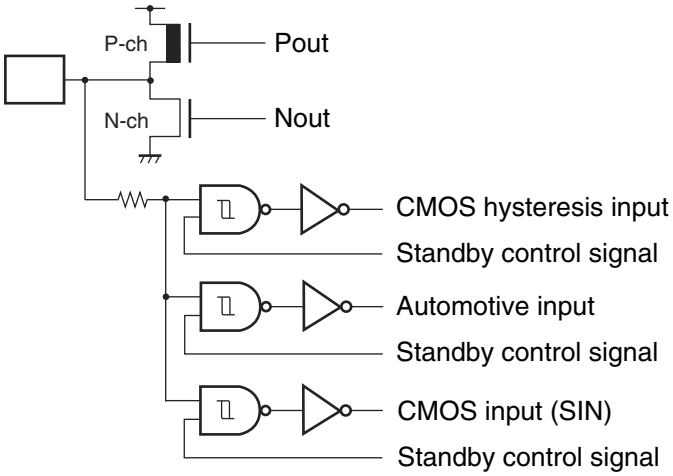
Type	Circuit	Remarks
H		A/D converter input common general-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
I		General-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
J		General-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

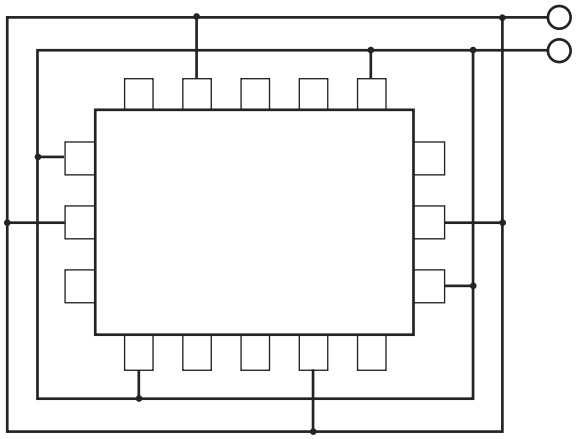
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



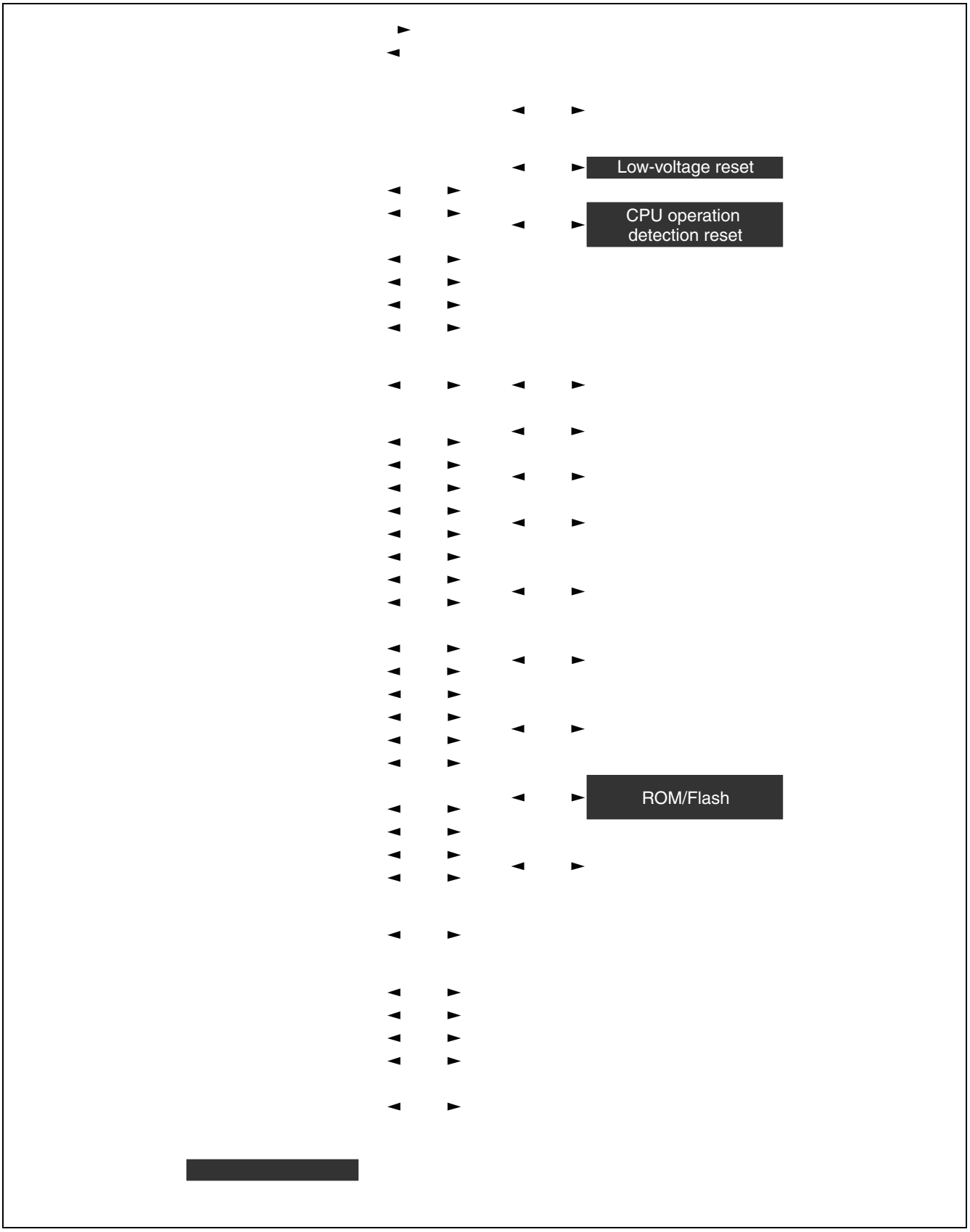
Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

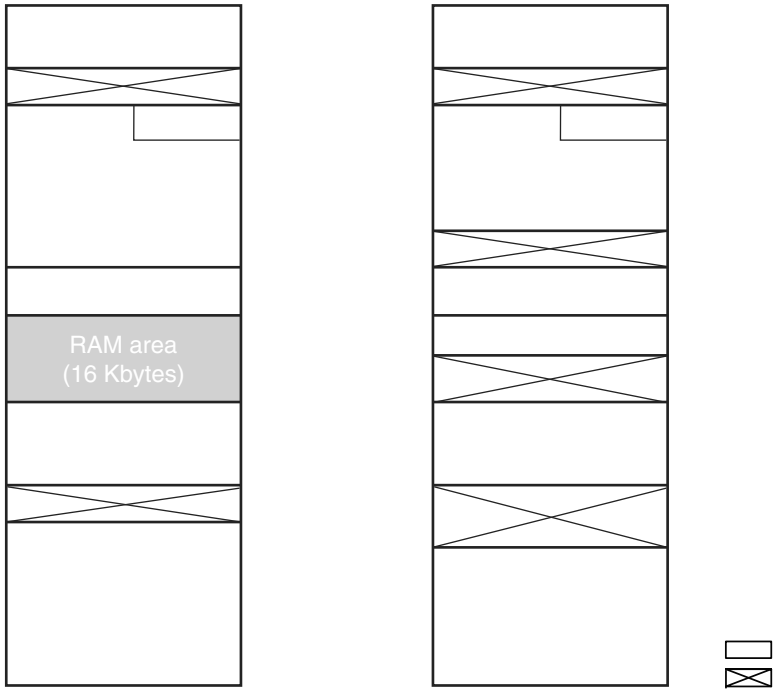
- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ BLOCK DIAGRAM



■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000D4H	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000B
0000D5H	Higher timer control status register 2	TMCSR2H	R/W		XXX10000B
0000D6H	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000B
0000D7H	Higher timer control status register 3	TMCSR3H	R/W		XXX10000B
0000D8H	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000B
0000D9H	Higher sound control register 1	SGCRH1	R/W		0XXXX100B
0000DAH	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000B
0000DBH	Higher PPG3 control status register	PCNTH3	R/W		00000001B
0000DCH	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000B
0000DDH	Higher PPG4 control status register	PCNTH4	R/W		00000001B
0000DEH	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000B
0000DFH	Higher PPG5 control status register	PCNTH5	R/W		00000001B
0000E0H	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000B
0000E1H	Serial control register 2	SCR2	R/W, W		00000000B
0000E2H	Reception/transmission data register 2	RDR2/ TDR2	R/W		00000000B
0000E3H	Serial status register 2	SSR2	R/W, R		00001000B
0000E4H	Extended communication control register 2	ECCR2	R/W, R		000000XXB
0000E5H	Extended status control register 2	ESCR2	R/W		00000100B
0000E6H	Baud rate generator register 20	BGR20	R/W		00000000B
0000E7H	Baud rate generator register 21	BGR21	R/W, R		00000000B
0000E8H	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000B
0000E9H	Serial control register 3	SCR3	R/W, W		00000000B
0000EAH	Reception/transmission data register 3	RDR3/ TDR3	R/W		00000000B
0000EBH	Serial status register 3	SSR3	R/W, R		00001000B
0000ECH	Extended communication control register 3	ECCR3	R/W, R		000000XXB
0000EDH	Extended status control register 3	ESCR3	R/W		00000100B
0000EEH	Baud rate generator register 30	BGR30	R/W		00000000B
0000EFH	Baud rate generator register 31	BGR31	R/W, R		00000000B
001FF0H	Program address detection register 0	PADR0	R/W	Address match detection	XXXXXXXXB
001FF1H	Program address detection register 1	PADR0	R/W		XXXXXXXXB
001FF2H	Program address detection register 2	PADR0	R/W		XXXXXXXXB
001FF3H	Program address detection register 3	PADR1	R/W		XXXXXXXXB
001FF4H	Program address detection register 4	PADR1	R/W		XXXXXXXXB
001FF5H	Program address detection register 5	PADR1	R/W		XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003970H to 003973H	(Disabled)				
003974H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXXB
003975H	Amplitude data register 1	SGAR1	R/W		00000000B
003976H	Decrement grade register 1	SGDR1	R/W		XXXXXXXXB
003977H	Tone count register 1	SGTR1	R/W		XXXXXXXXB
003978H to 00397FH	(Disabled)				
003980H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXXB
003981H					XXXXXXXXB
003982H	PWM2 compare register 0	PWC20	R/W		XXXXXXXXB
003983H					XXXXXXXXB
003984H	PWM1 select register 0	PWS10	R/W		00000000B
003985H	PWM2 select register 0	PWS20	R/W		X0000000B
003986H, 003987H	(Disabled)				
003988H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXXB
003989H					XXXXXXXXB
00398AH	PWM2 compare register 1	PWC21	R/W		XXXXXXXXB
00398BH					XXXXXXXXB
00398CH	PWM1 select register 1	PWS11	R/W		00000000B
00398DH	PWM2 select register 1	PWS21	R/W		X0000000B
00398EH, 00398FH	(Disabled)				
003990H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXXB
003991H					XXXXXXXXB
003992H	PWM2 compare register 2	PWC22	R/W		XXXXXXXXB
003993H					XXXXXXXXB
003994H	PWM1 select register 2	PWS12	R/W		00000000B
003995H	PWM2 select register 2	PWS22	R/W		X0000000B
003996H, 003997H	(Disabled)				

(Continued)

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Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40H	003B40H	003740H	003840H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003A41H	003B41H	003741H	003841H				
003A42H	003B42H	003742H	003842H				XXXXX---B XXXXXXXXB
003A43H	003B43H	003743H	003843H				
003A44H	003B44H	003744H	003844H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003A45H	003B45H	003745H	003845H				
003A46H	003B46H	003746H	003846H				XXXXX---B XXXXXXXXB
003A47H	003B47H	003747H	003847H				
003A48H	003B48H	003748H	003848H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003A49H	003B49H	003749H	003849H				
003A4AH	003B4AH	00374AH	00384AH				XXXXX---B XXXXXXXXB
003A4BH	003B4BH	00374BH	00384BH				
003A4CH	003B4CH	00374CH	00384CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
003A4DH	003B4DH	00374DH	00384DH				
003A4EH	003B4EH	00374EH	00384EH				XXXXX---B XXXXXXXXB
003A4FH	003B4FH	00374FH	00384FH				
003A50H	003B50H	003750H	003850H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003A51H	003B51H	003751H	003851H				
003A52H	003B52H	003752H	003852H				XXXXX---B XXXXXXXXB
003A53H	003B53H	003753H	003853H				
003A54H	003B54H	003754H	003854H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003A55H	003B55H	003755H	003855H				
003A56H	003B56H	003756H	003856H				XXXXX---B XXXXXXXXB
003A57H	003B57H	003757H	003857H				
003A58H	003B58H	003758H	003858H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003A59H	003B59H	003759H	003859H				
003A5AH	003B5AH	00375AH	00385AH				XXXXX---B XXXXXXXXB
003A5BH	003B5BH	00375BH	00385BH				
003A5CH	003B5CH	00375CH	00385CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
003A5DH	003B5DH	00375DH	00385DH				
003A5EH	003B5EH	00375EH	00385EH				XXXXX---B XXXXXXXXB
003A5FH	003B5FH	00375FH	00385FH				

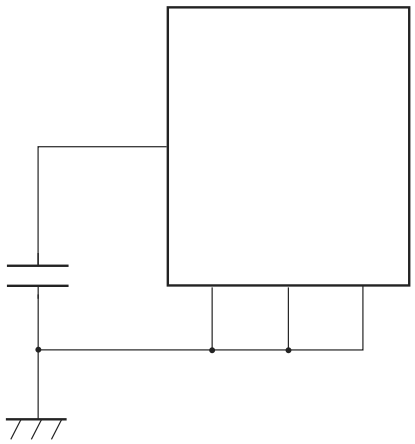
2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.0	5.5	V	The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
		4.4	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin.
Operating temperature	T_A	− 40	+ 105	°C	

* : Refer to the following diagram for details on the connection of the smoothing capacitor C_S.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = –30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product

(Continued)

4. AC Characteristics

(1) Clock timing

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

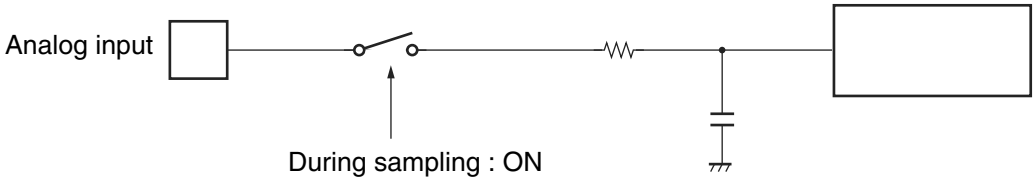
*1 : The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	12.1 kΩ (Max)	8.5 pF (Max)

MB90V920-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

Note : The values are reference values.

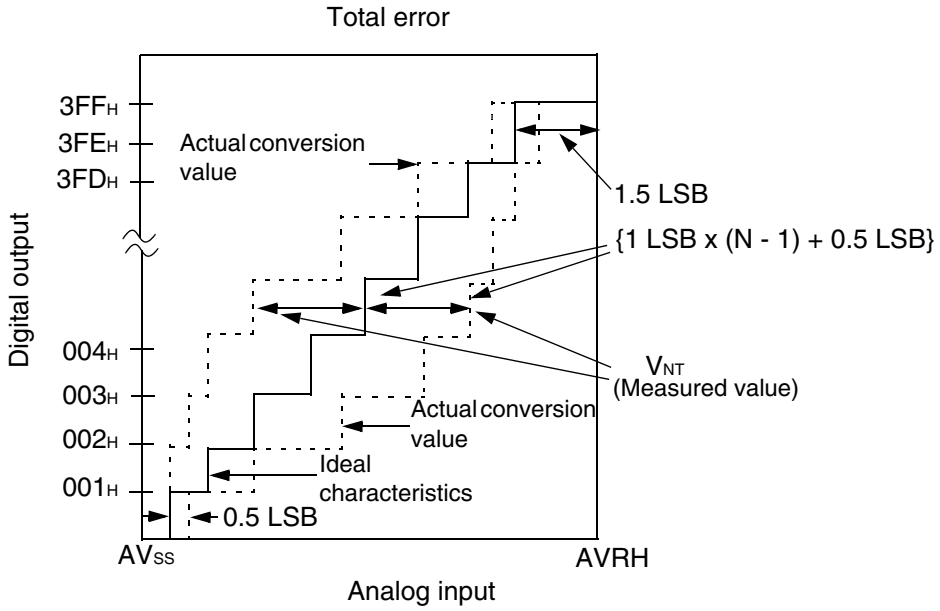
(2) Definition of terms

Resolution : Analog changes that are identifiable by the A/D converter.

Non-Linear error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ←→ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111") from actual conversion characteristics.

Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.

Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

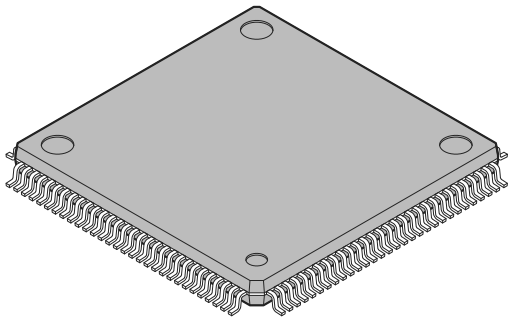
V_{OT} (Ideal) = AVss + 0.5 LSB [V]

V_{FST} (Ideal) = AVRH − 1.5 LSB [V]

V_{NT} : Voltage when the digital output changes from (N - 1) to N

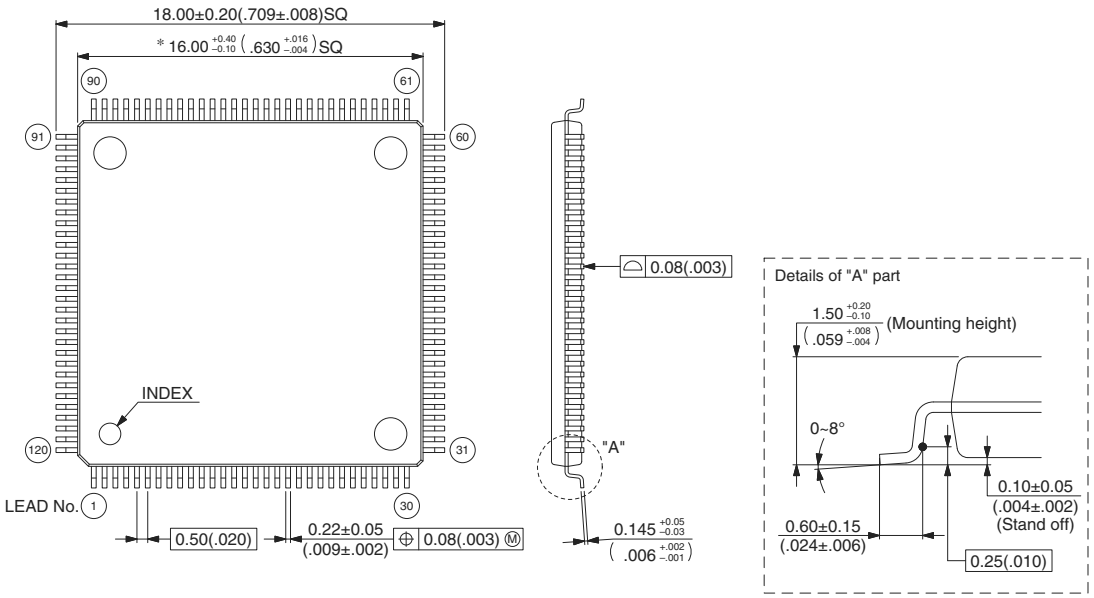
(Continued)

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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