Infineon Technologies - MB90922NCSPMC-GS-139E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-139e1

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Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

- **Serial communication**

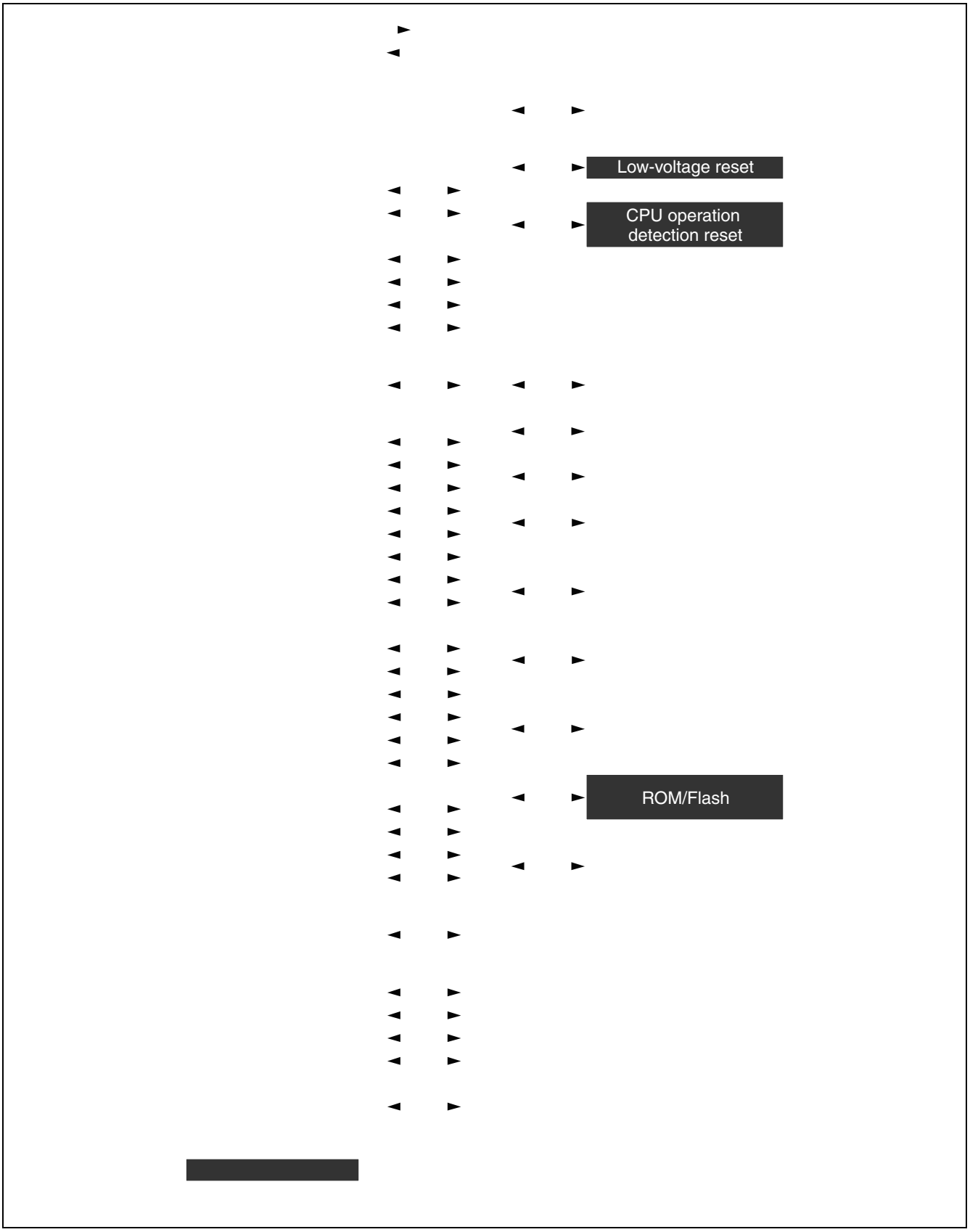
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

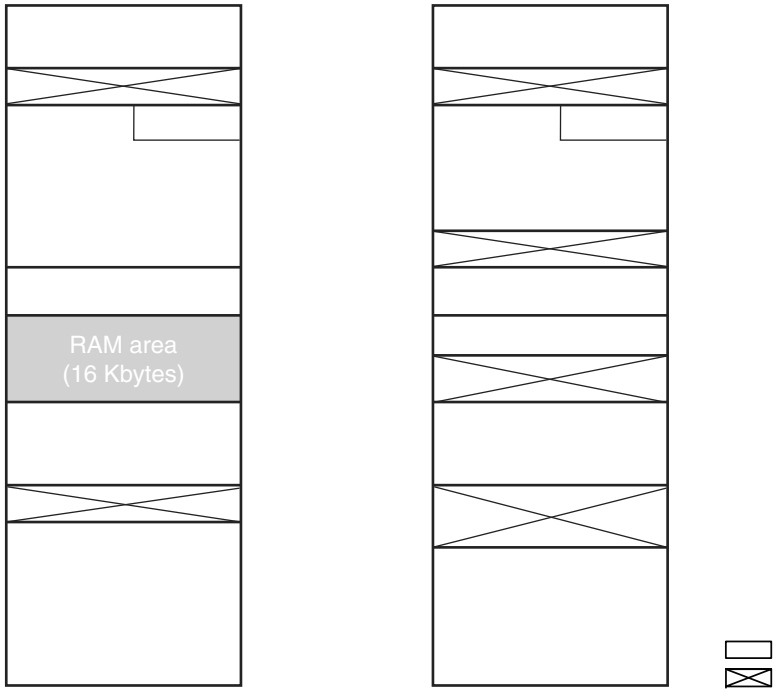
In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ BLOCK DIAGRAM



■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000083H	(Disabled)				
000084H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	000000X0B
000085H	(Disabled)				
000086H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	000000X0B
000087H	(Disabled)				
000088H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXX111B
000089H	(Disabled)				
00008AH	A/D setting register 0	ADSR0	R/W	A/D converter	00000000B
00008BH	A/D setting register 1	ADSR1	R/W		00000000B
00008CH	Port input level select 0	PIL0	R/W	Port input level select	00000000B
00008DH	Port input level select 1	PIL1	R/W		XXXX0000B
00008EH	Port input level select 2	PIL2	R/W		XXXX0000B
00008FH to 00009DH	(Disabled)				
00009EH	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0XB
00009FH	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	XXXXXXX0B
0000A0H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000B
0000A1H	Clock select register	CKSCR	R/W, R		11111100B
0000A2H to 0000A7H	(Disabled)				
0000A8H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111B
0000A9H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100B
0000AAH	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000B
0000ABH to 0000ADH	(Disabled)				
0000AEH	Flash memory control status register	FMCS	R/W	Flash interface	000X0000B
0000AFH	(Disabled)				

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111B
0000B1H	Interrupt control register 01	ICR01	R/W		00000111B
0000B2H	Interrupt control register 02	ICR02	R/W		00000111B
0000B3H	Interrupt control register 03	ICR03	R/W		00000111B
0000B4H	Interrupt control register 04	ICR04	R/W		00000111B
0000B5H	Interrupt control register 05	ICR05	R/W		00000111B
0000B6H	Interrupt control register 06	ICR06	R/W		00000111B
0000B7H	Interrupt control register 07	ICR07	R/W		00000111B
0000B8H	Interrupt control register 08	ICR08	R/W		00000111B
0000B9H	Interrupt control register 09	ICR09	R/W		00000111B
0000BAH	Interrupt control register 10	ICR10	R/W		00000111B
0000BBH	Interrupt control register 11	ICR11	R/W		00000111B
0000BCH	Interrupt control register 12	ICR12	R/W		00000111B
0000BDH	Interrupt control register 13	ICR13	R/W		00000111B
0000BEH	Interrupt control register 14	ICR14	R/W		00000111B
0000BFH	Interrupt control register 15	ICR15	R/W		00000111B
0000C0H to 0000C3H	(Disabled)				
0000C4H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000B
0000C5H	Serial control register 1	SCR1	R/W, W		00000000B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000B
0000C7H	Serial status register 1	SSR1	R/W, R		00001000B
0000C8H	Extended communication control register 1	ECCR1	R/W, R		000000XXB
0000C9H	Extended status control register 1	ESCR1	R/W		00000100B
0000CAH	Baud rate generator register 10	BGR10	R/W		00000000B
0000CBH	Baud rate generator register 11	BGR11	R/W, R		00000000B
0000CCH	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0B
0000CDH	Middle watch timer control register	WTCRM	R/W		00000000B
0000CEH	Higher watch timer control register	WTCRH	R/W		XXXXXX00B
0000CFH	Sub clock control register	PSCCR	W	Sub clock	XXXX0000B
0000D0H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000B
0000D1H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXB
0000D2H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000B
0000D3H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XXB

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003944H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXXB
003945H					XXXXXXXXB
003946H	Input capture register 7	IPCP7	R		XXXXXXXXB
003947H					XXXXXXXXB
003948H to 00394FH	(Disabled)				
003950H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXXB
003951H					XXXXXXXXB
003952H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXXB
003953H					XXXXXXXXB
003954H to 003957H	(Disabled)				
003958H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXXB
003959H					XXXXXXXXB
00395AH					XXXXXXXXB
00395BH	Second data register	WTSR	R/W		XX000000B
00395CH	Minute data register	WTMR	R/W		XX000000B
00395DH	Hour data register	WTHR	R/W		XXX00000B
00395EH	Day data register	WTDR	R/W		00X00001B
00395FH	(Disabled)				
003960H	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXXB
003961H					XXXXXXXXB
003962H					XXXXXXXXB
003963H					XXXXXXXXB
003964H					XXXXXXXXB
003965H					XXXXXXXXB
003966H					XXXXXXXXB
003967H					XXXXXXXXB
003968H					XXXXXXXXB
003969H					XXXXXXXXB
00396AH					XXXXXXXXB
00396BH					XXXXXXXXB
00396CH					XXXXXXXXB
00396DH					XXXXXXXXB
00396EH					XXXXXXXXB
00396FH					XXXXXXXXB

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■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

(Continued)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40H	003B40H	003740H	003840H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003A41H	003B41H	003741H	003841H				
003A42H	003B42H	003742H	003842H				XXXXX---B XXXXXXXXB
003A43H	003B43H	003743H	003843H				
003A44H	003B44H	003744H	003844H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003A45H	003B45H	003745H	003845H				
003A46H	003B46H	003746H	003846H				XXXXX---B XXXXXXXXB
003A47H	003B47H	003747H	003847H				
003A48H	003B48H	003748H	003848H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003A49H	003B49H	003749H	003849H				
003A4AH	003B4AH	00374AH	00384AH				XXXXX---B XXXXXXXXB
003A4BH	003B4BH	00374BH	00384BH				
003A4CH	003B4CH	00374CH	00384CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
003A4DH	003B4DH	00374DH	00384DH				
003A4EH	003B4EH	00374EH	00384EH				XXXXX---B XXXXXXXXB
003A4FH	003B4FH	00374FH	00384FH				
003A50H	003B50H	003750H	003850H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003A51H	003B51H	003751H	003851H				
003A52H	003B52H	003752H	003852H				XXXXX---B XXXXXXXXB
003A53H	003B53H	003753H	003853H				
003A54H	003B54H	003754H	003854H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003A55H	003B55H	003755H	003855H				
003A56H	003B56H	003756H	003856H				XXXXX---B XXXXXXXXB
003A57H	003B57H	003757H	003857H				
003A58H	003B58H	003758H	003858H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003A59H	003B59H	003759H	003859H				
003A5AH	003B5AH	00375AH	00385AH				XXXXX---B XXXXXXXXB
003A5BH	003B5BH	00375BH	00385BH				
003A5CH	003B5CH	00375CH	00385CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
003A5DH	003B5DH	00375DH	00385DH				
003A5EH	003B5EH	00375EH	00385EH				XXXXX---B XXXXXXXXB
003A5FH	003B5FH	00375FH	00385FH				

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
CAN0 received/CAN2 received	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	0CH	FFFFCCH			
CAN1 received/CAN3 received	×	#13	0DH	FFFFC8H	ICR01	0000B1H*1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	0EH	FFFFC4H			
Input capture 0	△	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10H	FFFFBCH			
Reload timer 0	△	#17	11H	FFFFB8H	ICR03	0000B3H*1	
Reload timer 2	△	#18	12H	FFFFB4H			
Input capture 1	△	#19	13H	FFFFB0H	ICR04	0000B4H*1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14H	FFFFACH			
Input capture 2	△	#21	15H	FFFFA8H	ICR05	0000B5H*1	
Reload timer 3	△	#22	16H	FFFFA4H			
Input capture 3/4/5/6/7	△	#23	17H	FFFFA0H	ICR06	0000B6H*1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18H	FFFF9CH			
PPG timer 0	△	#25	19H	FFFF98H	ICR07	0000B7H*1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1AH	FFFF94H			
PPG timer 1	△	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Reload timer 1	△	#28	1CH	FFFF8CH			
PPG timer 2/3/4/5	○	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Real time watch timer watch timer (sub clock)	×	#30	1EH	FFFF84H			
Free-run timer overflow/clear	×	#31	1FH	FFFF80H	ICR10	0000BAH *1	
A/D converter conversion complete	○	#32	20H	FFFF7CH			
Sound generator 0/1	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Time-base timer	×	#34	22H	FFFF74H			
UART2 RX	○	#35	23H	FFFF70H	ICR12	0000BCH*1	
UART2 TX	△	#36	24H	FFFF6CH			Low

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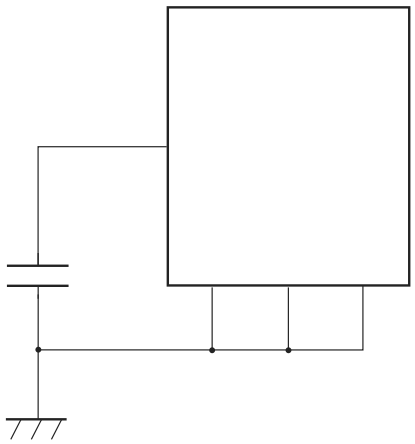
2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.0	5.5	V	The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
		4.4	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin.
Operating temperature	T_A	− 40	+ 105	°C	

* : Refer to the following diagram for details on the connection of the smoothing capacitor C_S.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHA}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHC}	—	—	0.7 V_{CC}	—	—	V	$\overline{RST}$ input pin (CMOS hysteresis)
"L" level input voltage	V_{ILA}	—	—	—	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	—	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	—	—	0.3 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
Power supply current*	I_{CC}	V_{CC}	Maximum operating frequency F_{CP} = 32 MHz, normal operation	—	35	45	mA	
			Maximum operating frequency F_{CP} = 32 MHz, writing Flash memory	—	55	65	mA	
	I_{CCS}		Operating frequency F_{CP} = 32 MHz, sleep mode	—	13	20	mA	
	I_{CTS}		Operating frequency F_{CP} = 2 MHz, time-base timer mode	—	0.6	1.0	mA	
	I_{CTSPLL}		Operating frequency F_{CP} = 32 MHz, PLL timer mode, External frequency = 4 MHz	—	2.5	4	mA	
	I_{CCL}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub clock operation	—	120	270	µA	
	I_{CCLS}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub sleep operation	—	100	200	µA	
	I_{CCT}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, watch mode	—	90	180	µA	
	I_{CCH}		T_A = + 25 °C, stop mode	—	80	170	µA	

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4. AC Characteristics

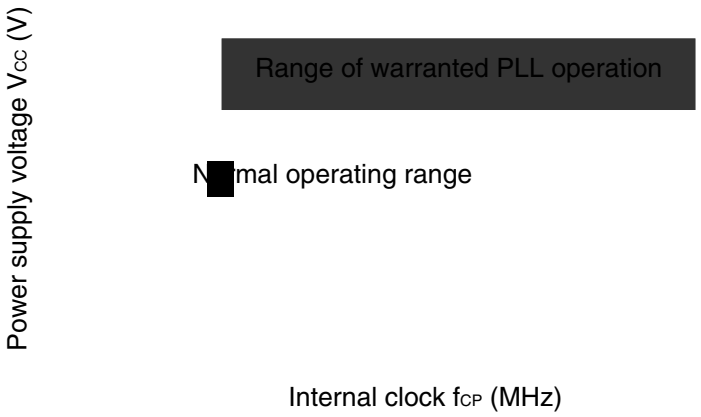
(1) Clock timing

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage



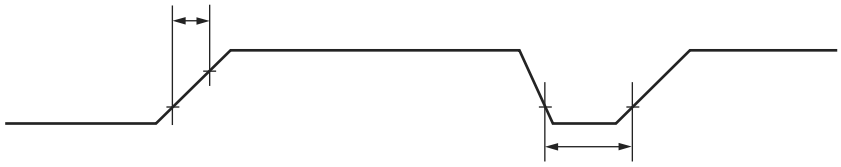
Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

(Continued)

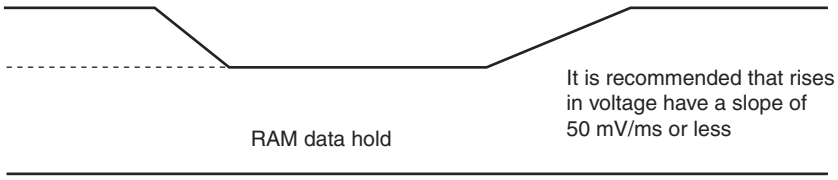
(3) Power-on reset

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

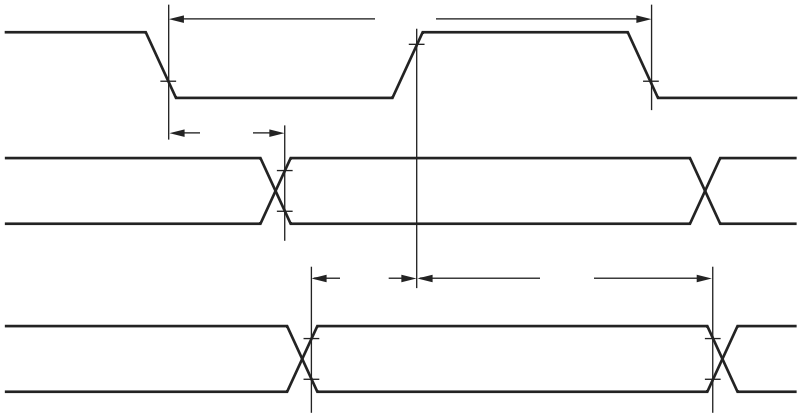
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	VCC	—	0.05	30	ms	
Power off time	t_{OFF}			1	—	ms	Waiting time until power-on



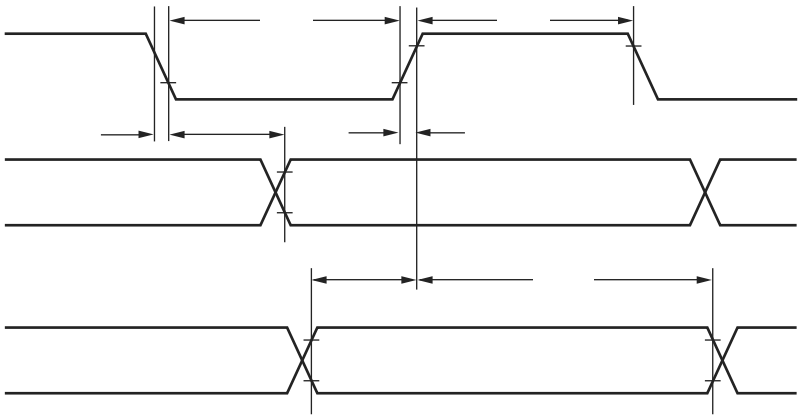
Note : Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



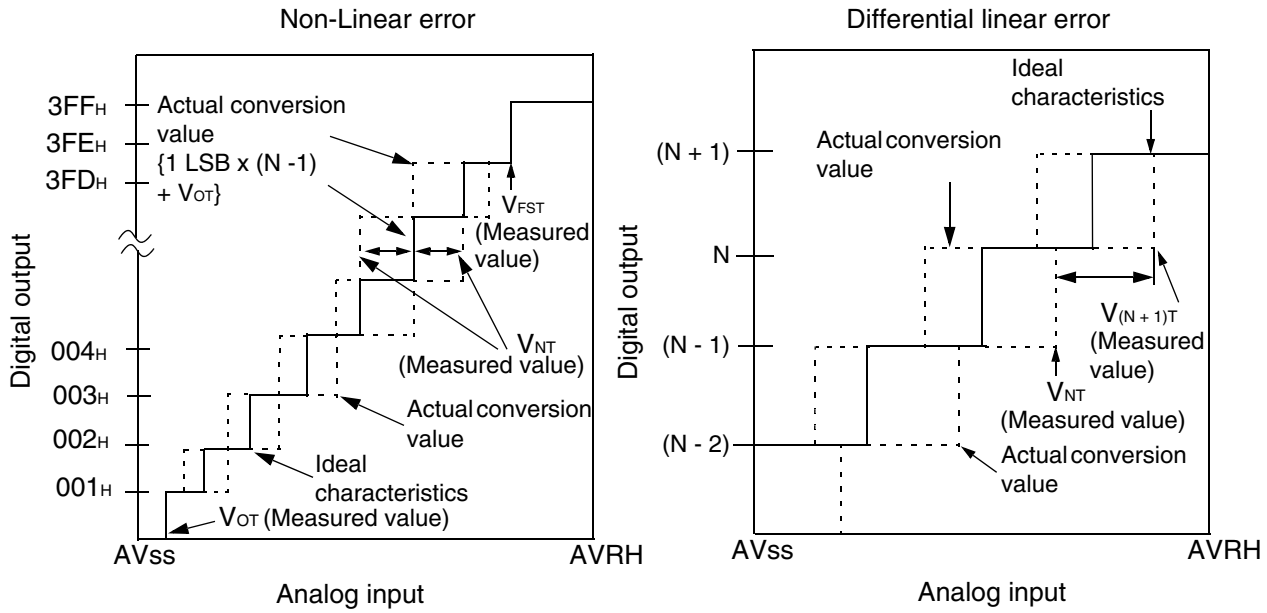
- Internal shift clock mode



- External shift clock mode



(Continued)



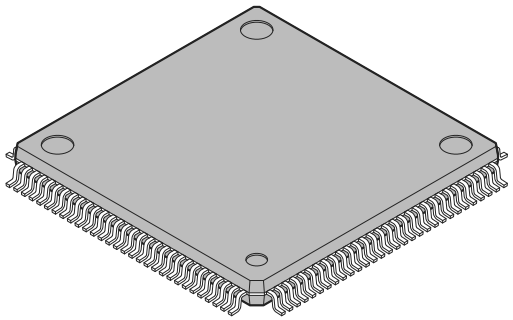
$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

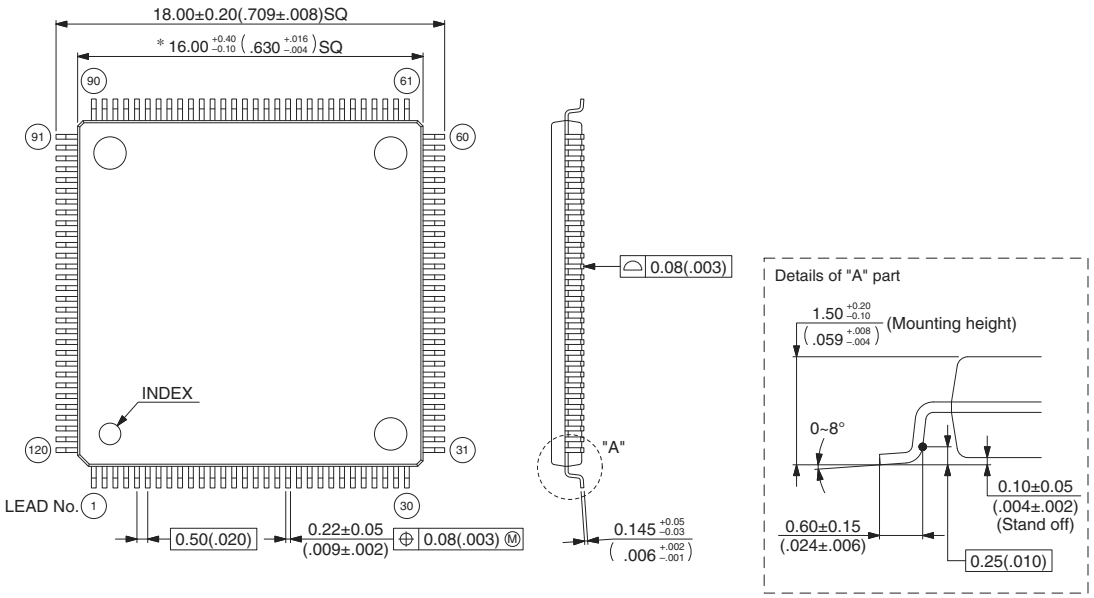
N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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