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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-140e1

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- 16-bit reload timer (4 channels)
16-bit reload timer operation (select toggle output or one-shot output)
Selectable event count function
- Real time watch timer (main clock)
Operates directly from oscillator clock.
Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
Output pins (3 channels), external trigger input pin (1 channel)
Operation clock frequencies : f_{CP} , $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
Generates interrupt for task switching.
Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
8-channel independent operation
Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
Conversion time : 3 μ s (at $f_{CP} = 32$ MHz)
External trigger activation available (P50/INT0/ADTG)
Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
Equipped with full duplex double buffer
Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
Conforms to CAN specifications version 2.0 Part A and B.
Automatic resend in case of error.
Automatic transfer in response to remote frame.
16 prioritized message buffers for data and ID
Multiple message support
Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
Supports up to 1 Mbps
CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
Automatic reset when low voltage is detected
Program looping detection function
- Stepping motor controller (4 channels)
High current output for each channel $\times 4$
Synchronized 8/10-bit PWM for each channel $\times 2$
- Sound generator (2 channels)
8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at $f_{CP} = 32$ MHz)
Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
Automotive/CMOS-Schmitt
- Flash memory security function
Protects the contents of Flash memory (Flash memory product only)

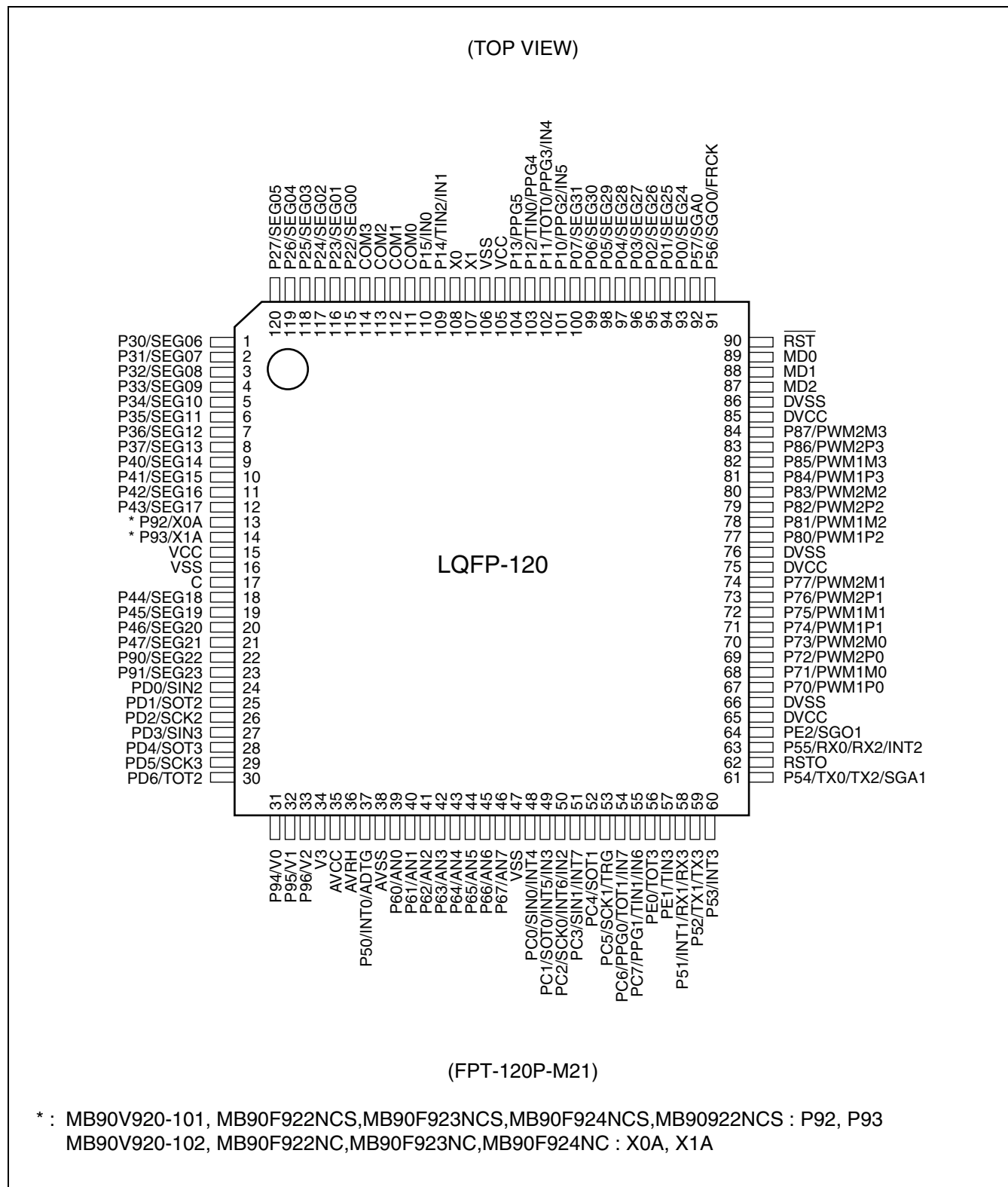
MB90920 Series

■ PRODUCT LINEUP

Part number Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F ² MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes						No		
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V						4.5 V to 5.5 V		
Package	LQFP-120						PGA-299		

MB90920 Series

PIN ASSIGNMENT



Pin no.	Pin name	I/O circuit type*1	Function
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin

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Pin no.	Pin name	I/O circuit type*1	Function
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin

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MB90920 Series

Pin no.	Pin name	I/O circuit type*1	Function
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin
52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin

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MB90920 Series

Type	Circuit	Remarks
H		A/D converter input common general-purpose port • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
I		General-purpose port • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
J		General-purpose port (serial input) • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)

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■ HANDLING DEVICES

• Strictly observe maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between V_{CC} and V_{SS} pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC} , AV_{RH}), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC} , AV_{RH}) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

• Supply voltage stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the V_{CC} power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

• Precautions when turning the power on

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μ s.

• Handling unused pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 k Ω .

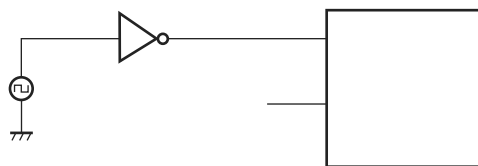
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 k Ω or more.

• Handling A/D converter power supply pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVR_{H} = V_{SS}$.

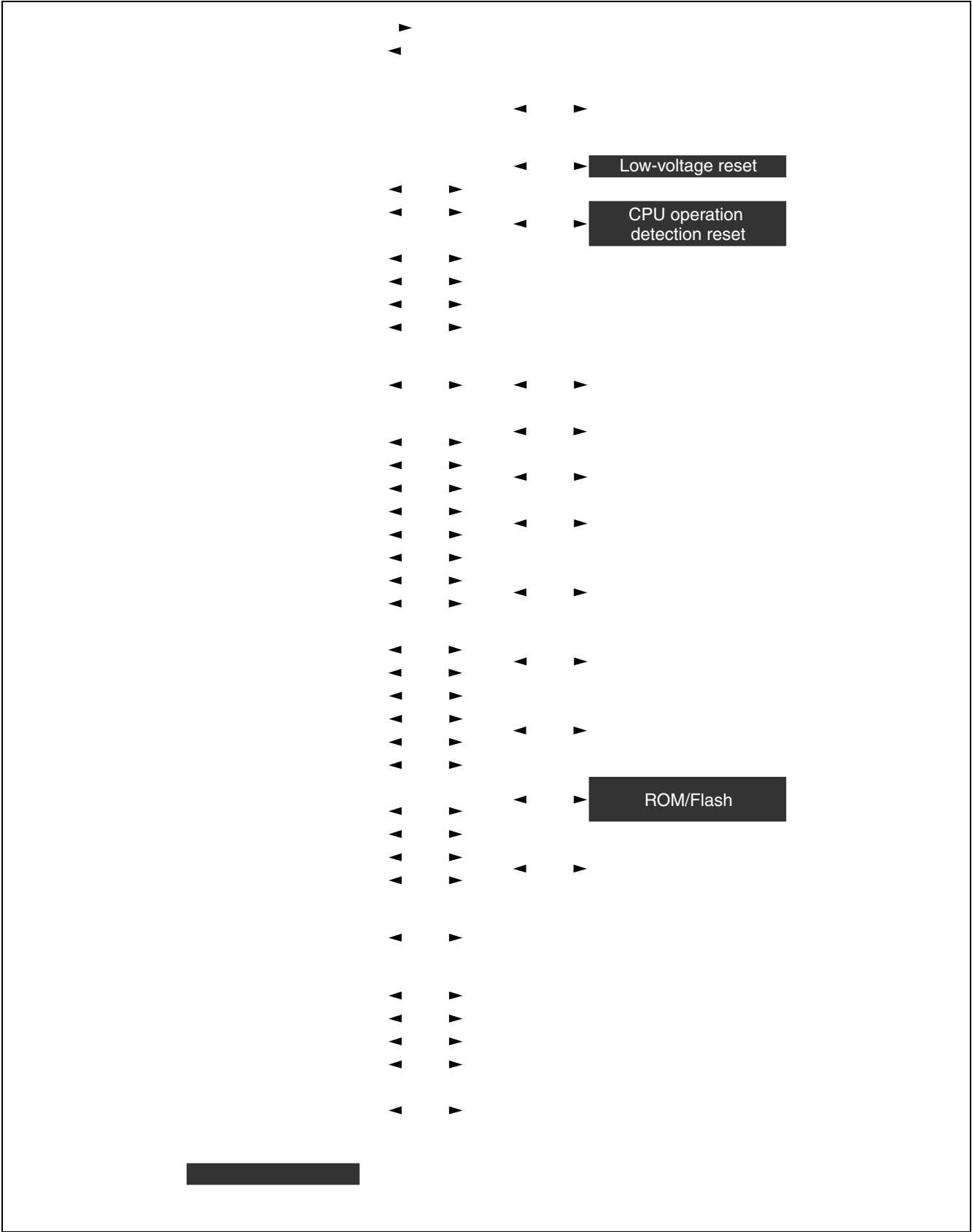
• Notes on using an external clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



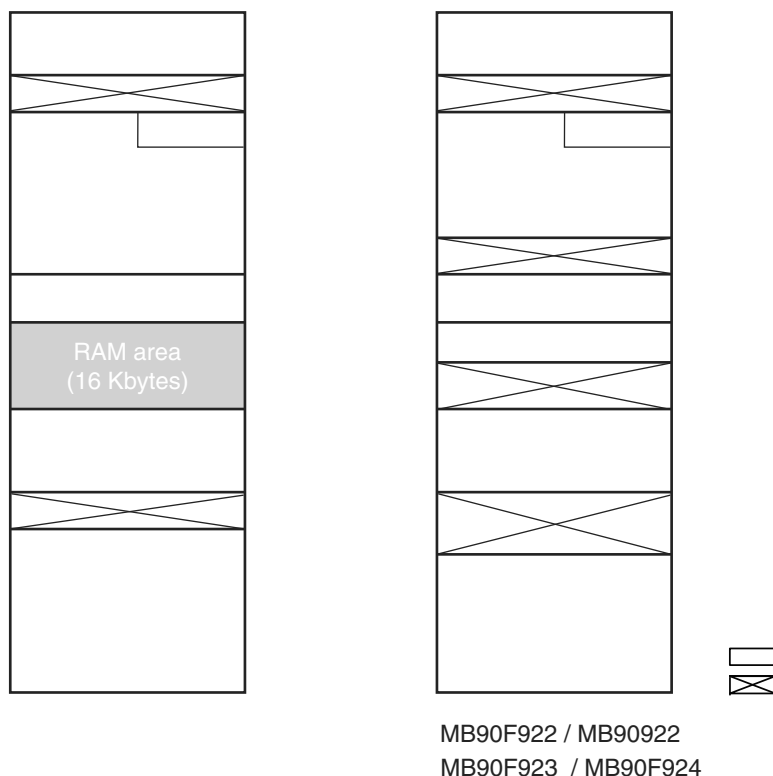
Sample external clock connection

■ BLOCK DIAGRAM



MB90920 Series

■ MEMORY MAP



Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000 _H	004000 _H	002900 _H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000 _H	004A00 _H	003700 _H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000 _H	006A00 _H	003700 _H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000_H, the actual address to be accessed is FFC000_H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000_H to FFFFFFF_H appears in the image from 008000_H to 00FFFF_H, it is recommended that ROM data tables be stored in the area from FF8000_H to FFFFFFF_H.

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H , 00000B _H	(Disabled)				
00000C _H	Port C data register	PDRC	R/W	Port C	XXXXXXXX _B
00000D _H	Port D data register	PDRD	R/W	Port D	XXXXXXXX _B
00000E _H	Port E data register	PDRE	R/W	Port E	XXXXXXXX _B
00000F _H	(Disabled)				
000010 _H	Port 0 direction register	DDR0	R/W	Port 0	00000000 _B
000011 _H	Port 1 direction register	DDR1	R/W	Port 1	XX000000 _B
000012 _H	Port 2 direction register	DDR2	R/W	Port 2	000000XX _B
000013 _H	Port 3 direction register	DDR3	R/W	Port 3	00000000 _B
000014 _H	Port 4 direction register	DDR4	R/W	Port 4	00000000 _B
000015 _H	Port 5 direction register	DDR5	R/W	Port 5	00000000 _B
000016 _H	Port 6 direction register	DDR6	R/W	Port 6	00000000 _B
000017 _H	Port 7 direction register	DDR7	R/W	Port 7	00000000 _B
000018 _H	Port 8 direction register	DDR8	R/W	Port 8	00000000 _B
000019 _H	Port 9 direction register	DDR9	R/W	Port 9	X0000000 _B
00001A _H	Analog input enable	ADER6	R/W	Port 6, A/D	11111111 _B
00001B _H	(Disabled)				
00001C _H	Port C direction register	DDRC	R/W	Port C	00000000 _B
00001D _H	Port D direction register	DDRD	R/W	Port D	X0000000 _B
00001E _H	Port E direction register	DDRE	R/W	Port E	XXXXX000 _B
00001F _H	(Disabled)				
000020 _H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0 _B
000021 _H	Higher A/D control status register	ADCS1	R/W		0000000X _B
000022 _H	Lower A/D control status register	ADCR0	R		00000000 _B
000023 _H	Higher A/D data register	ADCR1	R		XXXXXX00 _B

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List of Message Buffers (ID Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00 _H to 003A1F _H	003B00 _H to 003B1F _H	003700 _H to 00371F _H	003800 _H to 00381F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003B20 _H	003720 _H	003820 _H	ID register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
003A21 _H	003B21 _H	003721 _H	003821 _H				XXXXXX--- _B XXXXXXXX _B
003A22 _H	003B22 _H	003722 _H	003822 _H				
003A23 _H	003B23 _H	003723 _H	003823 _H				
003A24 _H	003B24 _H	003724 _H	003824 _H	ID register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
003A25 _H	003B25 _H	003725 _H	003825 _H				XXXXXX--- _B XXXXXXXX _B
003A26 _H	003B26 _H	003726 _H	003826 _H				
003A27 _H	003B27 _H	003727 _H	003827 _H				
003A28 _H	003B28 _H	003728 _H	003828 _H	ID register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
003A29 _H	003B29 _H	003729 _H	003829 _H				XXXXXX--- _B XXXXXXXX _B
003A2A _H	003B2A _H	00372A _H	00382A _H				
003A2B _H	003B2B _H	00372B _H	00382B _H				
003A2C _H	003B2C _H	00372C _H	00382C _H	ID register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
003A2D _H	003B2D _H	00372D _H	00382D _H				XXXXXX--- _B XXXXXXXX _B
003A2E _H	003B2E _H	00372E _H	00382E _H				
003A2F _H	003B2F _H	00372F _H	00382F _H				
003A30 _H	003B30 _H	003730 _H	003830 _H	ID register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
003A31 _H	003B31 _H	003731 _H	003831 _H				XXXXXX--- _B XXXXXXXX _B
003A32 _H	003B32 _H	003732 _H	003832 _H				
003A33 _H	003B33 _H	003733 _H	003833 _H				
003A34 _H	003B34 _H	003734 _H	003834 _H	ID register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
003A35 _H	003B35 _H	003735 _H	003835 _H				XXXXXX--- _B XXXXXXXX _B
003A36 _H	003B36 _H	003736 _H	003836 _H				
003A37 _H	003B37 _H	003737 _H	003837 _H				
003A38 _H	003B38 _H	003738 _H	003838 _H	ID register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
003A39 _H	003B39 _H	003739 _H	003839 _H				XXXXXX--- _B XXXXXXXX _B
003A3A _H	003B3A _H	00373A _H	00383A _H				
003A3B _H	003B3B _H	00373B _H	00383B _H				
003A3C _H	003B3C _H	00373C _H	00383C _H	ID register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
003A3D _H	003B3D _H	00373D _H	00383D _H				XXXXXX--- _B XXXXXXXX _B
003A3E _H	003B3E _H	00373E _H	00383E _H				
003A3F _H	003B3F _H	00373F _H	00383F _H				

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MB90920 Series

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Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40 _H	003B40 _H	003740 _H	003840 _H	ID register 8	IDR8	R/W	XXXXXXXX _B XXXXXXXX _B
003A41 _H	003B41 _H	003741 _H	003841 _H				XXXXXX--- _B XXXXXXXX _B
003A42 _H	003B42 _H	003742 _H	003842 _H				
003A43 _H	003B43 _H	003743 _H	003843 _H				
003A44 _H	003B44 _H	003744 _H	003844 _H	ID register 9	IDR9	R/W	XXXXXXXX _B XXXXXXXX _B
003A45 _H	003B45 _H	003745 _H	003845 _H				XXXXXX--- _B XXXXXXXX _B
003A46 _H	003B46 _H	003746 _H	003846 _H				
003A47 _H	003B47 _H	003747 _H	003847 _H				
003A48 _H	003B48 _H	003748 _H	003848 _H	ID register 10	IDR10	R/W	XXXXXXXX _B XXXXXXXX _B
003A49 _H	003B49 _H	003749 _H	003849 _H				XXXXXX--- _B XXXXXXXX _B
003A4A _H	003B4A _H	00374A _H	00384A _H				
003A4B _H	003B4B _H	00374B _H	00384B _H				
003A4C _H	003B4C _H	00374C _H	00384C _H	ID register 11	IDR11	R/W	XXXXXXXX _B XXXXXXXX _B
003A4D _H	003B4D _H	00374D _H	00384D _H				XXXXXX--- _B XXXXXXXX _B
003A4E _H	003B4E _H	00374E _H	00384E _H				
003A4F _H	003B4F _H	00374F _H	00384F _H				
003A50 _H	003B50 _H	003750 _H	003850 _H	ID register 12	IDR12	R/W	XXXXXXXX _B XXXXXXXX _B
003A51 _H	003B51 _H	003751 _H	003851 _H				XXXXXX--- _B XXXXXXXX _B
003A52 _H	003B52 _H	003752 _H	003852 _H				
003A53 _H	003B53 _H	003753 _H	003853 _H				
003A54 _H	003B54 _H	003754 _H	003854 _H	ID register 13	IDR13	R/W	XXXXXXXX _B XXXXXXXX _B
003A55 _H	003B55 _H	003755 _H	003855 _H				XXXXXX--- _B XXXXXXXX _B
003A56 _H	003B56 _H	003756 _H	003856 _H				
003A57 _H	003B57 _H	003757 _H	003857 _H				
003A58 _H	003B58 _H	003758 _H	003858 _H	ID register 14	IDR14	R/W	XXXXXXXX _B XXXXXXXX _B
003A59 _H	003B59 _H	003759 _H	003859 _H				XXXXXX--- _B XXXXXXXX _B
003A5A _H	003B5A _H	00375A _H	00385A _H				
003A5B _H	003B5B _H	00375B _H	00385B _H				
003A5C _H	003B5C _H	00375C _H	00385C _H	ID register 15	IDR15	R/W	XXXXXXXX _B XXXXXXXX _B
003A5D _H	003B5D _H	00375D _H	00385D _H				XXXXXX--- _B XXXXXXXX _B
003A5E _H	003B5E _H	00375E _H	00385E _H				
003A5F _H	003B5F _H	00375F _H	00385F _H				

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(Continued)

Interrupt source	EI ² OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
UART 1 RX	◎	#37	25 _H	FFFF68 _H	ICR13	0000BD _H *1	High ↑
UART 1 TX	△	#38	26 _H	FFFF64 _H			
UART 0 RX	◎	#39	27 _H	FFFF60 _H	ICR14	0000BE _H *1	↓ Low
UART 0 TX	△	#40	28 _H	FFFF5C _H			
Flash memory status	×	#41	29 _H	FFFF58 _H	ICR15	0000BF _H *1	
Delay interrupt generator module	×	#42	2A _H	FFFF54 _H			

◎ : Usable, and has expanded intelligent I/O services (EI²OS) stop function

○ : Usable

△ : Usable when interrupt sources sharing ICR are not in use

×

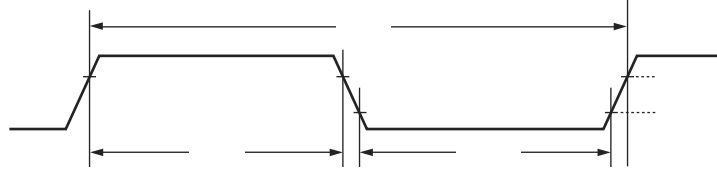
*1 : • Peripheral functions that share the ICR register have the same interrupt level.

• If the expanded intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.

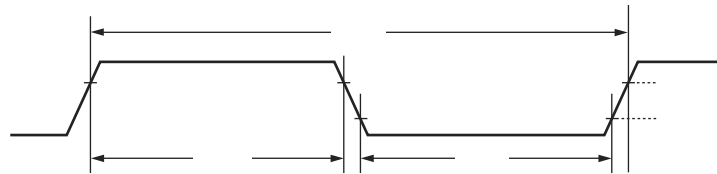
• When the expanded intelligent I/O service (EI²OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2 : Priority applies when interrupts of the same level are generated.

- X0, X1 clock timing



- X0A, X1A clock timing



• Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1

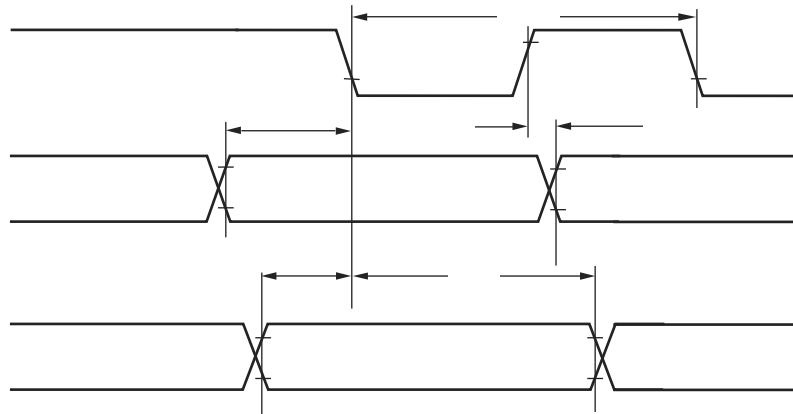
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t _{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXI}			0	—	ns
SOT → SCK ↓ delay time	t _{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t _{CP} – 70	—	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.

• C_L is the load capacitance connected to the pin during testing.

• t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.



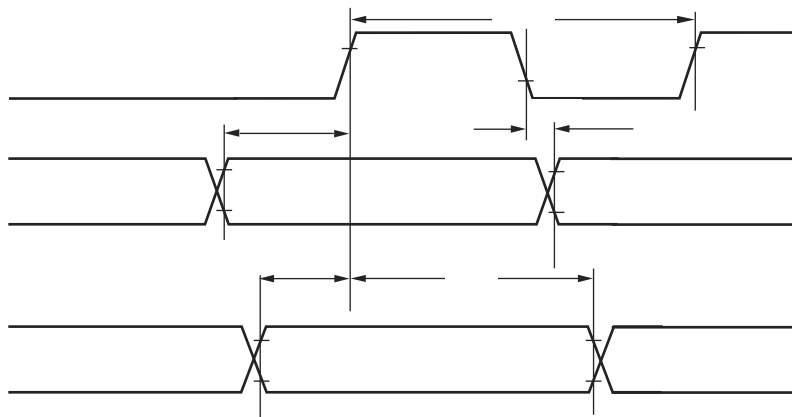
MB90920 Series

- Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t _{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t _{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t _{CP} – 70	—	ns

- Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
 - C_L is the load capacitance connected to the pin during testing.
 - t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.



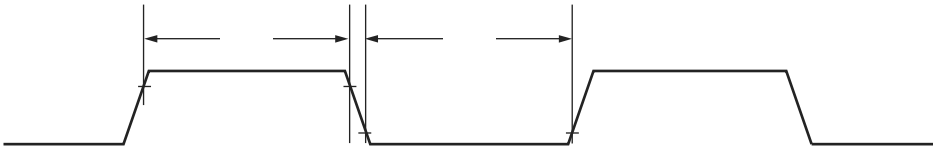
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t _{TIWH} t _{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t _{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Timer input timing



MB90920 Series

5. A/D Converter

(1) Electrical Characteristics

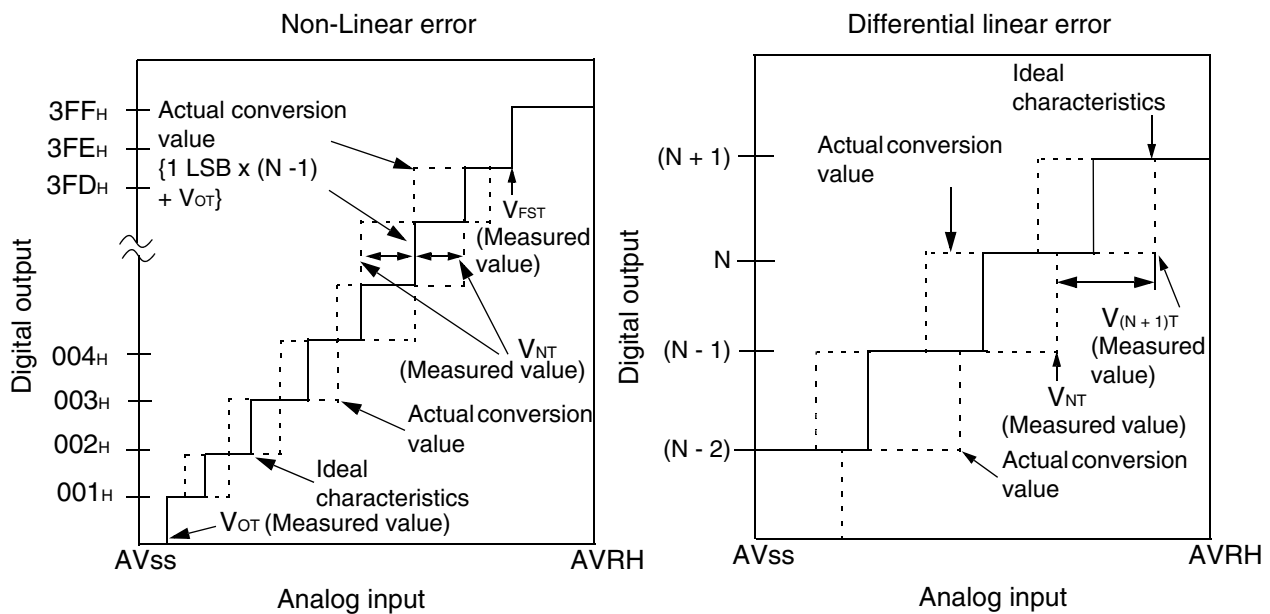
($V_{CC} = AV_{CC} = AVRH = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	− 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{SS} - 1.5\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 2.5\text{ LSB}$	V	1 LSB = ($AVRH - AV_{SS}$) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 3.5\text{ LSB}$	$AVRH - 1.5\text{ LSB}$	$AVRH + 0.5\text{ LSB}$	V	
Sampling time	t_{SMP}	—	0.4	—	16500	μs	4.5 V $\leq$ $AV_{CC} \leq$ 5.5 V
			1.0				4.0 V $\leq$ $AV_{CC} \leq$ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	μs	4.5 V $\leq$ $AV_{CC} \leq$ 5.5 V
			2.2				4.0 V $\leq$ $AV_{CC} \leq$ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	μs	*1
Analog port input current	I_{AIN}	AN0 to AN7	− 0.3	—	+ 10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	$AVRH$	V	
Reference voltage	$AV+$	$AVRH$	$AV_{SS} + 2.7$	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	μA	*2
Reference voltage supply current	I_R	$AVRH$	—	520	900	μA	$V_{AVRH} = 5.0\text{ V}$
	I_{RH}		—	—	5	μA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : The time per channel (4.5 V $\leq$ $AV_{CC} \leq$ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when $V_{CC} = AV_{CC} = AVRH = 5.0\text{ V}$) with A/D converter not operating, and CPU in stop mode.

(Continued)



$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage when digital output changes from 000_H to 001_H

V_{FST} : Voltage when digital output changes from 3FE_H to 3FF_H