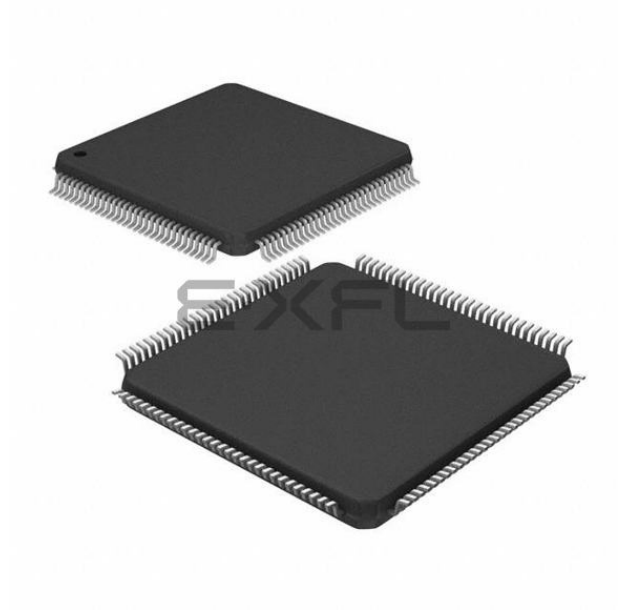
# Infineon Technologies - MB90922NCSPMC-GS-149E1 Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 93 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-149e1 |

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

*16-bit Microcontroller*

**CMOS**

# F²MC-16LX MB90920 Series

## MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

## ■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

## ■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

*(Continued)*

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/


2010.9

*(Continued)*

- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : $f_{CP}$, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at $f_{CP}$ = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at $f_{CP}$ = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

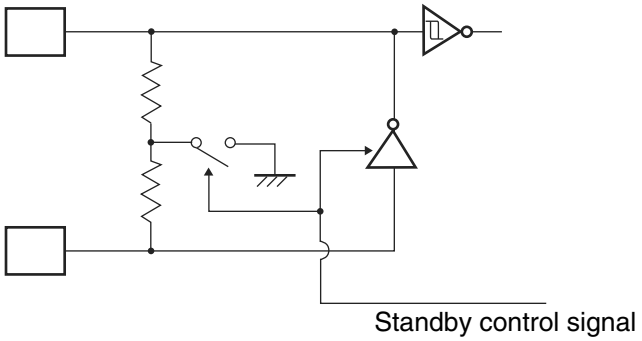
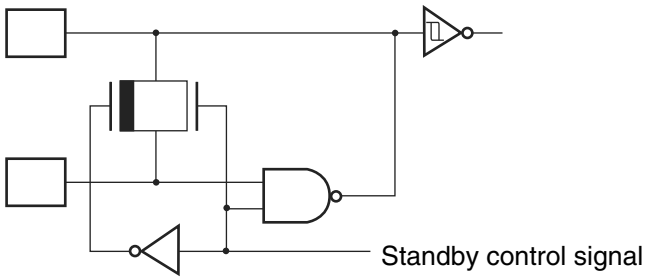
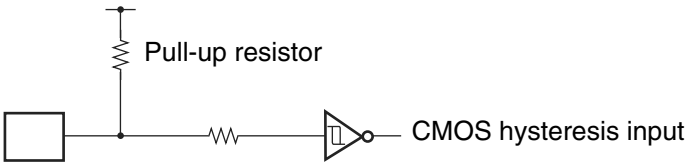
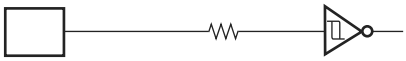
## ■ PRODUCT LINEUP

| Part number / Parameter | MB90 F922NC | MB90 F922NCS | MB90 F923NC | MB90 F923NCS | MB90 F924NC | MB90 F924NCS | MB90 922NCS | MB90 V920-101 | MB90 V920-102 |
|---|---|---|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | | MASK ROM product | Evaluation product | |
| CPU | $F^2MC$-16LX CPU | | | | | | | | |
| System clock | PLL clock multiplier circuit ( × 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped)<br>Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8) | | | | | | | | |
| Sub clock pins (X0A, X1A) | Yes | No | Yes | No | Yes | No | No | No | Yes |
| ROM | Flash memory 256 Kbytes | | Flash memory 384 Kbytes | | Flash memory 512 Kbytes | | 256 K bytes | External | |
| RAM | 10 Kbytes | | 16 Kbytes | | 24 Kbytes | | 10 K bytes | 30 Kbytes | |
| I/O port | 91 ports | 93 ports | 91 ports | 93 ports | 91 ports | 93 ports | 93 ports | 93 ports | 91 ports |
| LCD controller | 32 segment × 4 common | | | | | | | | |
| LIN-UART | UART (LIN/SCI) 4 channels | | | | | | | | |
| CAN interface | 4 channels | | | | | | | | |
| 16-bit input capture | 8 channels | | | | | | | | |
| 16-bit reload timer | 4 channels | | | | | | | | |
| 16-bit free-run timer | 1 channel | | | | | | | | |
| Real time watch timer | 1 channel | | | | | | | | |
| 16-bit PPG timer | 6 channels | | | | | | | | |
| External interrupt | 8 channels | | | | | | | | |
| 8/10-bit A/D converter | 8 channels | | | | | | | | |
| Low-voltage/ CPU operating detection reset | Yes | | | | | | | No | |
| Stepping motor controller | 4 channels | | | | | | | | |
| Sound generator | 2 channels | | | | | | | | |
| Flash memory security | Yes | | | | | | — | | |
| Operating voltage | 4.0 V to 5.5 V | | | | | | | 4.5 V to 5.5 V | |
| Package | LQFP-120 | | | | | | | PGA-299 | |

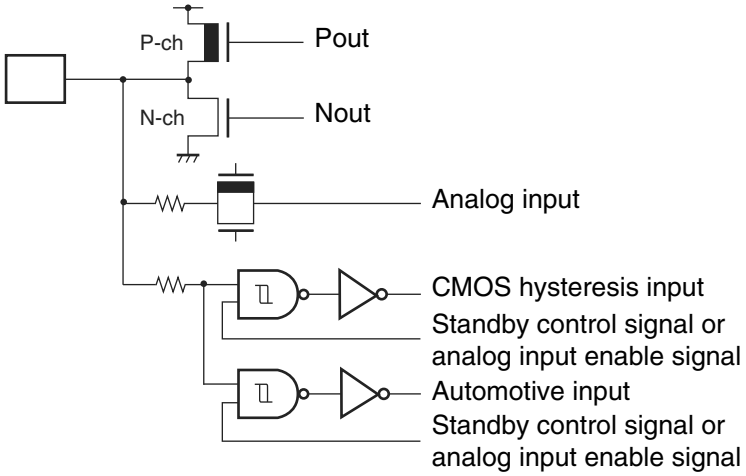
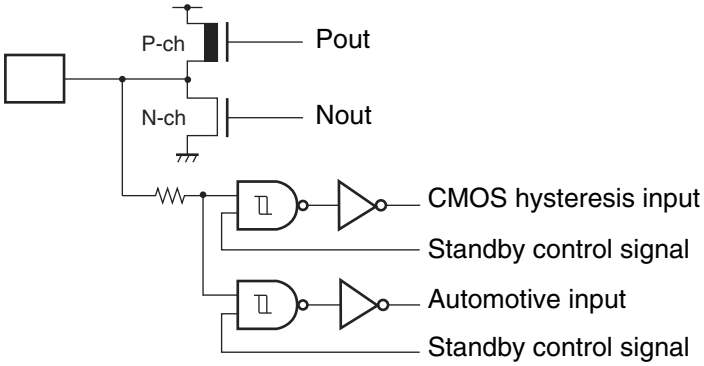
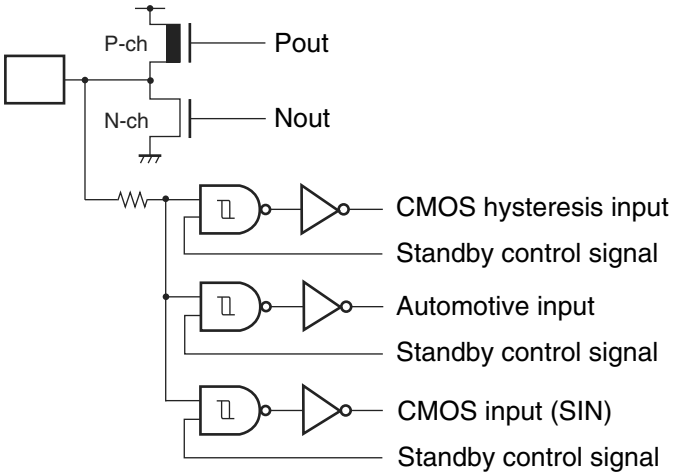
| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 104 | P13 | I | General-purpose I/O port |
| | PPG5 | | 16-bit PPG ch.5 output pin |
| 109 | P14 | I | General-purpose I/O port |
| | TIN2 | | 16-bit reload timer ch.2 TIN input pin |
| | IN1 | | Input capture ch.1 trigger input pin |
| 110 | P15 | I | General-purpose I/O port |
| | IN0 | | Input capture ch.0 trigger input pin |
| 111 | COM0 | P | LCD controller/driver common output pin |
| 112 | COM1 | P | LCD controller/driver common output pin |
| 113 | COM2 | P | LCD controller/driver common output pin |
| 114 | COM3 | P | LCD controller/driver common output pin |
| 115 | P22 | F | General-purpose I/O port |
| | SEG00 | | LCD controller/driver segment output pin |
| 116 | P23 | F | General-purpose I/O port |
| | SEG01 | | LCD controller/driver segment output pin |
| 117 | P24 | F | General-purpose I/O port |
| | SEG02 | | LCD controller/driver segment output pin |
| 118 | P25 | F | General-purpose I/O port |
| | SEG03 | | LCD controller/driver segment output pin |
| 119 | P26 | F | General-purpose I/O port |
| | SEG04 | | LCD controller/driver segment output pin |
| 120 | P27 | F | General-purpose I/O port |
| | SEG05 | | LCD controller/driver segment output pin |
| 1 | P30 | F | General-purpose I/O port |
| | SEG06 | | LCD controller/driver segment output pin |
| 2 | P31 | F | General-purpose I/O port |
| | SEG07 | | LCD controller/driver segment output pin |
| 3 | P32 | F | General-purpose I/O port |
| | SEG08 | | LCD controller/driver segment output pin |
| 4 | P33 | F | General-purpose I/O port |
| | SEG09 | | LCD controller/driver segment output pin |
| 5 | P34 | F | General-purpose I/O port |
| | SEG10 | | LCD controller/driver segment output pin |
| 6 | P35 | F | General-purpose I/O port |
| | SEG11 | | LCD controller/driver segment output pin |

*(Continued)*

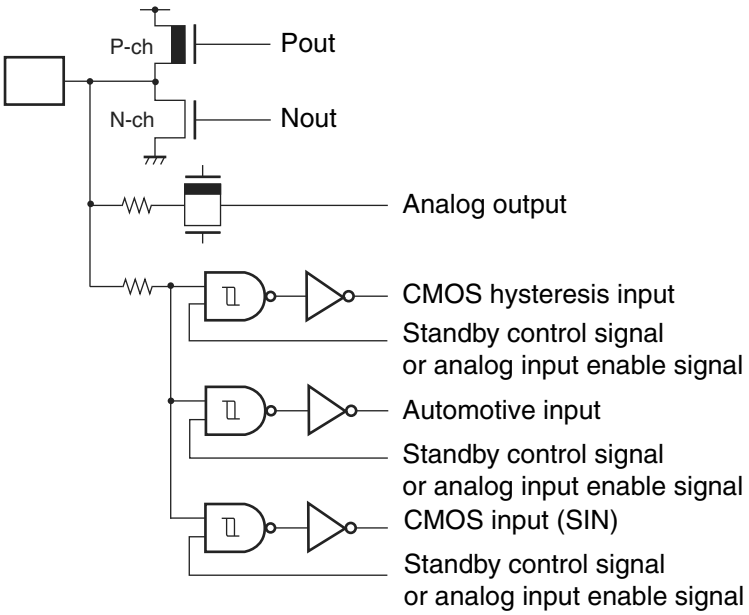
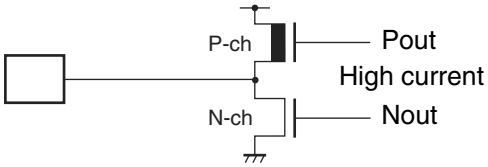
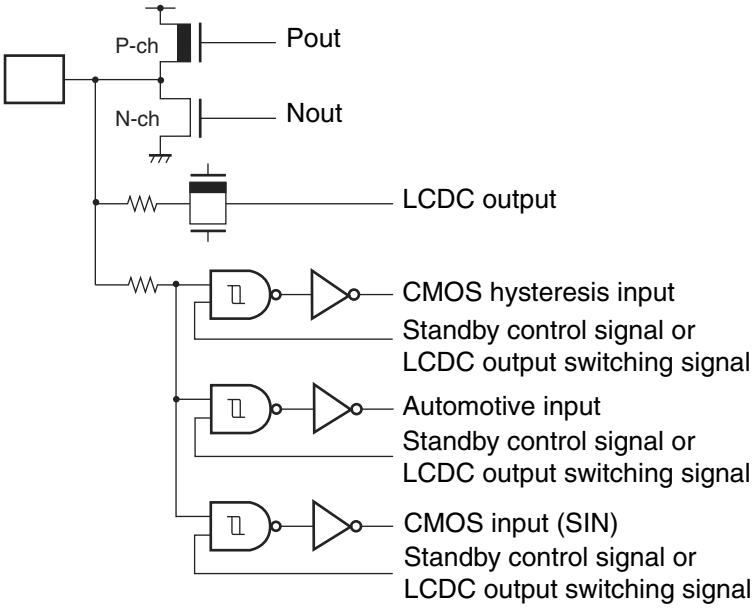
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>High-speed oscillation feedback resistance :<br>approx. 1 MΩ<br>(Flash memory product/MASK ROM product/Evaluation product) |
| B |  | Oscillation circuit<br>Low-speed oscillation feedback resistance : approx. 10 MΩ |
| C |  | Input-only pin (with pull-up resistance)<br>• Attached pull-up resistor : approx. 50 kΩ<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$) |
| D |  | Input-only pin<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>Note: The MD2 pin of the Flash memory products uses this circuit type. |

*(Continued)*

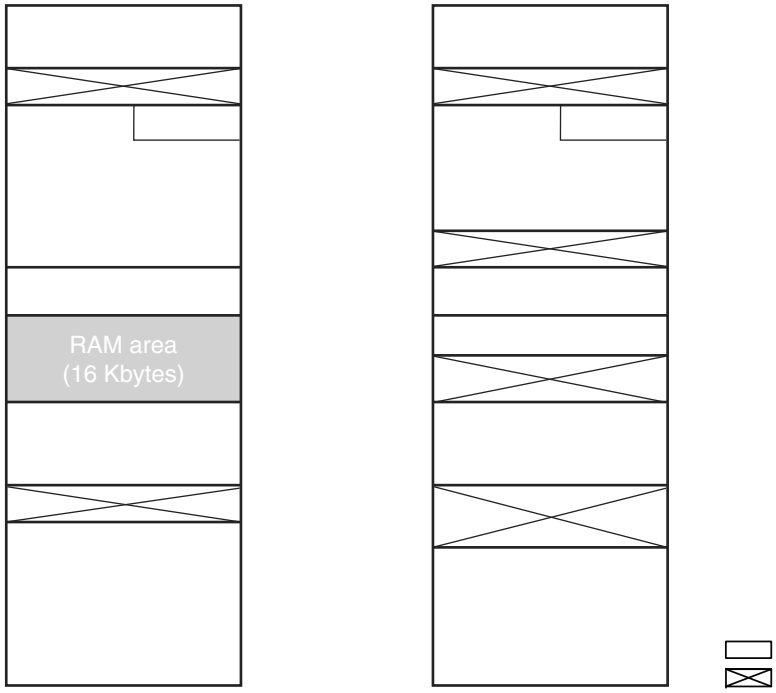
| Type | Circuit | Remarks |
|---|---|---|
| H |  | A/D converter input common general-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| I |  | General-purpose port<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| J |  | General-purpose port (serial input)<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| K |  | A/D converter input common general-purpose port (serial input)<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| L |  | High current output port (SMC pin)<br>CMOS output ($I_{OH}/I_{OL}$ = ± 30 mA) |
| M |  | LCDC output common general-purpose port (serial input) )<br>• CMOS output ($I_{OH}/I_{OL}$ = ± 4 mA)<br>• CMOS hysteresis input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.2 $V_{CC}$)<br>• CMOS input (SIN) ($V_{IH}/V_{IL}$ = 0.7 $V_{CC}$/0.3 $V_{CC}$)<br>• Automotive input ($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |

*(Continued)*

## ■ MEMORY MAP




MB90F922 / MB90922
MB90F923 / MB90F924

| Parts No. | ROM (Flash) capacitance | RAM capacitance | Address #1 | Address #2 | Address #3 |
|---|---|---|---|---|---|
| MB90F922NC/F922NCS/922NCS | 256 Kbytes | 10 Kbytes | FC0000H | 004000H | 002900H |
| MB90F923NC/F923NCS | 384 Kbytes | 16 Kbytes | FA0000H | 004A00H | 003700H |
| MB90F924NC/F924NCS | 512 Kbytes | 24 Kbytes | F80000H | 006A00H | 003700H |

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

## ■ I/O MAP

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000000H | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXXB |
| 000001H | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXXB |
| 000002H | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXXB |
| 000003H | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXXB |
| 000004H | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXXB |
| 000005H | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXXB |
| 000006H | Port 6 data register | PDR6 | R/W | Port 6 | XXXXXXXXB |
| 000007H | Port 7 data register | PDR7 | R/W | Port 7 | XXXXXXXXB |
| 000008H | Port 8 data register | PDR8 | R/W | Port 8 | XXXXXXXXB |
| 000009H | Port 9 data register | PDR9 | R/W | Port 9 | XXXXXXXXB |
| 00000AH, 00000BH | (Disabled) | | | | |
| 00000CH | Port C data register | PDRC | R/W | Port C | XXXXXXXXB |
| 00000DH | Port D data register | PDRD | R/W | Port D | XXXXXXXXB |
| 00000EH | Port E data register | PDRE | R/W | Port E | XXXXXXXXB |
| 00000FH | (Disabled) | | | | |
| 000010H | Port 0 direction register | DDR0 | R/W | Port 0 | 00000000B |
| 000011H | Port 1 direction register | DDR1 | R/W | Port 1 | XX000000B |
| 000012H | Port 2 direction register | DDR2 | R/W | Port 2 | 000000XXB |
| 000013H | Port 3 direction register | DDR3 | R/W | Port 3 | 00000000B |
| 000014H | Port 4 direction register | DDR4 | R/W | Port 4 | 00000000B |
| 000015H | Port 5 direction register | DDR5 | R/W | Port 5 | 00000000B |
| 000016H | Port 6 direction register | DDR6 | R/W | Port 6 | 00000000B |
| 000017H | Port 7 direction register | DDR7 | R/W | Port 7 | 00000000B |
| 000018H | Port 8 direction register | DDR8 | R/W | Port 8 | 00000000B |
| 000019H | Port 9 direction register | DDR9 | R/W | Port 9 | X0000000B |
| 00001AH | Analog input enable | ADER6 | R/W | Port 6, A/D | 11111111B |
| 00001BH | (Disabled) | | | | |
| 00001CH | Port C direction register | DDRC | R/W | Port C | 00000000B |
| 00001DH | Port D direction register | DDRD | R/W | Port D | X0000000B |
| 00001EH | Port E direction register | DDRE | R/W | Port E | XXXXX000B |
| 00001FH | (Disabled) | | | | |
| 000020H | Lower A/D control status register | ADCS0 | R/W | A/D converter | 000XXXX0B |
| 000021H | Higher A/D control status register | ADCS1 | R/W | | 0000000XB |
| 000022H | Lower A/D control status register | ADCR0 | R | | 00000000B |
| 000023H | Higher A/D data register | ADCR1 | R | | XXXXXX00B |

*(Continued)*

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000B0H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111B |
| 0000B1H | Interrupt control register 01 | ICR01 | R/W | | 00000111B |
| 0000B2H | Interrupt control register 02 | ICR02 | R/W | | 00000111B |
| 0000B3H | Interrupt control register 03 | ICR03 | R/W | | 00000111B |
| 0000B4H | Interrupt control register 04 | ICR04 | R/W | | 00000111B |
| 0000B5H | Interrupt control register 05 | ICR05 | R/W | | 00000111B |
| 0000B6H | Interrupt control register 06 | ICR06 | R/W | | 00000111B |
| 0000B7H | Interrupt control register 07 | ICR07 | R/W | | 00000111B |
| 0000B8H | Interrupt control register 08 | ICR08 | R/W | | 00000111B |
| 0000B9H | Interrupt control register 09 | ICR09 | R/W | | 00000111B |
| 0000BAH | Interrupt control register 10 | ICR10 | R/W | | 00000111B |
| 0000BBH | Interrupt control register 11 | ICR11 | R/W | | 00000111B |
| 0000BCH | Interrupt control register 12 | ICR12 | R/W | | 00000111B |
| 0000BDH | Interrupt control register 13 | ICR13 | R/W | | 00000111B |
| 0000BEH | Interrupt control register 14 | ICR14 | R/W | | 00000111B |
| 0000BFH | Interrupt control register 15 | ICR15 | R/W | | 00000111B |
| 0000C0H to 0000C3H | (Disabled) | | | | |
| 0000C4H | Serial mode register 1 | SMR1 | R/W, W | UART (LIN/SCI) 1 | 00000000B |
| 0000C5H | Serial control register 1 | SCR1 | R/W, W | | 00000000B |
| 0000C6H | Reception/transmission data register 1 | RDR1/ TDR1 | R/W | | 00000000B |
| 0000C7H | Serial status register 1 | SSR1 | R/W, R | | 00001000B |
| 0000C8H | Extended communication control register 1 | ECCR1 | R/W, R | | 000000XXB |
| 0000C9H | Extended status control register 1 | ESCR1 | R/W | | 00000100B |
| 0000CAH | Baud rate generator register 10 | BGR10 | R/W | | 00000000B |
| 0000CBH | Baud rate generator register 11 | BGR11 | R/W, R | | 00000000B |
| 0000CCH | Lower watch timer control register | WTCRL | R/W | Real-time watch timer | 000XXXX0B |
| 0000CDH | Middle watch timer control register | WTCRM | R/W | | 00000000B |
| 0000CEH | Higher watch timer control register | WTCRH | R/W | | XXXXXX00B |
| 0000CFH | Sub clock control register | PSCCR | W | Sub clock | XXXX0000B |
| 0000D0H | Input capture control status 4/5 | ICS45 | R/W | Input capture 4/5 | 00000000B |
| 0000D1H | Input capture edge register 4/5 | ICE45 | R/W, R | | XXXXXXXXB |
| 0000D2H | Input capture control status 6/7 | ICS67 | R/W | Input capture 6/7 | 00000000B |
| 0000D3H | Input capture edge register 6/7 | ICE67 | R/W, R | | XXX0X0XXB |

*(Continued)*

**List of Control Registers(2)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 000040H | 000070H | 0039C0H | 0039D0H | Message buffer valid register | BVALR | R/W | 00000000B |
| 000041H | 000071H | 0039C1H | 0039D1H | | | | 00000000B |
| 000042H | 000072H | 0039C2H | 0039D2H | Transmit request register | TREQR | R/W | 00000000B |
| 000043H | 000073H | 0039C3H | 0039D3H | | | | 00000000B |
| 000044H | 000074H | 0039C4H | 0039D4H | Transmit cancel register | TCANR | W | 00000000B |
| 000045H | 000075H | 0039C5H | 0039D5H | | | | 00000000B |
| 000046H | 000076H | 0039C6H | 0039D6H | Transmit complete register | TCR | R/W | 00000000B |
| 000047H | 000077H | 0039C7H | 0039D7H | | | | 00000000B |
| 000048H | 000078H | 0039C8H | 0039D8H | Receive complete register | RCR | R/W | 00000000B |
| 000049H | 000079H | 0039C9H | 0039D9H | | | | 00000000B |
| 00004AH | 00007AH | 0039CAH | 0039DAH | Remote request receive register | RRTRR | R/W | 00000000B |
| 00004BH | 00007BH | 0039CBH | 0039DBH | | | | 00000000B |
| 00004CH | 00007CH | 0039CCH | 0039DCH | Receive overrun register | ROVRR | R/W | 00000000B |
| 00004DH | 00007DH | 0039CDH | 0039DDH | | | | 00000000B |
| 00004EH | 00007EH | 0039CEH | 0039DEH | Receive interrupt enable register | RIER | R/W | 00000000B |
| 00004FH | 00007FH | 0039CFH | 0039DFH | | | | 00000000B |
| 003C08H | 003D08H | 003E08H | 003F08H | IDE register | IDER | R/W | XXXXXXXXB |
| 003C09H | 003D09H | 003E09H | 003F09H | | | | XXXXXXXXB |
| 003C0AH | 003D0AH | 003E0AH | 003F0AH | Transmit RTR register | TRTRR | R/W | 00000000B |
| 003C0BH | 003D0BH | 003E0BH | 003F0BH | | | | 00000000B |
| 003C0CH | 003D0CH | 003E0CH | 003F0CH | Remote frame receive wait register | RFWTR | R/W | XXXXXXXXB |
| 003C0DH | 003D0DH | 003E0DH | 003F0DH | | | | XXXXXXXXB |
| 003C0EH | 003D0EH | 003E0EH | 003F0EH | Transmit interrupt enable register | TIER | R/W | 00000000B |
| 003C0FH | 003D0FH | 003E0FH | 003F0FH | | | | 00000000B |
| 003C10H | 003D10H | 003E10H | 003F10H | Acceptance mask select register | AMSR | R/W | XXXXXXXXB |
| 003C11H | 003D11H | 003E11H | 003F11H | | | | XXXXXXXXB |
| 003C12H | 003D12H | 003E12H | 003F12H | | | | XXXXXXXXB |
| 003C13H | 003D13H | 003E13H | 003F13H | | | | XXXXXXXXB |
| 003C14H | 003D14H | 003E14H | 003F14H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXXB |
| 003C15H | 003D15H | 003E15H | 003F15H | | | | XXXXXXXXB |
| 003C16H | 003D16H | 003E16H | 003F16H | | | | XXXXX---B |
| 003C17H | 003D17H | 003E17H | 003F17H | | | | XXXXXXXXB |
| 003C18H | 003D18H | 003E18H | 003F18H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXXB |
| 003C19H | 003D19H | 003E19H | 003F19H | | | | XXXXXXXXB |
| 003C1AH | 003D1AH | 003E1AH | 003F1AH | | | | XXXXX---B |
| 003C1BH | 003D1BH | 003E1BH | 003F1BH | | | | XXXXXXXXB |

**List of Message Buffers (ID Registers)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A00H to 003A1FH | 003B00H to 003B1FH | 003700H to 00371FH | 003800H to 00381FH | General-purpose RAM | — | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A20H | 003B20H | 003720H | 003820H | ID register 0 | IDR0 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A21H | 003B21H | 003721H | 003821H | | | | |
| 003A22H | 003B22H | 003722H | 003822H | | | | XXXXX---B XXXXXXXXB |
| 003A23H | 003B23H | 003723H | 003823H | | | | |
| 003A24H | 003B24H | 003724H | 003824H | ID register 1 | IDR1 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A25H | 003B25H | 003725H | 003825H | | | | |
| 003A26H | 003B26H | 003726H | 003826H | | | | XXXXX---B XXXXXXXXB |
| 003A27H | 003B27H | 003727H | 003827H | | | | |
| 003A28H | 003B28H | 003728H | 003828H | ID register 2 | IDR2 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A29H | 003B29H | 003729H | 003829H | | | | |
| 003A2AH | 003B2AH | 00372AH | 00382AH | | | | XXXXX---B XXXXXXXXB |
| 003A2BH | 003B2BH | 00372BH | 00382BH | | | | |
| 003A2CH | 003B2CH | 00372CH | 00382CH | ID register 3 | IDR3 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A2DH | 003B2DH | 00372DH | 00382DH | | | | |
| 003A2EH | 003B2EH | 00372EH | 00382EH | | | | XXXXX---B XXXXXXXXB |
| 003A2FH | 003B2FH | 00372FH | 00382FH | | | | |
| 003A30H | 003B30H | 003730H | 003830H | ID register 4 | IDR4 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A31H | 003B31H | 003731H | 003831H | | | | |
| 003A32H | 003B32H | 003732H | 003832H | | | | XXXXX---B XXXXXXXXB |
| 003A33H | 003B33H | 003733H | 003833H | | | | |
| 003A34H | 003B34H | 003734H | 003834H | ID register 5 | IDR5 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A35H | 003B35H | 003735H | 003835H | | | | |
| 003A36H | 003B36H | 003736H | 003836H | | | | XXXXX---B XXXXXXXXB |
| 003A37H | 003B37H | 003737H | 003837H | | | | |
| 003A38H | 003B38H | 003738H | 003838H | ID register 6 | IDR6 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A39H | 003B39H | 003739H | 003839H | | | | |
| 003A3AH | 003B3AH | 00373AH | 00383AH | | | | XXXXX---B XXXXXXXXB |
| 003A3BH | 003B3BH | 00373BH | 00383BH | | | | |
| 003A3CH | 003B3CH | 00373CH | 00383CH | ID register 7 | IDR7 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A3DH | 003B3DH | 00373DH | 00383DH | | | | |
| 003A3EH | 003B3EH | 00373EH | 00383EH | | | | XXXXX---B XXXXXXXXB |
| 003A3FH | 003B3FH | 00373FH | 00383FH | | | | |

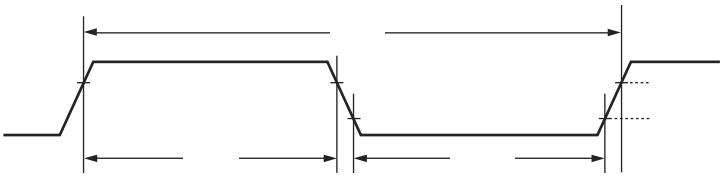
*(Continued)*

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

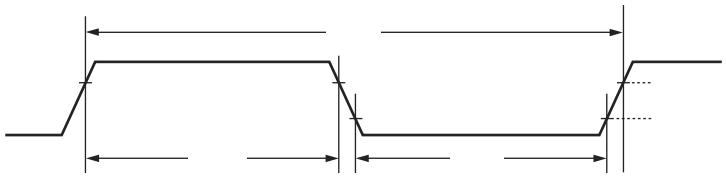
| Interrupt source | EI²OS corresponding | Interrupt vector | | | Interrupt control register | | Priority *2 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| Reset | × | #08 | 08H | FFFFDCH | — | — | High |
| INT9 instruction | × | #09 | 09H | FFFFD8H | — | — | |
| Exception processing | × | #10 | 0AH | FFFFD4H | — | — | |
| CAN0 received/CAN2 received | × | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H*1 | |
| CAN0 transmitted/node status/ CAN2 transmitted/node status | × | #12 | 0CH | FFFFCCH | | | |
| CAN1 received/CAN3 received | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H*1 | |
| CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO | × | #14 | 0EH | FFFFC4H | | | |
| Input capture 0 | △ | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H*1 | |
| DTP/ external interrupt - ch.0/ch.1 detected | △ | #16 | 10H | FFFFBCH | | | |
| Reload timer 0 | △ | #17 | 11H | FFFFB8H | ICR03 | 0000B3H*1 | |
| Reload timer 2 | △ | #18 | 12H | FFFFB4H | | | |
| Input capture 1 | △ | #19 | 13H | FFFFB0H | ICR04 | 0000B4H*1 | |
| DTP/ external interrupt - ch.2/ch.3 detected | △ | #20 | 14H | FFFFACH | | | |
| Input capture 2 | △ | #21 | 15H | FFFFA8H | ICR05 | 0000B5H*1 | |
| Reload timer 3 | △ | #22 | 16H | FFFFA4H | | | |
| Input capture 3/4/5/6/7 | △ | #23 | 17H | FFFFA0H | ICR06 | 0000B6H*1 | |
| DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX | △ | #24 | 18H | FFFF9CH | | | |
| PPG timer 0 | △ | #25 | 19H | FFFF98H | ICR07 | 0000B7H*1 | |
| DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX | △ | #26 | 1AH | FFFF94H | | | |
| PPG timer 1 | △ | #27 | 1BH | FFFF90H | ICR08 | 0000B8H*1 | |
| Reload timer 1 | △ | #28 | 1CH | FFFF8CH | | | |
| PPG timer 2/3/4/5 | ○ | #29 | 1DH | FFFF88H | ICR09 | 0000B9H*1 | |
| Real time watch timer watch timer (sub clock) | × | #30 | 1EH | FFFF84H | | | |
| Free-run timer overflow/clear | × | #31 | 1FH | FFFF80H | ICR10 | 0000BAH *1 | |
| A/D converter conversion complete | ○ | #32 | 20H | FFFF7CH | | | |
| Sound generator 0/1 | × | #33 | 21H | FFFF78H | ICR11 | 0000BBH*1 | |
| Time-base timer | × | #34 | 22H | FFFF74H | | | |
| UART2 RX | ○ | #35 | 23H | FFFF70H | ICR12 | 0000BCH*1 | |
| UART2 TX | △ | #36 | 24H | FFFF6CH | | | Low |

*(Continued)*

• X0, X1 clock timing

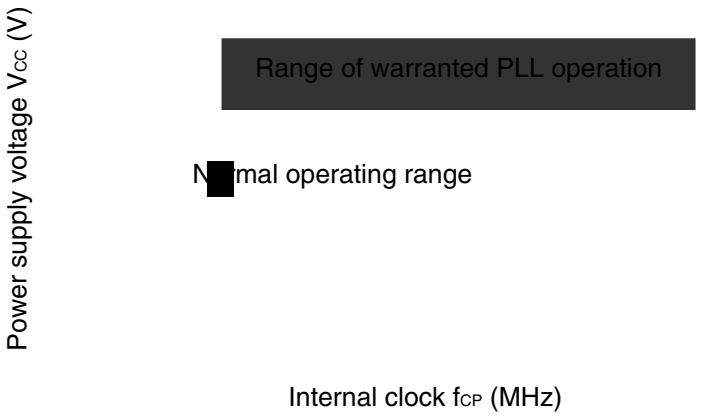


• X0A, X1A clock timing



• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage

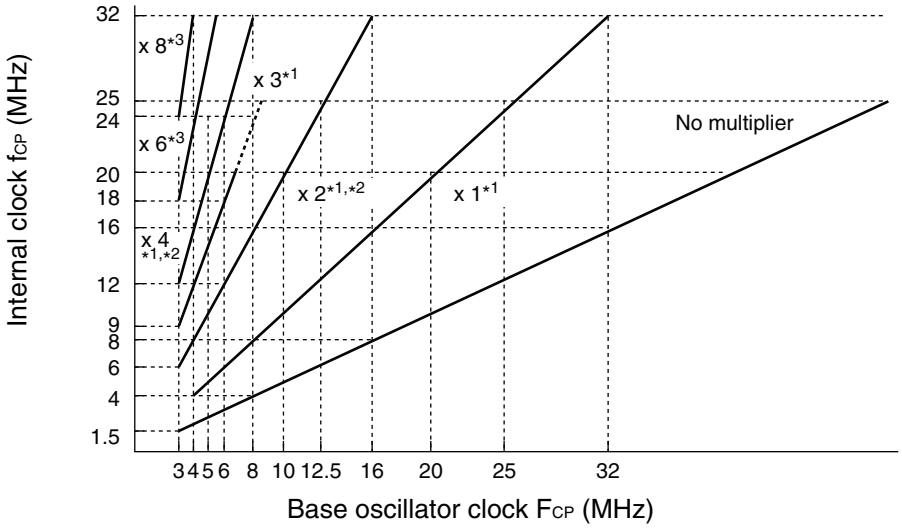



Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

*(Continued)*

*(Continued)*

Base oscillator frequency vs. Internal operating clock frequency




*1 : When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example] When using a base oscillator frequency of 24 MHz at PLL × 1 :
CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4,CS2 bit = "1"
[Example] When using a base oscillator frequency of 6 MHz at PLL × 3 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, the following settings are also supported.
PLL × 2 : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4 : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3 : When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example] When using a base oscillator frequency of 4 MHz at PLL × 6 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"
[Example] When using a base oscillator frequency of 3 MHz at PLL × 8 :
CKSCR register : CS1 bit = "1", CS0 bit = "1"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

**(2) Reset input**

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to +105 °C)

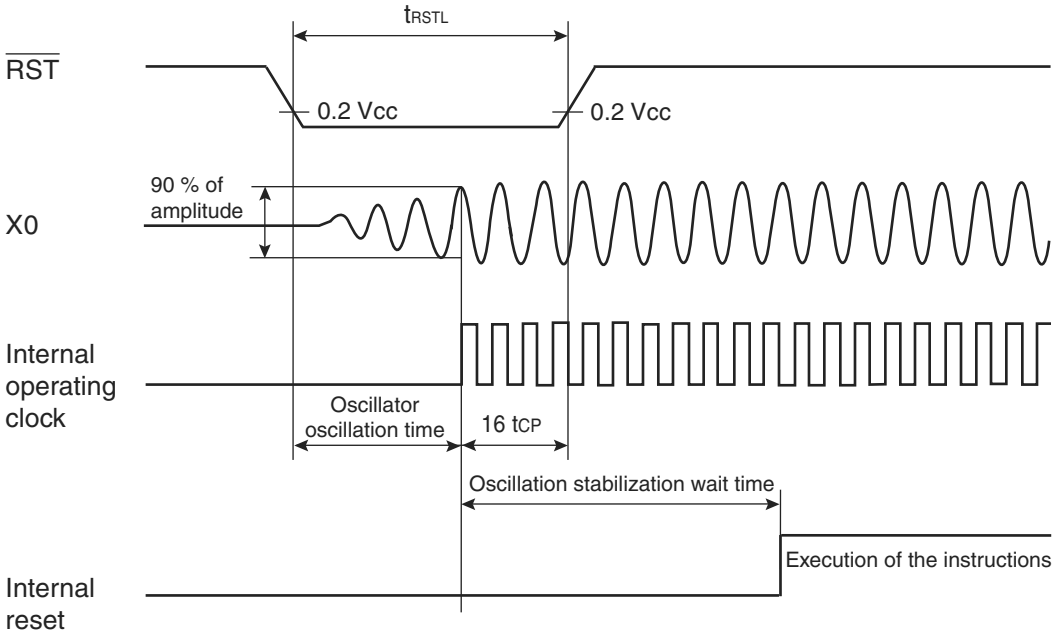
| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500 | — | ns | During normal operation |
| | | | Oscillator oscillation time* + 16 $t_{CP}$ | — | ms | In stop mode, sub clock mode, sub sleep mode, and watch mode |
| | | | 100 | — | µs | In time-base timer mode |

*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

Note : $t_{CP}$ is the internal operating clock cycle time. (Unit : ns)

• During normal operation

• In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



## 5. A/D Converter

### (1) Electrical Characteristics

($V_{CC}$ = $AV_{CC}$ = AVRH = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

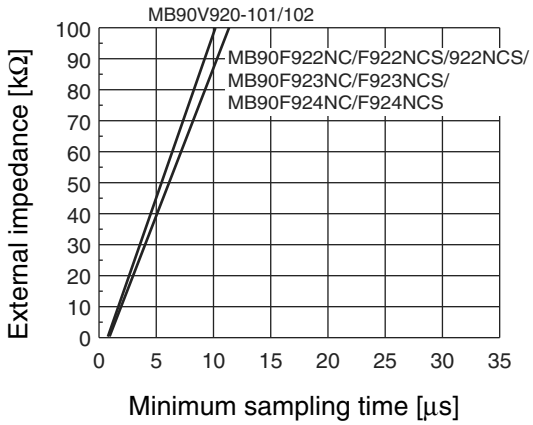
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | – 3.0 | — | + 3.0 | LSB | |
| Non-linear error | — | — | – 2.5 | — | + 2.5 | LSB | |
| Differential linear error | — | — | – 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | V | 1 LSB = (AVRH – $AV_{SS}$) / 1024 |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH – 3.5 LSB | AVRH – 1.5 LSB | AVRH + 0.5 LSB | V | |
| Sampling time | $t_{SMP}$ | — | 0.4 | — | 16500 | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 1.0 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| Compare time | $t_{CMP}$ | — | 0.66 | — | — | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 2.2 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| A/D conversion time | $t_{CNV}$ | — | 1.44 | — | — | µs | *1 |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | – 0.3 | — | + 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | 0 | — | AVRH | V | |
| Reference voltage | AV+ | AVRH | AVss + 2.7 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 2.3 | 6.0 | mA | |
| | $I_{AH}$ | | — | — | 5 | µA | *2 |
| Reference voltage supply current | $I_R$ | AVRH | — | 520 | 900 | µA | $V_{AVRH}$ = 5.0 V |
| | $I_{RH}$ | | — | — | 5 | µA | *2 |
| Inter-channel variation | — | AN0 to AN7 | — | — | 4 | LSB | |

*1 : The time per channel (4.5 V ≤ $AV_{CC}$ ≤ 5.5 V, and internal operating frequency = 32 MHz) .

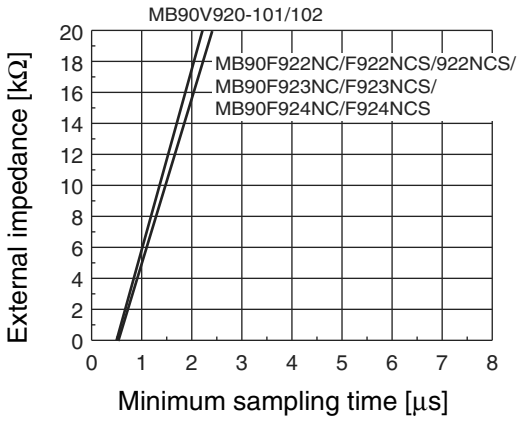
*2 : Defined as supply current (when $V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

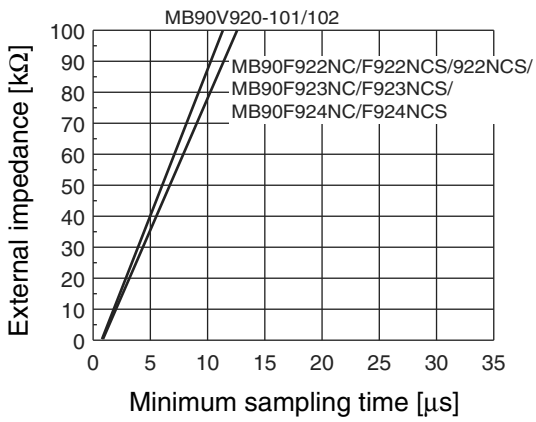



(External impedance = 0 kΩ to 20 kΩ)

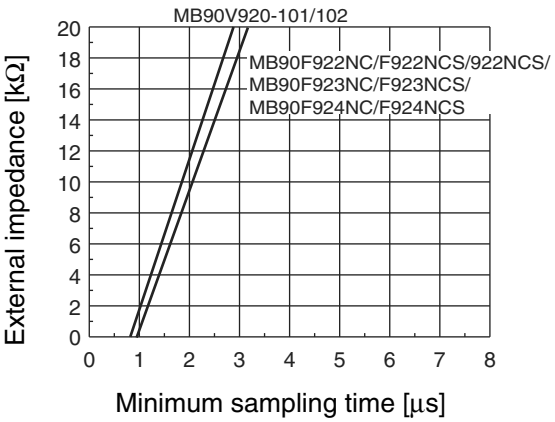



- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)




- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.

# MEMO