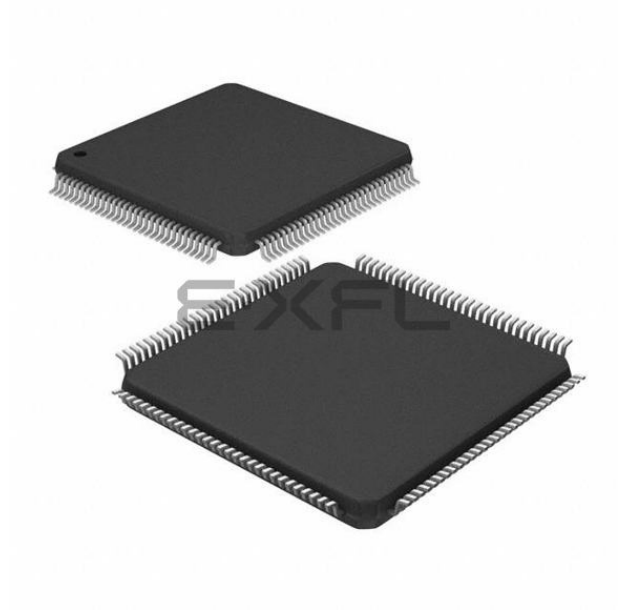
Infineon Technologies - MB90922NCSPMC-GS-169E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-169e1

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- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at f_{CP} = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

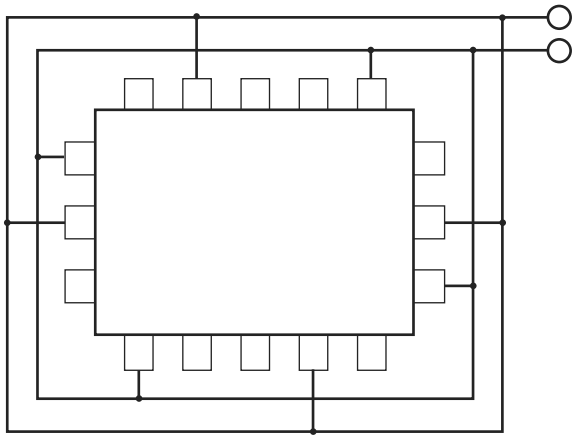
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH, 00000BH	(Disabled)				
00000CH	Port C data register	PDRC	R/W	Port C	XXXXXXXXB
00000DH	Port D data register	PDRD	R/W	Port D	XXXXXXXXB
00000EH	Port E data register	PDRE	R/W	Port E	XXXXXXXXB
00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 direction register	DDR1	R/W	Port 1	XX000000B
000012H	Port 2 direction register	DDR2	R/W	Port 2	000000XXB
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 direction register	DDR9	R/W	Port 9	X0000000B
00001AH	Analog input enable	ADER6	R/W	Port 6, A/D	11111111B
00001BH	(Disabled)				
00001CH	Port C direction register	DDRC	R/W	Port C	00000000B
00001DH	Port D direction register	DDRD	R/W	Port D	X0000000B
00001EH	Port E direction register	DDRE	R/W	Port E	XXXXX000B
00001FH	(Disabled)				
000020H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0B
000021H	Higher A/D control status register	ADCS1	R/W		0000000XB
000022H	Lower A/D control status register	ADCR0	R		00000000B
000023H	Higher A/D data register	ADCR1	R		XXXXXX00B

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Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

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Address	Register name	Symbol	Read/write	Resource name	Initial value
000054H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000B
000055H	Higher timer control status register 1	TMCSR1H	R/W		XXX10000B
000056H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
000057H					XXXXXXXXB
000058H	LCD output control register 1	LOCR1	R/W	LCDC	11111111B
000059H	LCD output control register 2	LOCR2	R/W		00000000B
00005AH	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	00000000B
00005BH	Higher sound control register 0	SGCRH0	R/W		0XXXX100B
00005CH	Frequency data register 0	SGFR0	R/W		XXXXXXXXB
00005DH	Amplitude data register 0	SGAR0	R/W		00000000B
00005EH	Decrement grade register 0	SGDR0	R/W		XXXXXXXXB
00005FH	Tone count register 0	SGTR0	R/W		XXXXXXXXB
000060H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXXB
000061H					XXXXXXXXB
000062H	Input capture register 1	IPCP1	R		XXXXXXXXB
000063H					XXXXXXXXB
000064H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXXB
000065H					XXXXXXXXB
000066H	Input capture register 3	IPCP3	R		XXXXXXXXB
000067H					XXXXXXXXB
000068H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000B
000069H	Input capture edge register 0/1	ICE01	R/W		XXX0X0XXB
00006AH	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000B
00006BH	Input capture edge register 2/3	ICE23	R/W		XXXXXXXXB
00006CH	Lower LCD control register	LCRL	R/W	LCD controller/ driver	00010000B
00006DH	Higher LCD control register	LCRH	R/W		00000000B
00006EH	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	00111000B
00006FH	ROM mirror	ROMM	W	ROM mirror	XXXXXXX1B
000070H to 00007FH	Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS"				
000080H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	000000X0B
000081H	(Disabled)				
000082H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	000000X0B

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Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111B
0000B1H	Interrupt control register 01	ICR01	R/W		00000111B
0000B2H	Interrupt control register 02	ICR02	R/W		00000111B
0000B3H	Interrupt control register 03	ICR03	R/W		00000111B
0000B4H	Interrupt control register 04	ICR04	R/W		00000111B
0000B5H	Interrupt control register 05	ICR05	R/W		00000111B
0000B6H	Interrupt control register 06	ICR06	R/W		00000111B
0000B7H	Interrupt control register 07	ICR07	R/W		00000111B
0000B8H	Interrupt control register 08	ICR08	R/W		00000111B
0000B9H	Interrupt control register 09	ICR09	R/W		00000111B
0000BAH	Interrupt control register 10	ICR10	R/W		00000111B
0000BBH	Interrupt control register 11	ICR11	R/W		00000111B
0000BCH	Interrupt control register 12	ICR12	R/W		00000111B
0000BDH	Interrupt control register 13	ICR13	R/W		00000111B
0000BEH	Interrupt control register 14	ICR14	R/W		00000111B
0000BFH	Interrupt control register 15	ICR15	R/W		00000111B
0000C0H to 0000C3H	(Disabled)				
0000C4H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000B
0000C5H	Serial control register 1	SCR1	R/W, W		00000000B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000B
0000C7H	Serial status register 1	SSR1	R/W, R		00001000B
0000C8H	Extended communication control register 1	ECCR1	R/W, R		000000XXB
0000C9H	Extended status control register 1	ESCR1	R/W		00000100B
0000CAH	Baud rate generator register 10	BGR10	R/W		00000000B
0000CBH	Baud rate generator register 11	BGR11	R/W, R		00000000B
0000CCH	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0B
0000CDH	Middle watch timer control register	WTCRM	R/W		00000000B
0000CEH	Higher watch timer control register	WTCRH	R/W		XXXXXX00B
0000CFH	Sub clock control register	PSCCR	W	Sub clock	XXXX0000B
0000D0H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000B
0000D1H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXB
0000D2H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000B
0000D3H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XXB

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003998H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXXB
003999H					XXXXXXXXB
00399AH	PWM2 compare register 3	PWC23	R/W		XXXXXXXXB
00399BH					XXXXXXXXB
00399CH	PWM1 select register 3	PWS13	R/W		00000000B
00399DH	PWM2 select register 3	PWS23	R/W		X0000000B
00399EH to 0039A5H	(Disabled)				
0039A6H	Flash write control register 0	FWR0	R/W	Flash I/F	00000000B
0039A7H	Flash write control register 1	FWR1			00000000B
0039A8H to 0039BFH	(Disabled)				
0039C0H to 0039DFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0039E0H to 0039FFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				
003A00H to 003AFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003B00H to 003BFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003C00H to 003CFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003D00H to 003DFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003E00H to 003EFFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
003F00H to 003FFFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
CAN0 received/CAN2 received	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	0CH	FFFFCCH			
CAN1 received/CAN3 received	×	#13	0DH	FFFFC8H	ICR01	0000B1H*1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	0EH	FFFFC4H			
Input capture 0	△	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10H	FFFFBCH			
Reload timer 0	△	#17	11H	FFFFB8H	ICR03	0000B3H*1	
Reload timer 2	△	#18	12H	FFFFB4H			
Input capture 1	△	#19	13H	FFFFB0H	ICR04	0000B4H*1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14H	FFFFACH			
Input capture 2	△	#21	15H	FFFFA8H	ICR05	0000B5H*1	
Reload timer 3	△	#22	16H	FFFFA4H			
Input capture 3/4/5/6/7	△	#23	17H	FFFFA0H	ICR06	0000B6H*1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18H	FFFF9CH			
PPG timer 0	△	#25	19H	FFFF98H	ICR07	0000B7H*1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1AH	FFFF94H			
PPG timer 1	△	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Reload timer 1	△	#28	1CH	FFFF8CH			
PPG timer 2/3/4/5	○	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Real time watch timer watch timer (sub clock)	×	#30	1EH	FFFF84H			
Free-run timer overflow/clear	×	#31	1FH	FFFF80H	ICR10	0000BAH *1	
A/D converter conversion complete	○	#32	20H	FFFF7CH			
Sound generator 0/1	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Time-base timer	×	#34	22H	FFFF74H			
UART2 RX	○	#35	23H	FFFF70H	ICR12	0000BCH*1	
UART2 TX	△	#36	24H	FFFF6CH			Low

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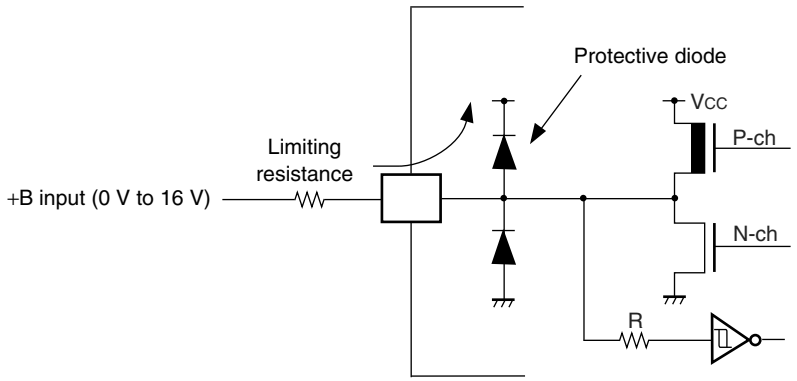
*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = –30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product

(Continued)

(Continued)

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCDC leakage current	I_{LCDC}	V0 to V3, COMm (m = 0 to 3) , SEGn, (n = 00 to 31)	—	—	—	5.0	µA	
LCD output impedance	Rvcom	COMn (n = 0 to 3)	—	—	—	4.5	kΩ	
	Rvseg	SEGn (n = 00 to 31)	—	—	—	17	kΩ	

* : Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

4. AC Characteristics

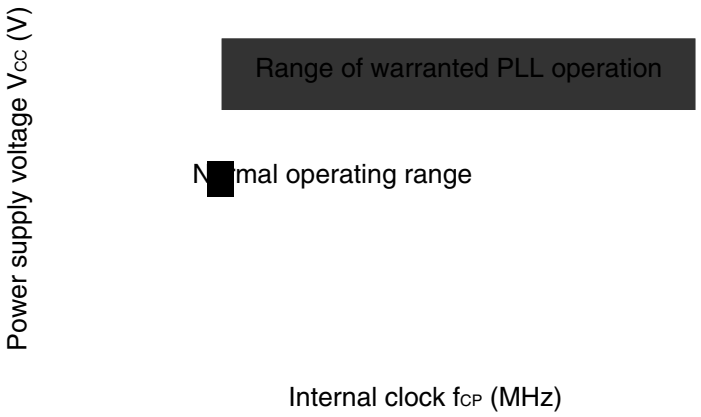
(1) Clock timing

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage



Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

(Continued)

(2) Reset input

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

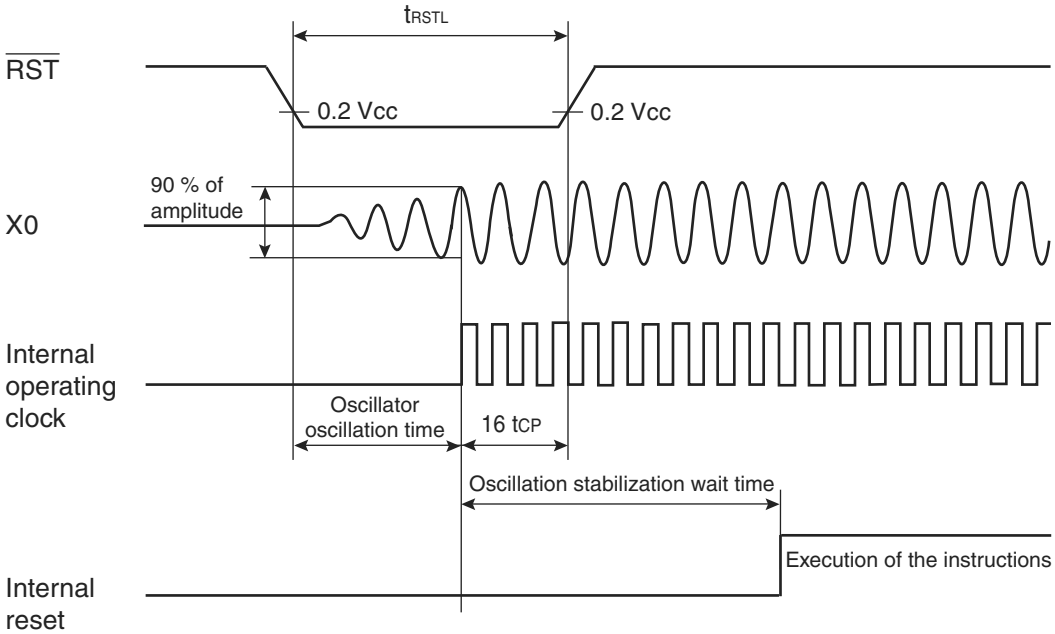
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	During normal operation
			Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	In time-base timer mode

*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

Note : t_{CP} is the internal operating clock cycle time. (Unit : ns)

• During normal operation

• In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



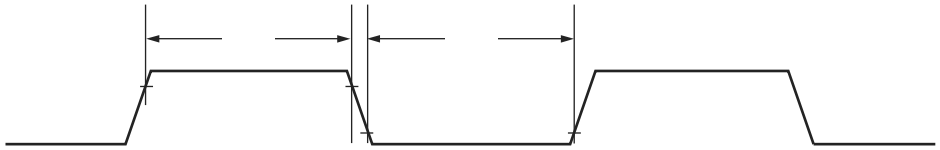
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to " (1) Clock timing".

- Timer input timing



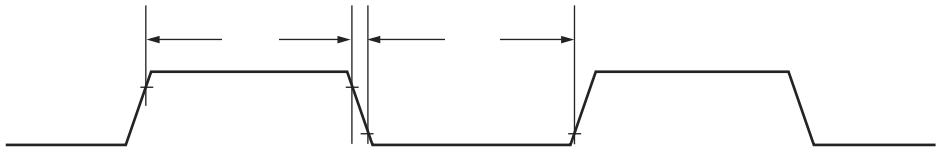
(6) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Trigger input timing



5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

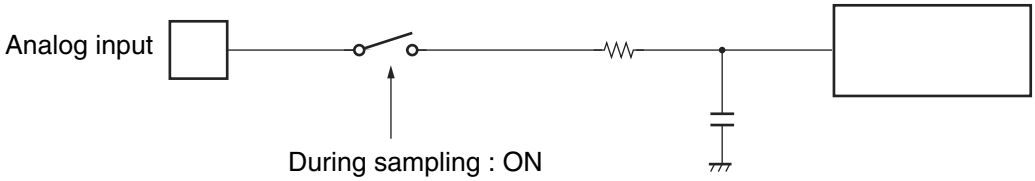
*1 : The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	12.1 kΩ (Max)	8.5 pF (Max)

MB90V920-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

Note : The values are reference values.

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department