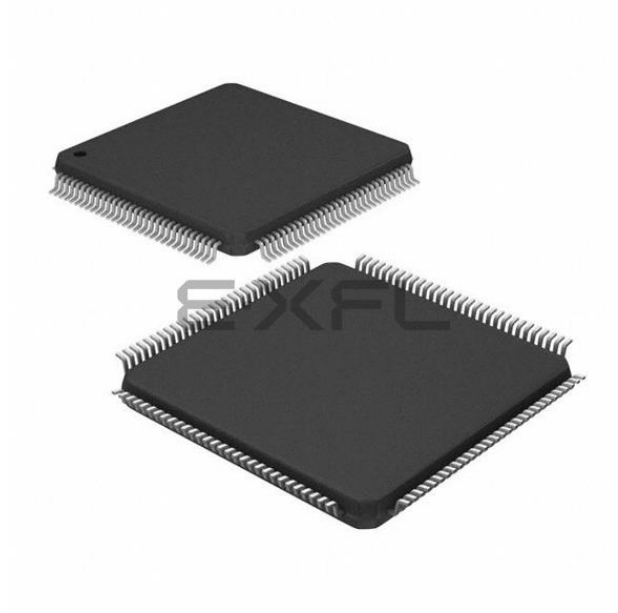
Infineon Technologies - MB90922NCSPMC-GS-171E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-171e1

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.9

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type*1	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	$\overline{\text{RST}}$	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
61	P54	I	General-purpose I/O port
	TX0		CAN interface 0 TX output pin
	TX2		CAN interface 2 TX output pin
	SGA1		Sound generator ch.1 SGA output pin
63	P55	I	General-purpose I/O port
	RX0		CAN interface 0 RX input pin
	RX2		CAN interface 2 RX input pin
	INT2		INT2 external interrupt input pin
91	P56	I	General-purpose I/O port
	SGO0		Sound generator ch.0 SGO output pin
	FRCK		Free-run timer clock input pin
92	P57	I	General-purpose I/O port
	SGA0		Sound generator ch.0 SGA output pin
39	P60	H	General-purpose I/O port
	AN0		A/D converter input pin
40	P61	H	General-purpose I/O port
	AN1		A/D converter input pin
41	P62	H	General-purpose I/O port
	AN2		A/D converter input pin
42	P63	H	General-purpose I/O port
	AN3		A/D converter input pin
43	P64	H	General-purpose I/O port
	AN4		A/D converter input pin
44	P65	H	General-purpose I/O port
	AN5		A/D converter input pin
45	P66	H	General-purpose I/O port
	AN6		A/D converter input pin
46	P67	H	General-purpose I/O port
	AN7		A/D converter input pin
67	P70	L	General-purpose output-only port
	PWM1P0		Stepping motor controller ch.0 output pin
68	P71	L	General-purpose output-only port
	PWM1M0		Stepping motor controller ch.0 output pin
69	P72	L	General-purpose output-only port
	PWM2P0		Stepping motor controller ch.0 output pin

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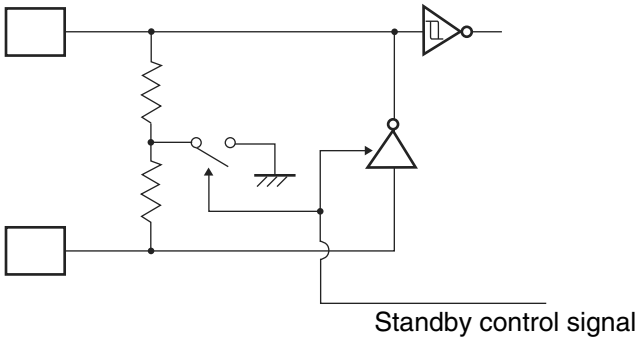
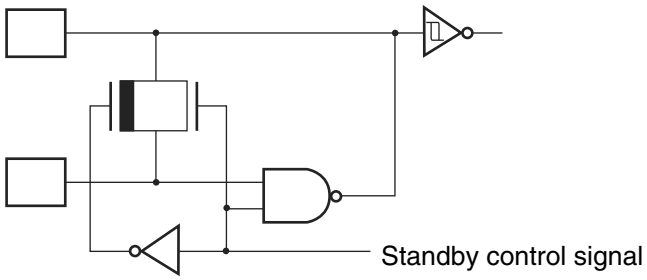
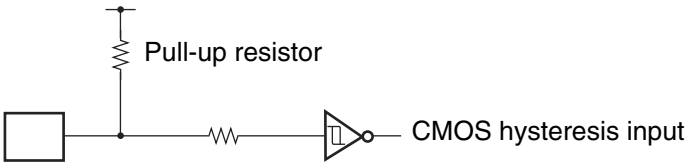
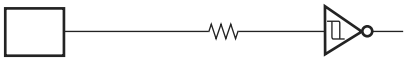
Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance : approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) • Attached pull-up resistor : approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.

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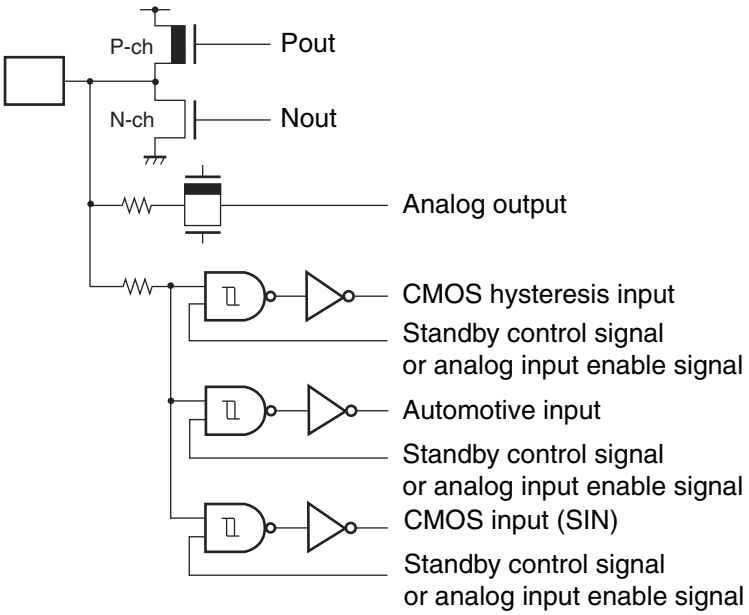
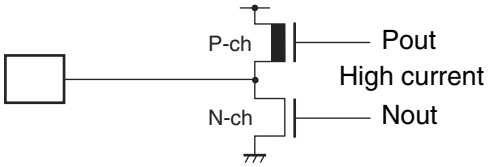
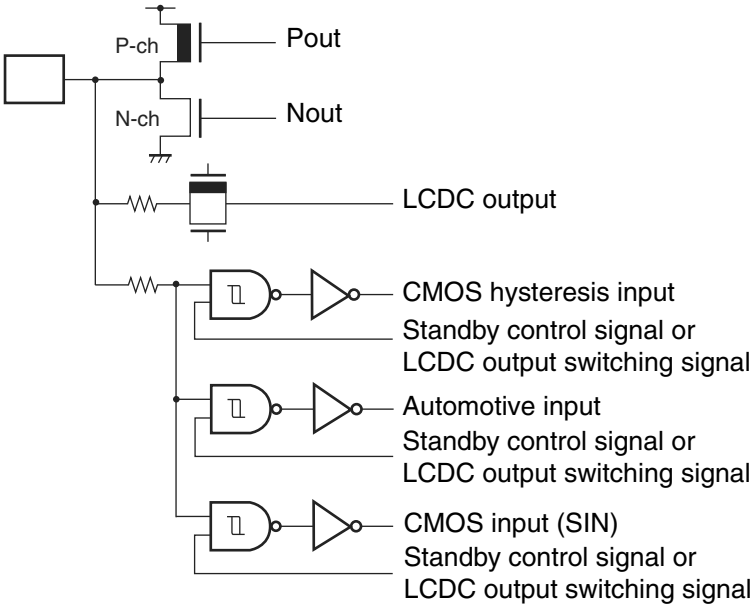
Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH, 00000BH	(Disabled)				
00000CH	Port C data register	PDRC	R/W	Port C	XXXXXXXXB
00000DH	Port D data register	PDRD	R/W	Port D	XXXXXXXXB
00000EH	Port E data register	PDRE	R/W	Port E	XXXXXXXXB
00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 direction register	DDR1	R/W	Port 1	XX000000B
000012H	Port 2 direction register	DDR2	R/W	Port 2	000000XXB
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 direction register	DDR9	R/W	Port 9	X0000000B
00001AH	Analog input enable	ADER6	R/W	Port 6, A/D	11111111B
00001BH	(Disabled)				
00001CH	Port C direction register	DDRC	R/W	Port C	00000000B
00001DH	Port D direction register	DDRD	R/W	Port D	X0000000B
00001EH	Port E direction register	DDRE	R/W	Port E	XXXXX000B
00001FH	(Disabled)				
000020H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0B
000021H	Higher A/D control status register	ADCS1	R/W		0000000XB
000022H	Lower A/D control status register	ADCR0	R		00000000B
000023H	Higher A/D data register	ADCR1	R		XXXXXX00B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003944H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXXB
003945H					XXXXXXXXB
003946H	Input capture register 7	IPCP7	R		XXXXXXXXB
003947H					XXXXXXXXB
003948H to 00394FH	(Disabled)				
003950H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXXB
003951H					XXXXXXXXB
003952H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXXB
003953H					XXXXXXXXB
003954H to 003957H	(Disabled)				
003958H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXXB
003959H					XXXXXXXXB
00395AH					XXXXXXXXB
00395BH	Second data register	WTSR	R/W		XX000000B
00395CH	Minute data register	WTMR	R/W		XX000000B
00395DH	Hour data register	WTHR	R/W		XXX00000B
00395EH	Day data register	WTDR	R/W		00X00001B
00395FH	(Disabled)				
003960H	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXXB
003961H					XXXXXXXXB
003962H					XXXXXXXXB
003963H					XXXXXXXXB
003964H					XXXXXXXXB
003965H					XXXXXXXXB
003966H					XXXXXXXXB
003967H					XXXXXXXXB
003968H					XXXXXXXXB
003969H					XXXXXXXXB
00396AH					XXXXXXXXB
00396BH					XXXXXXXXB
00396CH					XXXXXXXXB
00396DH					XXXXXXXXB
00396EH					XXXXXXXXB
00396FH					XXXXXXXXB

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003998H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXXB
003999H					XXXXXXXXB
00399AH	PWM2 compare register 3	PWC23	R/W		XXXXXXXXB
00399BH					XXXXXXXXB
00399CH	PWM1 select register 3	PWS13	R/W		00000000B
00399DH	PWM2 select register 3	PWS23	R/W		X0000000B
00399EH to 0039A5H	(Disabled)				
0039A6H	Flash write control register 0	FWR0	R/W	Flash I/F	00000000B
0039A7H	Flash write control register 1	FWR1			00000000B
0039A8H to 0039BFH	(Disabled)				
0039C0H to 0039DFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0039E0H to 0039FFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				
003A00H to 003AFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003B00H to 003BFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003C00H to 003CFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003D00H to 003DFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003E00H to 003EFFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
003F00H to 003FFFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				

List of Message Buffers (ID Registers)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00H to 003A1FH	003B00H to 003B1FH	003700H to 00371FH	003800H to 00381FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003B20H	003720H	003820H	ID register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
003A21H	003B21H	003721H	003821H				
003A22H	003B22H	003722H	003822H				XXXXX---B XXXXXXXXB
003A23H	003B23H	003723H	003823H				
003A24H	003B24H	003724H	003824H	ID register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
003A25H	003B25H	003725H	003825H				
003A26H	003B26H	003726H	003826H				XXXXX---B XXXXXXXXB
003A27H	003B27H	003727H	003827H				
003A28H	003B28H	003728H	003828H	ID register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
003A29H	003B29H	003729H	003829H				
003A2AH	003B2AH	00372AH	00382AH				XXXXX---B XXXXXXXXB
003A2BH	003B2BH	00372BH	00382BH				
003A2CH	003B2CH	00372CH	00382CH	ID register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
003A2DH	003B2DH	00372DH	00382DH				
003A2EH	003B2EH	00372EH	00382EH				XXXXX---B XXXXXXXXB
003A2FH	003B2FH	00372FH	00382FH				
003A30H	003B30H	003730H	003830H	ID register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
003A31H	003B31H	003731H	003831H				
003A32H	003B32H	003732H	003832H				XXXXX---B XXXXXXXXB
003A33H	003B33H	003733H	003833H				
003A34H	003B34H	003734H	003834H	ID register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
003A35H	003B35H	003735H	003835H				
003A36H	003B36H	003736H	003836H				XXXXX---B XXXXXXXXB
003A37H	003B37H	003737H	003837H				
003A38H	003B38H	003738H	003838H	ID register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
003A39H	003B39H	003739H	003839H				
003A3AH	003B3AH	00373AH	00383AH				XXXXX---B XXXXXXXXB
003A3BH	003B3BH	00373BH	00383BH				
003A3CH	003B3CH	00373CH	00383CH	ID register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
003A3DH	003B3DH	00373DH	00383DH				
003A3EH	003B3EH	00373EH	00383EH				XXXXX---B XXXXXXXXB
003A3FH	003B3FH	00373FH	00383FH				

(Continued)

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
CAN0 received/CAN2 received	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	0CH	FFFFCCH			
CAN1 received/CAN3 received	×	#13	0DH	FFFFC8H	ICR01	0000B1H*1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	0EH	FFFFC4H			
Input capture 0	△	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10H	FFFFBCH			
Reload timer 0	△	#17	11H	FFFFB8H	ICR03	0000B3H*1	
Reload timer 2	△	#18	12H	FFFFB4H			
Input capture 1	△	#19	13H	FFFFB0H	ICR04	0000B4H*1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14H	FFFFACH			
Input capture 2	△	#21	15H	FFFFA8H	ICR05	0000B5H*1	
Reload timer 3	△	#22	16H	FFFFA4H			
Input capture 3/4/5/6/7	△	#23	17H	FFFFA0H	ICR06	0000B6H*1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18H	FFFF9CH			
PPG timer 0	△	#25	19H	FFFF98H	ICR07	0000B7H*1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1AH	FFFF94H			
PPG timer 1	△	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Reload timer 1	△	#28	1CH	FFFF8CH			
PPG timer 2/3/4/5	○	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Real time watch timer watch timer (sub clock)	×	#30	1EH	FFFF84H			
Free-run timer overflow/clear	×	#31	1FH	FFFF80H	ICR10	0000BAH *1	
A/D converter conversion complete	○	#32	20H	FFFF7CH			
Sound generator 0/1	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Time-base timer	×	#34	22H	FFFF74H			
UART2 RX	○	#35	23H	FFFF70H	ICR12	0000BCH*1	
UART2 TX	△	#36	24H	FFFF6CH			Low

(Continued)

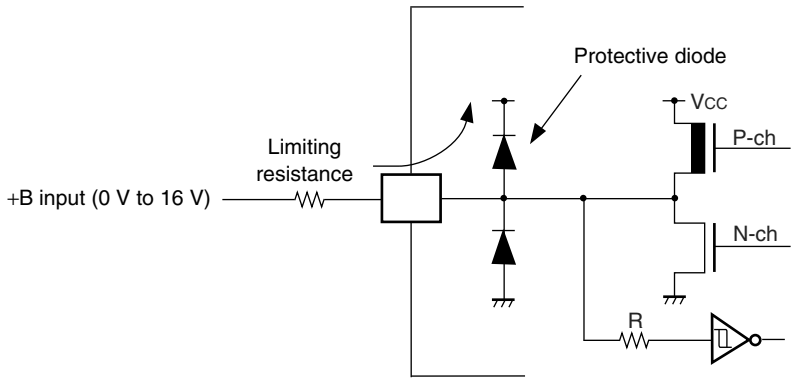
(Continued)

*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

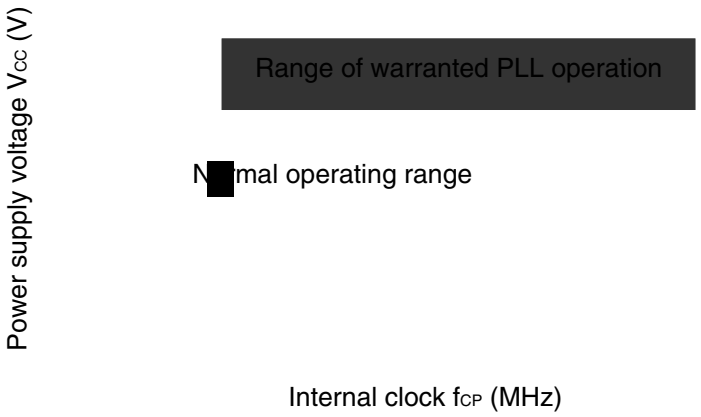
• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage

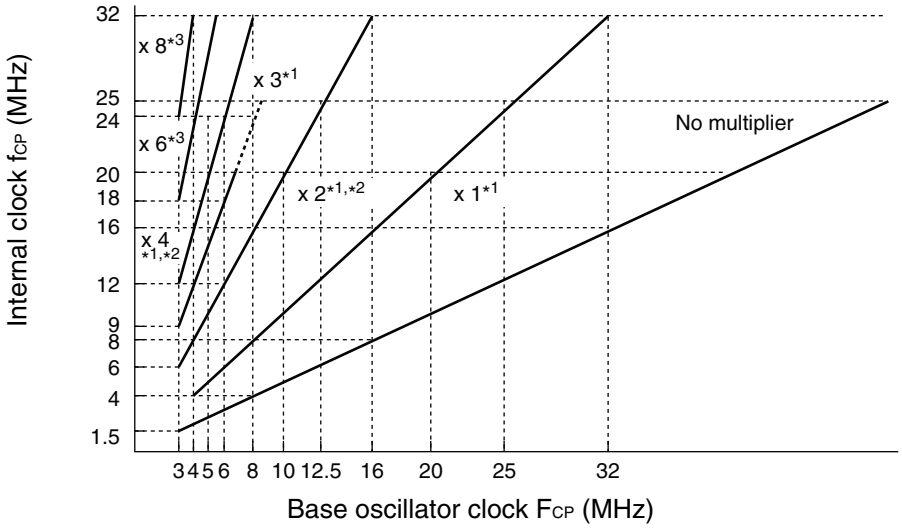


Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

(Continued)

(Continued)

Base oscillator frequency vs. Internal operating clock frequency



*1 : When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example] When using a base oscillator frequency of 24 MHz at PLL × 1 :
CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4,CS2 bit = "1"
[Example] When using a base oscillator frequency of 6 MHz at PLL × 3 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, the following settings are also supported.
PLL × 2 : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4 : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3 : When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example] When using a base oscillator frequency of 4 MHz at PLL × 6 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"
[Example] When using a base oscillator frequency of 3 MHz at PLL × 8 :
CKSCR register : CS1 bit = "1", CS0 bit = "1"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

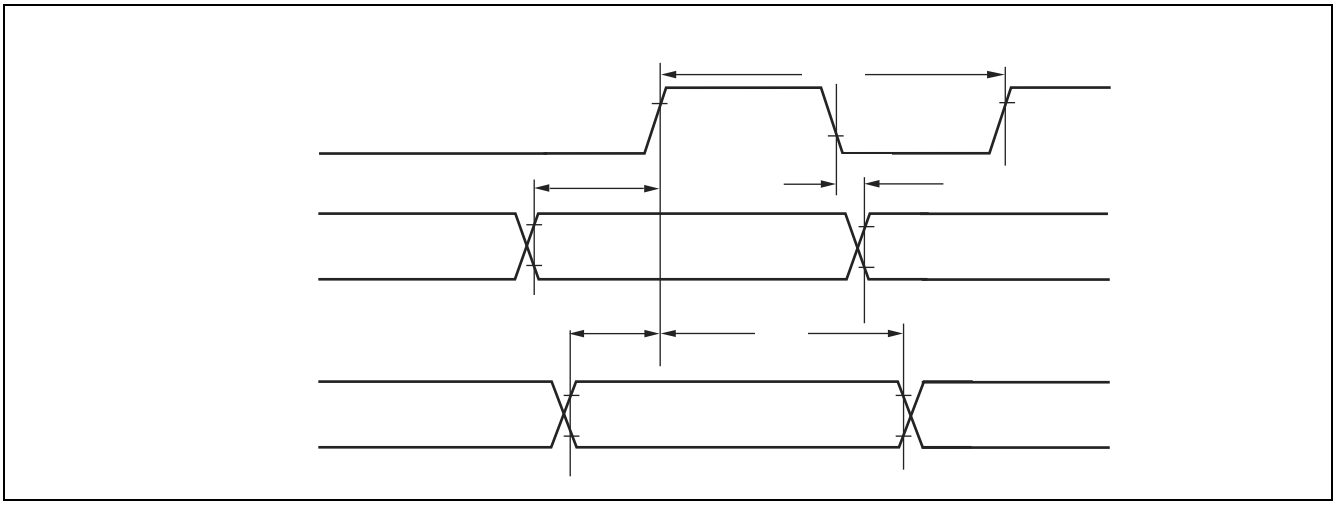
*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.



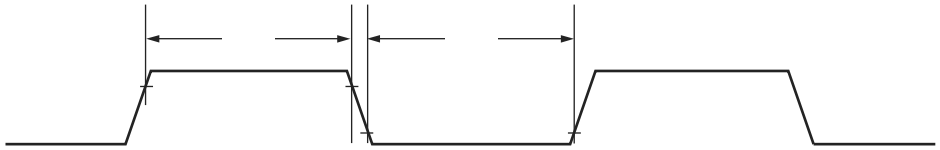
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to " (1) Clock timing".

- Timer input timing



5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

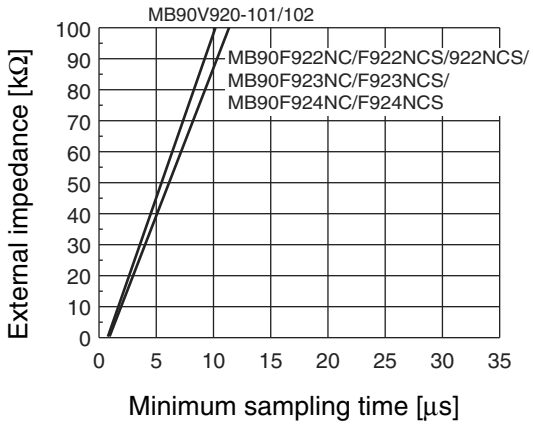
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

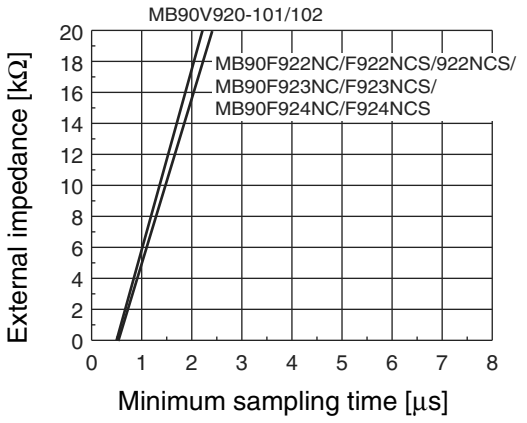
*2 : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

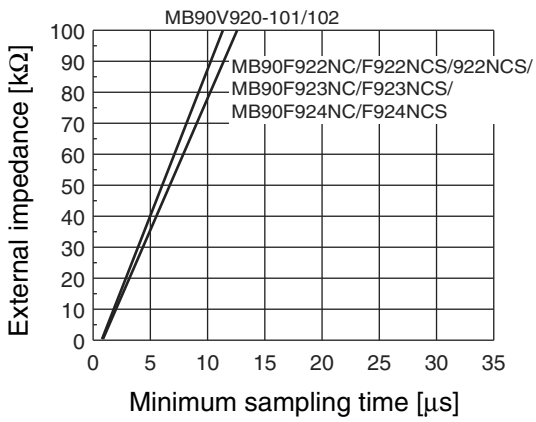


(External impedance = 0 kΩ to 20 kΩ)

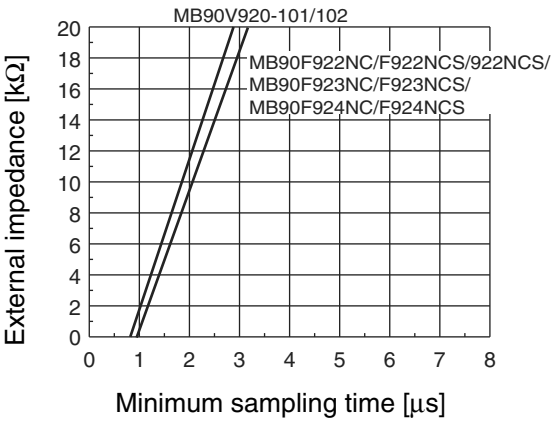


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.

6. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	0.9	3.6	s	Excludes pre-programming before erase
Word (16-bit width) programming time		—	23	370	µs	Excludes system-level overhead
Chip programming time	T_A = + 25 °C, V_{CC} = 5.0 V	—	3.4	55	s	
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .