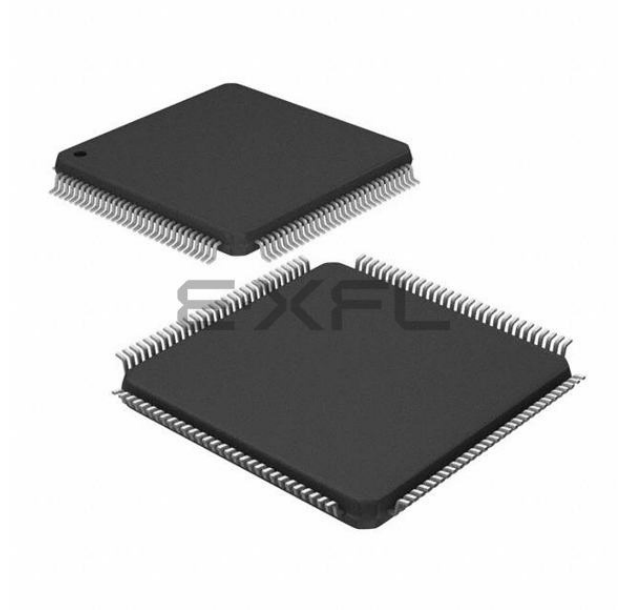
Infineon Technologies - MB90922NCSPMC-GS-182E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-182e1

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

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Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

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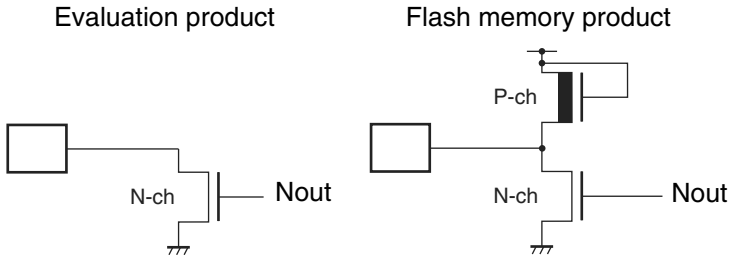
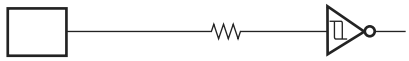
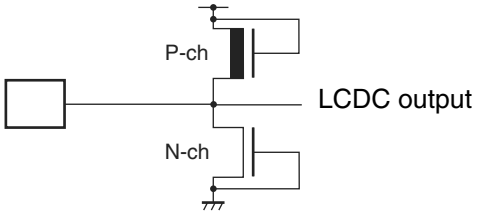
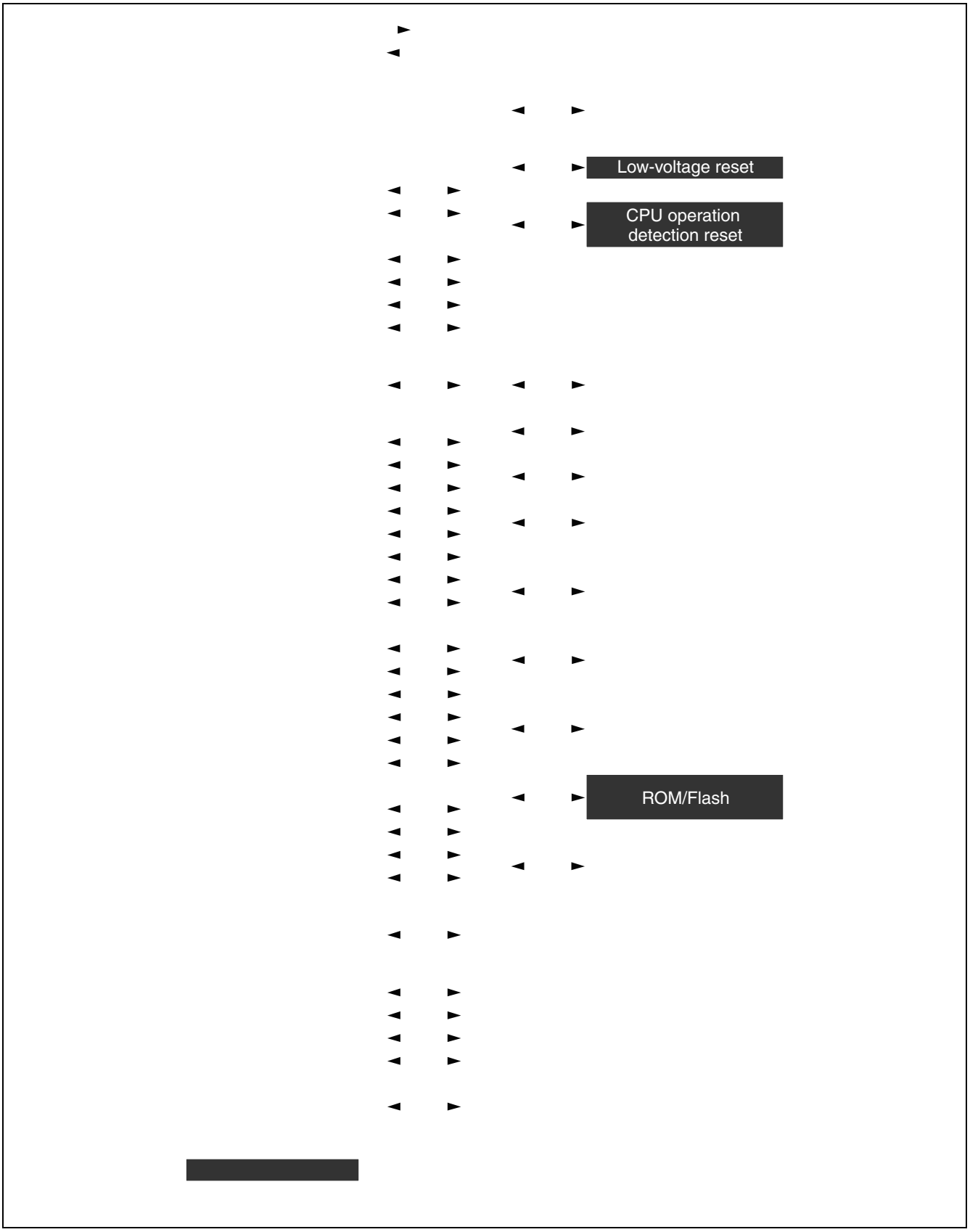
Type	Circuit	Remarks
N		N-ch open-drain pin I_{OL} = 4 mA
O		Input-only pin Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
P		LCDC output pin (COM pin)

■ BLOCK DIAGRAM



Address	Register name	Symbol	Read/write	Resource name	Initial value
000083H	(Disabled)				
000084H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	000000X0B
000085H	(Disabled)				
000086H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	000000X0B
000087H	(Disabled)				
000088H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXX111B
000089H	(Disabled)				
00008AH	A/D setting register 0	ADSR0	R/W	A/D converter	00000000B
00008BH	A/D setting register 1	ADSR1	R/W		00000000B
00008CH	Port input level select 0	PIL0	R/W	Port input level select	00000000B
00008DH	Port input level select 1	PIL1	R/W		XXXX0000B
00008EH	Port input level select 2	PIL2	R/W		XXXX0000B
00008FH to 00009DH	(Disabled)				
00009EH	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0XB
00009FH	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	XXXXXXX0B
0000A0H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000B
0000A1H	Clock select register	CKSCR	R/W, R		11111100B
0000A2H to 0000A7H	(Disabled)				
0000A8H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111B
0000A9H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100B
0000AAH	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000B
0000ABH to 0000ADH	(Disabled)				
0000AEH	Flash memory control status register	FMCS	R/W	Flash interface	000X0000B
0000AFH	(Disabled)				

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111B
0000B1H	Interrupt control register 01	ICR01	R/W		00000111B
0000B2H	Interrupt control register 02	ICR02	R/W		00000111B
0000B3H	Interrupt control register 03	ICR03	R/W		00000111B
0000B4H	Interrupt control register 04	ICR04	R/W		00000111B
0000B5H	Interrupt control register 05	ICR05	R/W		00000111B
0000B6H	Interrupt control register 06	ICR06	R/W		00000111B
0000B7H	Interrupt control register 07	ICR07	R/W		00000111B
0000B8H	Interrupt control register 08	ICR08	R/W		00000111B
0000B9H	Interrupt control register 09	ICR09	R/W		00000111B
0000BAH	Interrupt control register 10	ICR10	R/W		00000111B
0000BBH	Interrupt control register 11	ICR11	R/W		00000111B
0000BCH	Interrupt control register 12	ICR12	R/W		00000111B
0000BDH	Interrupt control register 13	ICR13	R/W		00000111B
0000BEH	Interrupt control register 14	ICR14	R/W		00000111B
0000BFH	Interrupt control register 15	ICR15	R/W		00000111B
0000C0H to 0000C3H	(Disabled)				
0000C4H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000B
0000C5H	Serial control register 1	SCR1	R/W, W		00000000B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000B
0000C7H	Serial status register 1	SSR1	R/W, R		00001000B
0000C8H	Extended communication control register 1	ECCR1	R/W, R		000000XXB
0000C9H	Extended status control register 1	ESCR1	R/W		00000100B
0000CAH	Baud rate generator register 10	BGR10	R/W		00000000B
0000CBH	Baud rate generator register 11	BGR11	R/W, R		00000000B
0000CCH	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0B
0000CDH	Middle watch timer control register	WTCRM	R/W		00000000B
0000CEH	Higher watch timer control register	WTCRH	R/W		XXXXXX00B
0000CFH	Sub clock control register	PSCCR	W	Sub clock	XXXX0000B
0000D0H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000B
0000D1H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXB
0000D2H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000B
0000D3H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XXB

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■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

List of Control Registers(2)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
000040H	000070H	0039C0H	0039D0H	Message buffer valid register	BVALR	R/W	00000000B
000041H	000071H	0039C1H	0039D1H				00000000B
000042H	000072H	0039C2H	0039D2H	Transmit request register	TREQR	R/W	00000000B
000043H	000073H	0039C3H	0039D3H				00000000B
000044H	000074H	0039C4H	0039D4H	Transmit cancel register	TCANR	W	00000000B
000045H	000075H	0039C5H	0039D5H				00000000B
000046H	000076H	0039C6H	0039D6H	Transmit complete register	TCR	R/W	00000000B
000047H	000077H	0039C7H	0039D7H				00000000B
000048H	000078H	0039C8H	0039D8H	Receive complete register	RCR	R/W	00000000B
000049H	000079H	0039C9H	0039D9H				00000000B
00004AH	00007AH	0039CAH	0039DAH	Remote request receive register	RRTRR	R/W	00000000B
00004BH	00007BH	0039CBH	0039DBH				00000000B
00004CH	00007CH	0039CCH	0039DCH	Receive overrun register	ROVRR	R/W	00000000B
00004DH	00007DH	0039CDH	0039DDH				00000000B
00004EH	00007EH	0039CEH	0039DEH	Receive interrupt enable register	RIER	R/W	00000000B
00004FH	00007FH	0039CFH	0039DFH				00000000B
003C08H	003D08H	003E08H	003F08H	IDE register	IDER	R/W	XXXXXXXXB
003C09H	003D09H	003E09H	003F09H				XXXXXXXXB
003C0AH	003D0AH	003E0AH	003F0AH	Transmit RTR register	TRTRR	R/W	00000000B
003C0BH	003D0BH	003E0BH	003F0BH				00000000B
003C0CH	003D0CH	003E0CH	003F0CH	Remote frame receive wait register	RFWTR	R/W	XXXXXXXXB
003C0DH	003D0DH	003E0DH	003F0DH				XXXXXXXXB
003C0EH	003D0EH	003E0EH	003F0EH	Transmit interrupt enable register	TIER	R/W	00000000B
003C0FH	003D0FH	003E0FH	003F0FH				00000000B
003C10H	003D10H	003E10H	003F10H	Acceptance mask select register	AMSR	R/W	XXXXXXXXB
003C11H	003D11H	003E11H	003F11H				XXXXXXXXB
003C12H	003D12H	003E12H	003F12H				XXXXXXXXB
003C13H	003D13H	003E13H	003F13H				XXXXXXXXB
003C14H	003D14H	003E14H	003F14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXXB
003C15H	003D15H	003E15H	003F15H				XXXXXXXXB
003C16H	003D16H	003E16H	003F16H				XXXXX---B
003C17H	003D17H	003E17H	003F17H				XXXXXXXXB
003C18H	003D18H	003E18H	003F18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXXB
003C19H	003D19H	003E19H	003F19H				XXXXXXXXB
003C1AH	003D1AH	003E1AH	003F1AH				XXXXX---B
003C1BH	003D1BH	003E1BH	003F1BH				XXXXXXXXB

(Continued)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40H	003B40H	003740H	003840H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003A41H	003B41H	003741H	003841H				
003A42H	003B42H	003742H	003842H				XXXXX---B XXXXXXXXB
003A43H	003B43H	003743H	003843H				
003A44H	003B44H	003744H	003844H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003A45H	003B45H	003745H	003845H				
003A46H	003B46H	003746H	003846H				XXXXX---B XXXXXXXXB
003A47H	003B47H	003747H	003847H				
003A48H	003B48H	003748H	003848H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003A49H	003B49H	003749H	003849H				
003A4AH	003B4AH	00374AH	00384AH				XXXXX---B XXXXXXXXB
003A4BH	003B4BH	00374BH	00384BH				
003A4CH	003B4CH	00374CH	00384CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
003A4DH	003B4DH	00374DH	00384DH				
003A4EH	003B4EH	00374EH	00384EH				XXXXX---B XXXXXXXXB
003A4FH	003B4FH	00374FH	00384FH				
003A50H	003B50H	003750H	003850H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003A51H	003B51H	003751H	003851H				
003A52H	003B52H	003752H	003852H				XXXXX---B XXXXXXXXB
003A53H	003B53H	003753H	003853H				
003A54H	003B54H	003754H	003854H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003A55H	003B55H	003755H	003855H				
003A56H	003B56H	003756H	003856H				XXXXX---B XXXXXXXXB
003A57H	003B57H	003757H	003857H				
003A58H	003B58H	003758H	003858H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003A59H	003B59H	003759H	003859H				
003A5AH	003B5AH	00375AH	00385AH				XXXXX---B XXXXXXXXB
003A5BH	003B5BH	00375BH	00385BH				
003A5CH	003B5CH	00375CH	00385CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
003A5DH	003B5DH	00375DH	00385DH				
003A5EH	003B5EH	00375EH	00385EH				XXXXX---B XXXXXXXXB
003A5FH	003B5FH	00375FH	00385FH				

List of Message Buffers (Data register)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A80H to 003A87H	003B80H to 003B87H	003780H to 003787H	003880H to 003887H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
003A88H to 003A8FH	003B88H to 003B8FH	003788H to 00378FH	003888H to 00388FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003A90H to 003A97H	003B90H to 003B97H	003790H to 003797H	003890H to 003897H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003A98H to 003A9FH	003B98H to 003B9FH	003798H to 00379FH	003898H to 00389FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
003AA0H to 003AA7H	003BA0H to 003BA7H	0037A0H to 0037A7H	0038A0H to 0038A7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
003AA8H to 003AAFH	003BA8H to 003BAFH	0037A8H to 0037AFH	0038A8H to 0038AFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
003AB0H to 003AB7H	003BB0H to 003BB7H	0037B0H to 0037B7H	0038B0H to 0038B7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
003AB8H to 003ABFH	003BB8H to 003BBFH	0037B8H to 0037BFH	0038B8H to 0038BFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	003BC0H to 003BC7H	0037C0H to 0037C7H	0038C0H to 0038C7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	003BC8H to 003BCFH	0037C8H to 0037CFH	0038C8H to 0038CFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
003AD0H to 003AD7H	003BD0H to 003BD7H	0037D0H to 0037D7H	0038D0H to 0038D7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	003BD8H to 003BDFH	0037D8H to 0037DFH	0038D8H to 0038DFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	003BE0H to 003BE7H	0037E0H to 0037E7H	0038E0H to 0038E7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	003BE8H to 003BEFH	0037E8H to 0037EFH	0038E8H to 0038EFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	003BF0H to 003BF7H	0037F0H to 0037F7H	0038F0H to 0038F7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	003BF8H to 003BFFH	0037F8H to 0037FFH	0038F8H to 0038FFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

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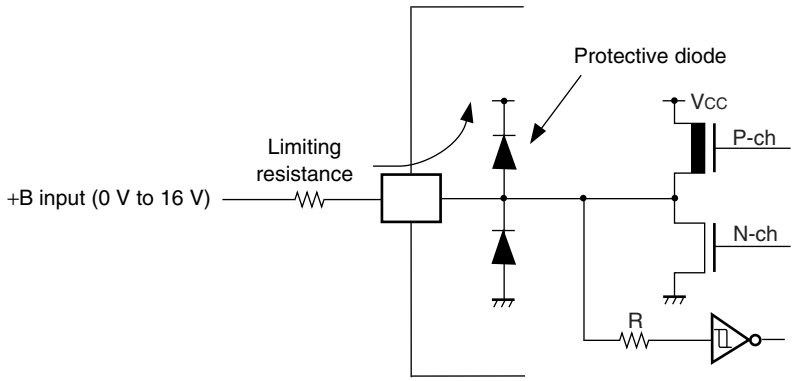
*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

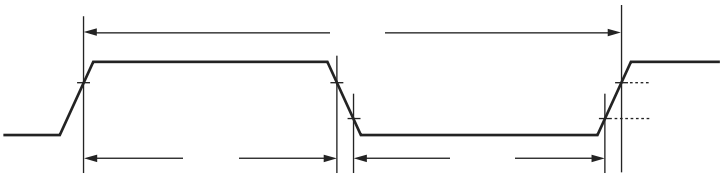
3. DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

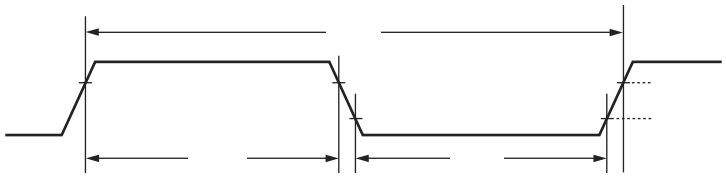
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHA}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHC}	—	—	0.7 V_{CC}	—	—	V	$\overline{RST}$ input pin (CMOS hysteresis)
"L" level input voltage	V_{ILA}	—	—	—	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	—	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	—	—	0.3 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
Power supply current*	I_{CC}	V_{CC}	Maximum operating frequency F_{CP} = 32 MHz, normal operation	—	35	45	mA	
			Maximum operating frequency F_{CP} = 32 MHz, writing Flash memory	—	55	65	mA	
	I_{CCS}		Operating frequency F_{CP} = 32 MHz, sleep mode	—	13	20	mA	
	I_{CTS}		Operating frequency F_{CP} = 2 MHz, time-base timer mode	—	0.6	1.0	mA	
	I_{CTSPLL}		Operating frequency F_{CP} = 32 MHz, PLL timer mode, External frequency = 4 MHz	—	2.5	4	mA	
	I_{CCL}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub clock operation	—	120	270	µA	
	I_{CCLS}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub sleep operation	—	100	200	µA	
	I_{CCT}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, watch mode	—	90	180	µA	
	I_{CCH}		T_A = + 25 °C, stop mode	—	80	170	µA	

(Continued)

• X0, X1 clock timing



• X0A, X1A clock timing



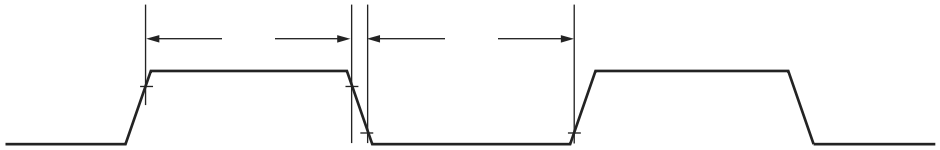
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to " (1) Clock timing".

- Timer input timing



5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

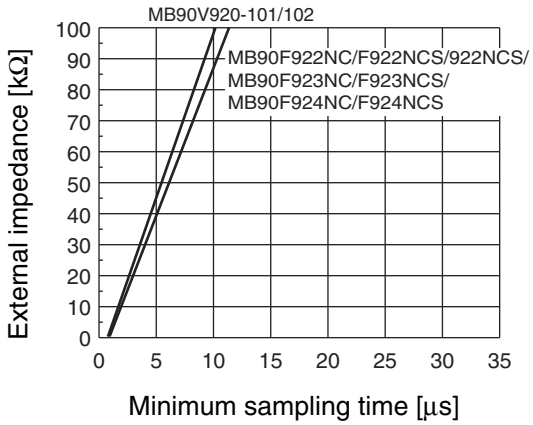
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

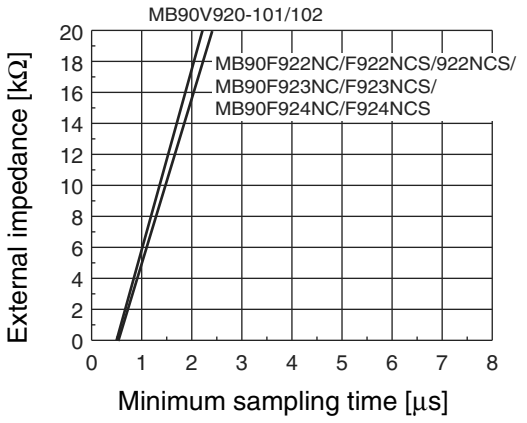
*2 : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

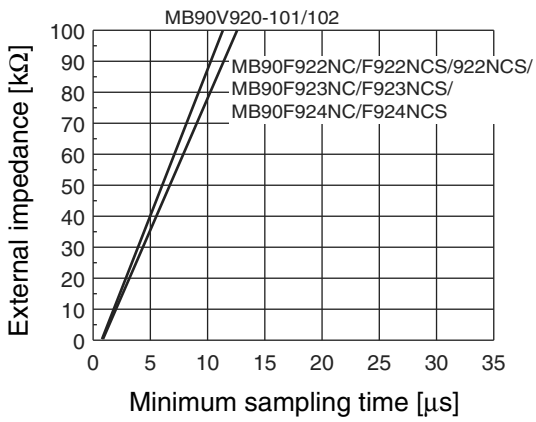


(External impedance = 0 kΩ to 20 kΩ)

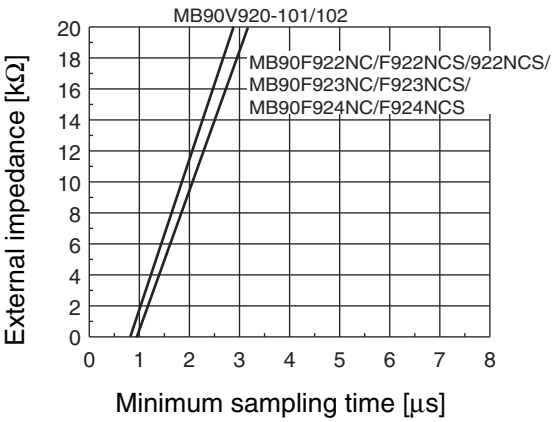


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.

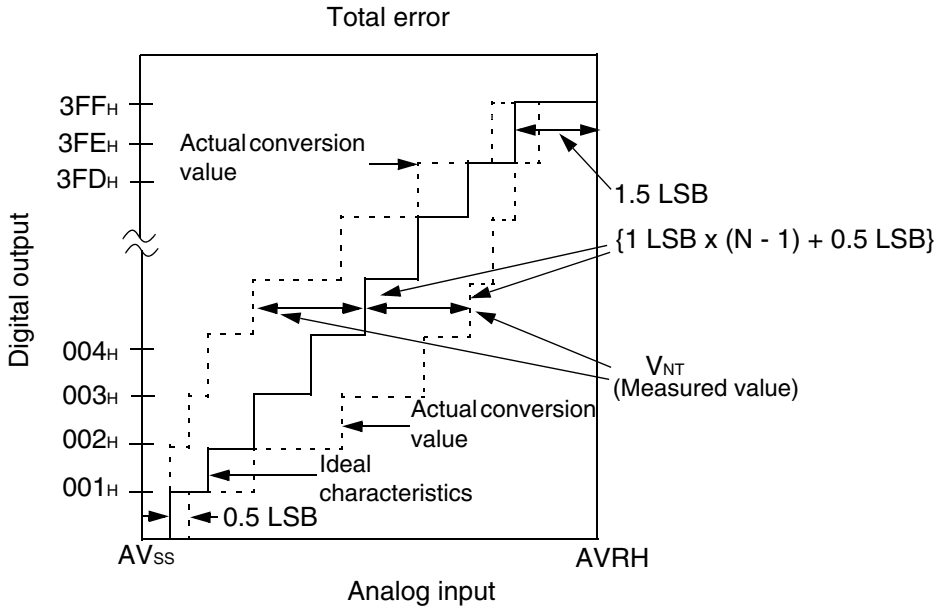
(2) Definition of terms

Resolution : Analog changes that are identifiable by the A/D converter.

Non-Linear error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ←→ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111") from actual conversion characteristics.

Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.

Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

V_{OT} (Ideal) = AVss + 0.5 LSB [V]

V_{FST} (Ideal) = AVRH − 1.5 LSB [V]

V_{NT} : Voltage when the digital output changes from (N - 1) to N

(Continued)

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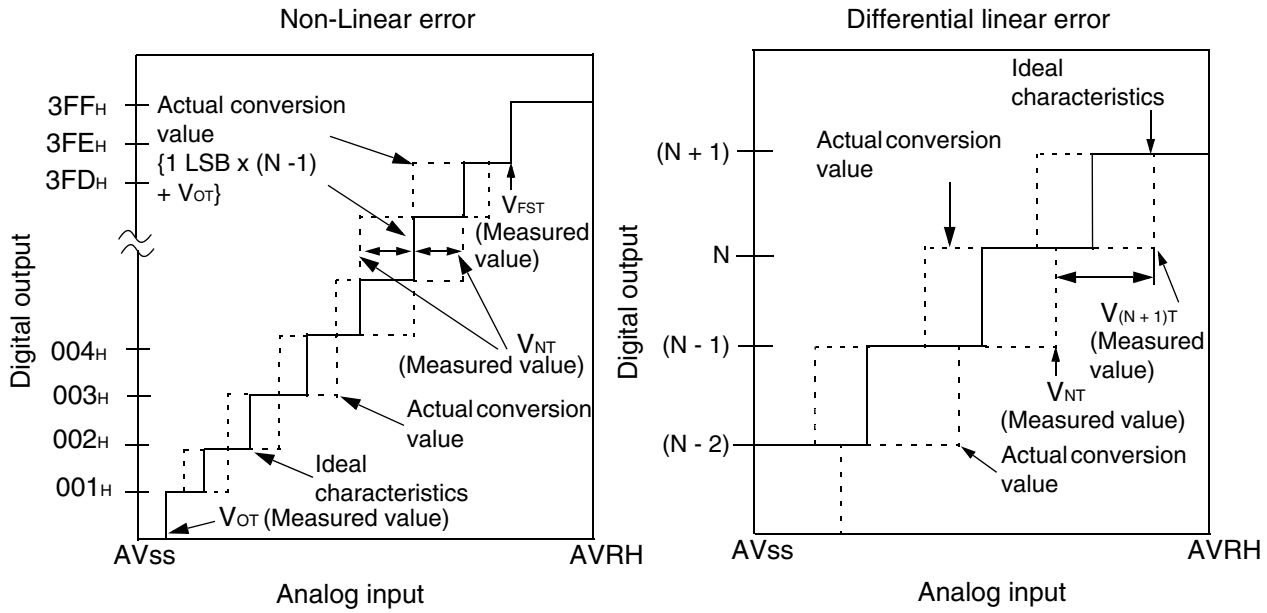

$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; • Serial communication • Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970$_H$”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR

The vertical lines marked in the left side of the page show the changes.