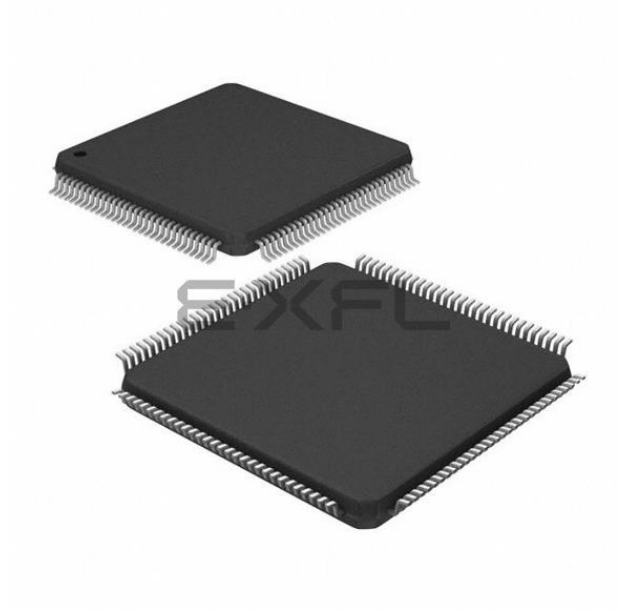
Infineon Technologies - MB90922NCSPMC-GS-200E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-200e1

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type*1	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	$\overline{\text{RST}}$	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

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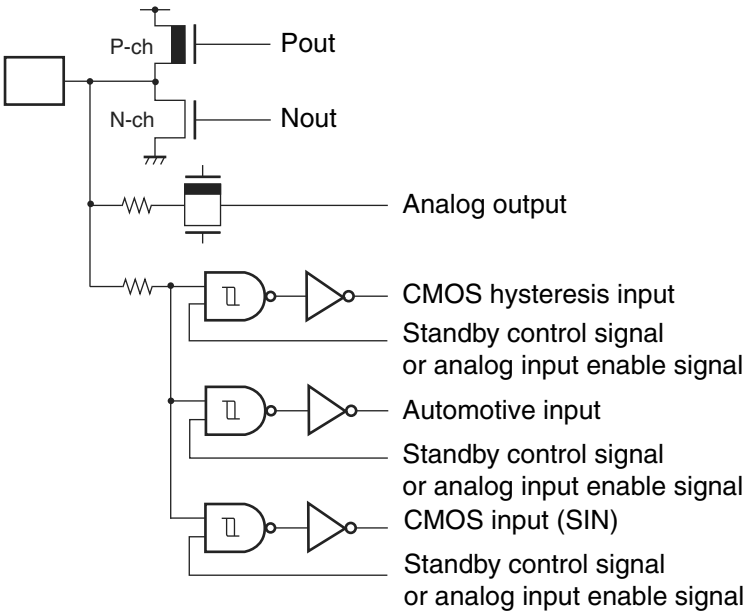
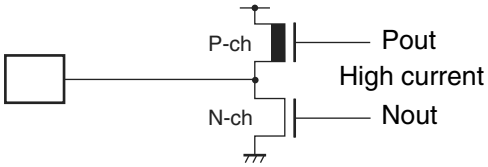
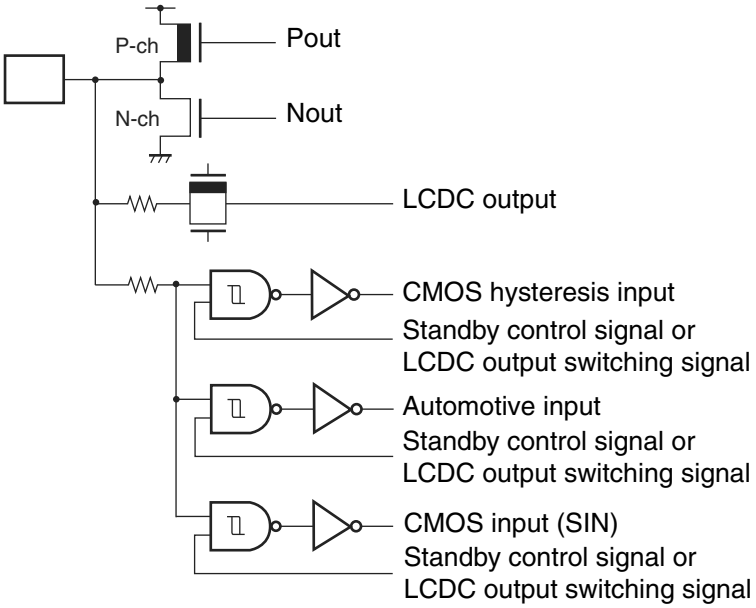
Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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- **Serial communication**

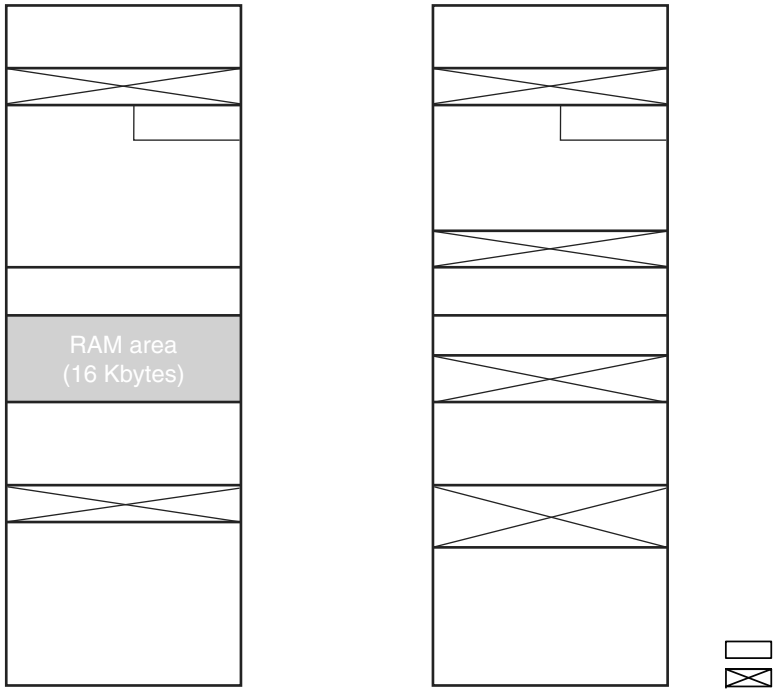
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
003970H to 003973H	(Disabled)				
003974H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXXB
003975H	Amplitude data register 1	SGAR1	R/W		00000000B
003976H	Decrement grade register 1	SGDR1	R/W		XXXXXXXXB
003977H	Tone count register 1	SGTR1	R/W		XXXXXXXXB
003978H to 00397FH	(Disabled)				
003980H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXXB
003981H					XXXXXXXXB
003982H	PWM2 compare register 0	PWC20	R/W		XXXXXXXXB
003983H					XXXXXXXXB
003984H	PWM1 select register 0	PWS10	R/W		00000000B
003985H	PWM2 select register 0	PWS20	R/W		X0000000B
003986H, 003987H	(Disabled)				
003988H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXXB
003989H					XXXXXXXXB
00398AH	PWM2 compare register 1	PWC21	R/W		XXXXXXXXB
00398BH					XXXXXXXXB
00398CH	PWM1 select register 1	PWS11	R/W		00000000B
00398DH	PWM2 select register 1	PWS21	R/W		X0000000B
00398EH, 00398FH	(Disabled)				
003990H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXXB
003991H					XXXXXXXXB
003992H	PWM2 compare register 2	PWC22	R/W		XXXXXXXXB
003993H					XXXXXXXXB
003994H	PWM1 select register 2	PWS12	R/W		00000000B
003995H	PWM2 select register 2	PWS22	R/W		X0000000B
003996H, 003997H	(Disabled)				

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■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

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Interrupt source	EI²OS corresponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
UART 1 RX	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART 1 TX	△	#38	26H	FFFF64H			
UART 0 RX	◎	#39	27H	FFFF60H	ICR14	0000BEH*1	
UART 0 TX	△	#40	28H	FFFF5CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH*1	
Delay interrupt generator module	×	#42	2AH	FFFF54H			Low

◎ : Usable, and has expanded intelligent I/O services (EI²OS) stop function
○ : Usable
△ : Usable when interrupt sources sharing ICR are not in use
× : Unusable

*1 : • Peripheral functions that share the ICR register have the same interrupt level.
• If the expanded intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.
• When the expanded intelligent I/O service (EI²OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2 : Priority applies when interrupts of the same level are generated.

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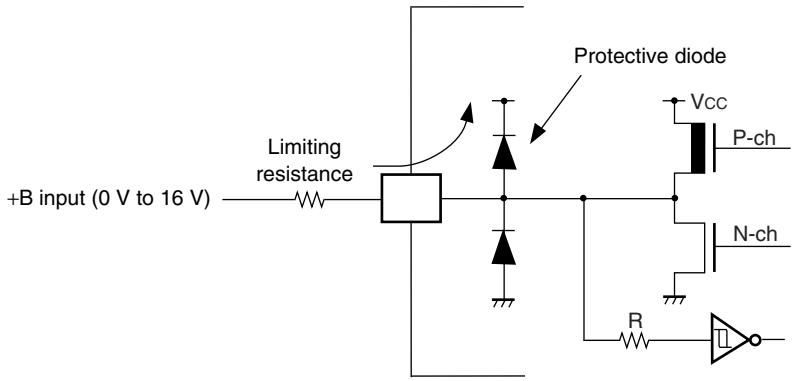
*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = –30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product

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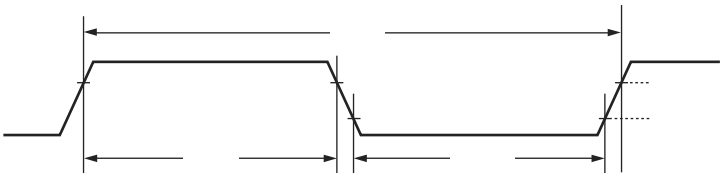
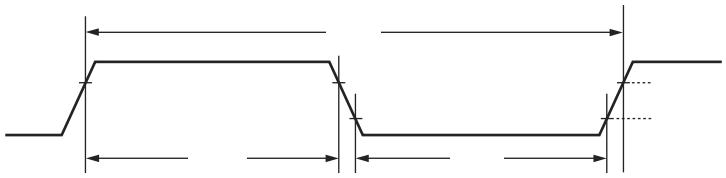
• X0, X1 clock timing



• X0A, X1A clock timing



(4) UART0/1/2/3 (LIN/SCI)

- **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}			t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

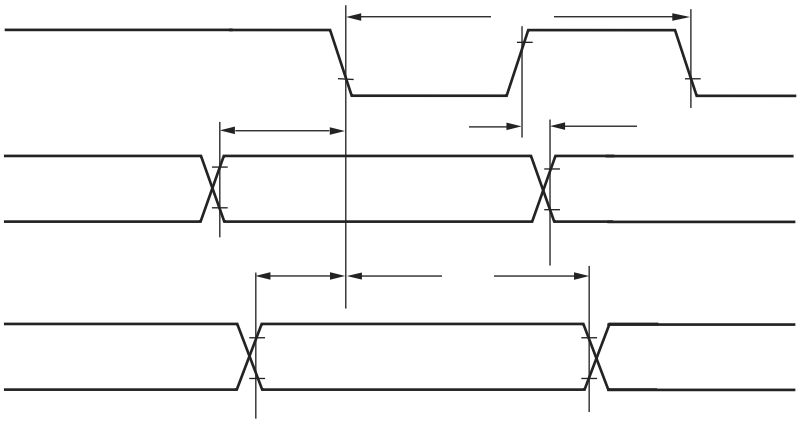
Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

• **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

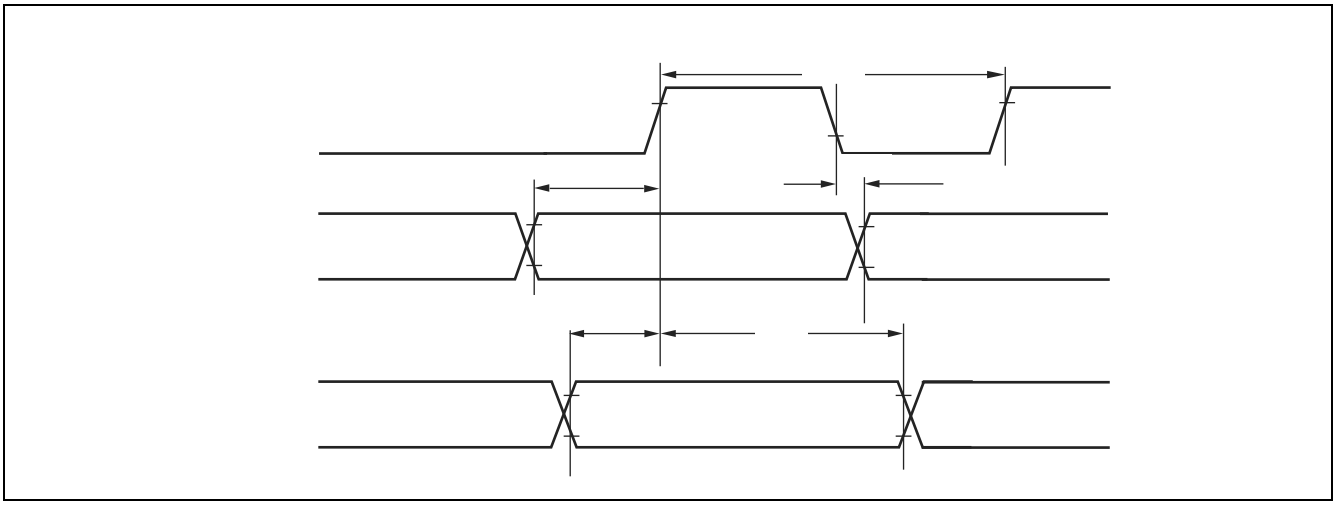


• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.



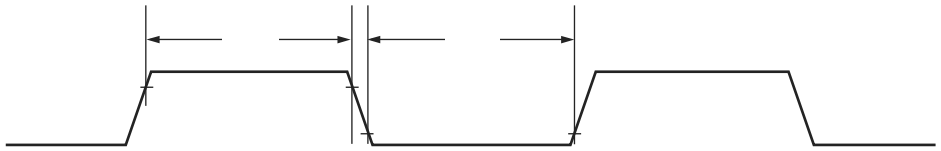
(6) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

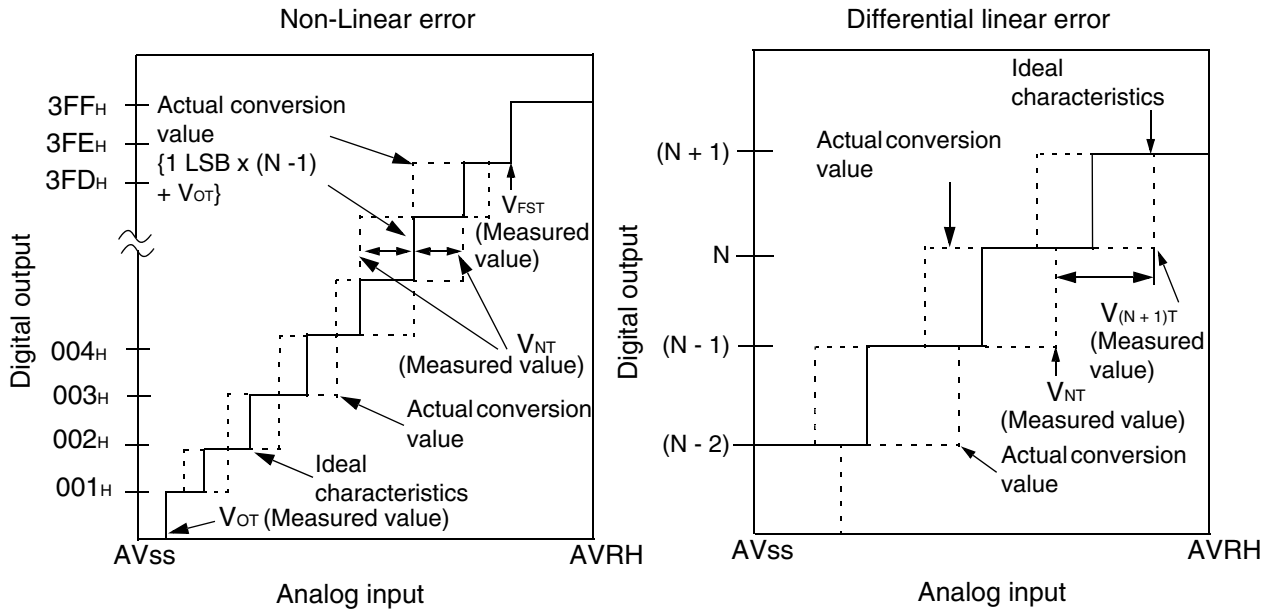
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Trigger input timing



(Continued)



$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

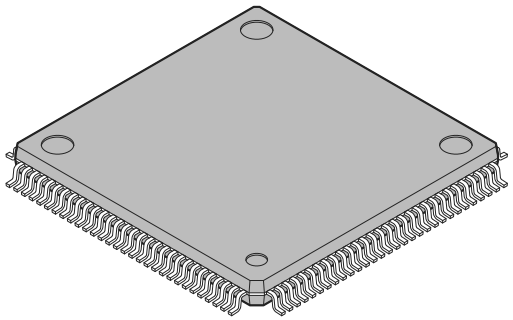
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

■ ORDERING INFORMATION

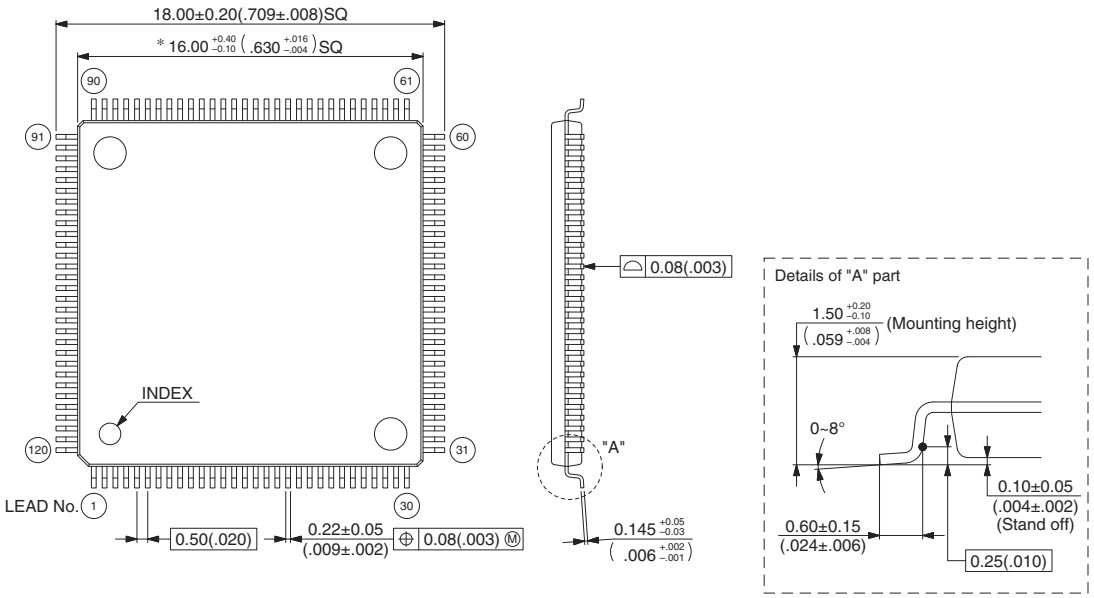
Part number	Package	Remarks
MB90F922NCPMC MB90F922NCSPMC MB90922NCSPMC MB90F923NCPMC MB90F923NCSPMC MB90F924NCPMC MB90F924NCSPMC	120-pin plastic LQFP (FPT-120P-M21)	
MB90V920-101CR MB90V920-102CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/