# Infineon Technologies - MB90922NCSPMC-GS-209E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

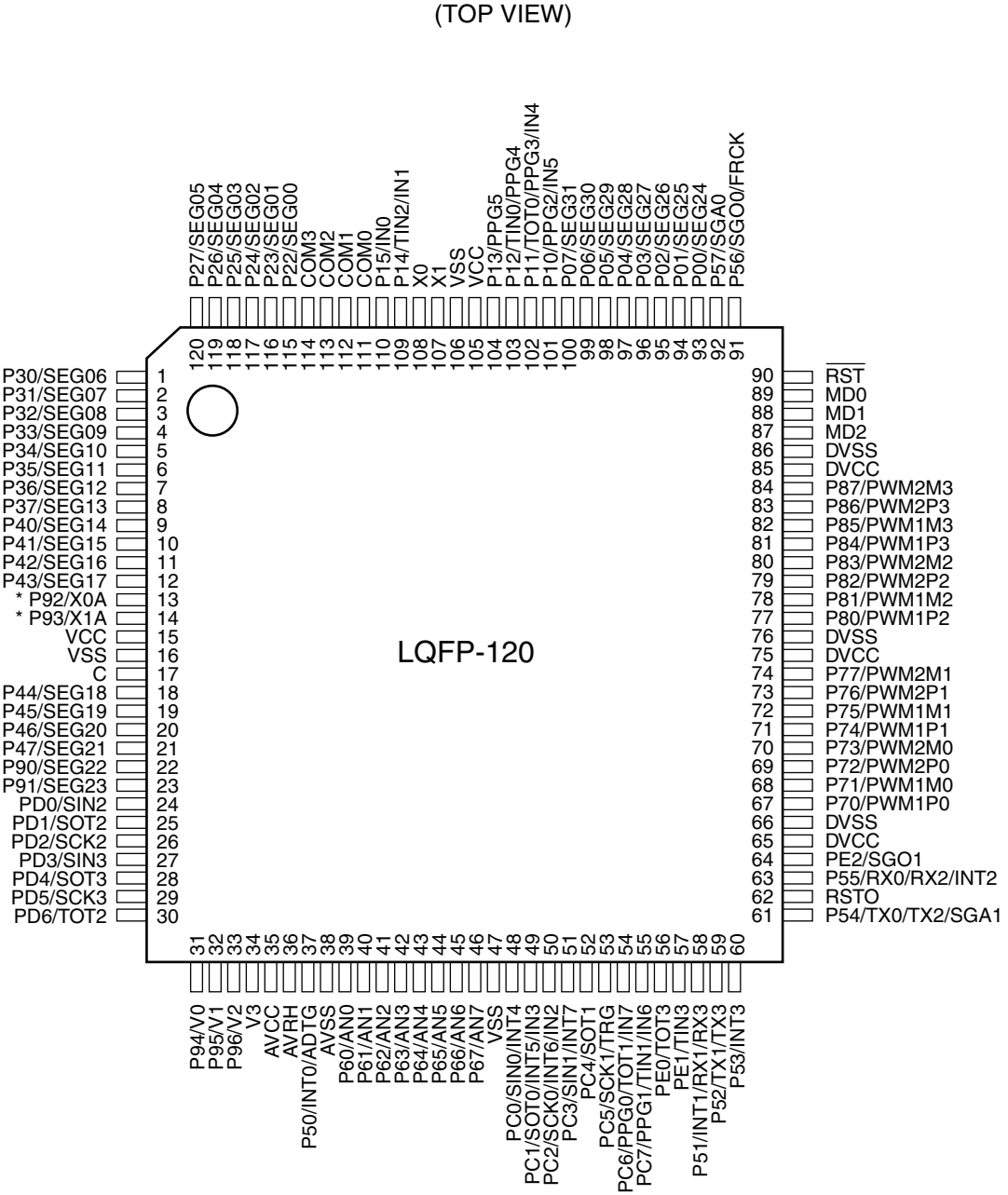
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 93 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-209e1 |

## ■ PRODUCT LINEUP

| Part number / Parameter | MB90 F922NC | MB90 F922NCS | MB90 F923NC | MB90 F923NCS | MB90 F924NC | MB90 F924NCS | MB90 922NCS | MB90 V920-101 | MB90 V920-102 |
|---|---|---|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | | MASK ROM product | Evaluation product | |
| CPU | $F^2MC$-16LX CPU | | | | | | | | |
| System clock | PLL clock multiplier circuit ( × 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped)<br>Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8) | | | | | | | | |
| Sub clock pins (X0A, X1A) | Yes | No | Yes | No | Yes | No | No | No | Yes |
| ROM | Flash memory 256 Kbytes | | Flash memory 384 Kbytes | | Flash memory 512 Kbytes | | 256 K bytes | External | |
| RAM | 10 Kbytes | | 16 Kbytes | | 24 Kbytes | | 10 K bytes | 30 Kbytes | |
| I/O port | 91 ports | 93 ports | 91 ports | 93 ports | 91 ports | 93 ports | 93 ports | 93 ports | 91 ports |
| LCD controller | 32 segment × 4 common | | | | | | | | |
| LIN-UART | UART (LIN/SCI) 4 channels | | | | | | | | |
| CAN interface | 4 channels | | | | | | | | |
| 16-bit input capture | 8 channels | | | | | | | | |
| 16-bit reload timer | 4 channels | | | | | | | | |
| 16-bit free-run timer | 1 channel | | | | | | | | |
| Real time watch timer | 1 channel | | | | | | | | |
| 16-bit PPG timer | 6 channels | | | | | | | | |
| External interrupt | 8 channels | | | | | | | | |
| 8/10-bit A/D converter | 8 channels | | | | | | | | |
| Low-voltage/ CPU operating detection reset | Yes | | | | | | | No | |
| Stepping motor controller | 4 channels | | | | | | | | |
| Sound generator | 2 channels | | | | | | | | |
| Flash memory security | Yes | | | | | | — | | |
| Operating voltage | 4.0 V to 5.5 V | | | | | | | 4.5 V to 5.5 V | |
| Package | LQFP-120 | | | | | | | PGA-299 | |

## ■ PIN ASSIGNMENT




(FPT-120P-M21)

* : MB90V920-101, MB90F922NCS,MB90F923NCS,MB90F924NCS,MB90922NCS : P92, P93
MB90V920-102, MB90F922NC,MB90F923NC,MB90F924NC : X0A, X1A

- **Handling the power supply for high-current output buffer pins** ($DV_{CC}$, $DV_{SS}$)

  - **Flash memory products and MASK ROM products (MB90F922NC/F922NCS/922NCS/F923NC/ F923NCS/F924NC/F924NCS)**

    In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is isolated from the digital power supply ($V_{CC}$).
    Therefore, DVcc can therefore be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is supplied before the digital power supply ($V_{CC}$), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply ($V_{CC}$) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$).

  - **Evaluation product** (**MB90V920-101**/**MB90V920-102**)

    In the evaluation products, the power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) is not isolated from the digital power supply ($V_{CC}$). Therefore, $DV_{CC}$ must therefore be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$) must always be applied after the digital power supply ($V_{CC}$) has been connected, and disconnected before the digital power supply (Vcc) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).
    Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins ($DV_{CC}$, $DV_{SS}$).

- **Pull-up/pull-down resistors**

MB90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

- **Precautions when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

- **Notes on operating when the external clock is stopped**

The MB90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

- **Flash memory security function**

A security bit is located within the Flash memory region. The security function is activated by writing the protection code $01_H$ to the security bit.
Do not write the value $01_H$ to this address if you are not using the security function.
Please refer to following table for the address of the security bit.

| | Flash memory size | Address for security bit |
|---|---|---|
| MB90F922NC<br>MB90F922NCS | Built-in 2 Mbits Flash Memory | $FC0001_H$ |
| MB90F923NCS | Built-in 3 Mbits Flash Memory | $F80001_H$ |
| MB90F924NCS | Built-in 4 Mbits Flash Memory | $F80001_H$ |

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000083H | (Disabled) | | | | |
| 000084H | PWM control register 2 | PWC2 | R/W | Stepping motor controller 2 | 000000X0B |
| 000085H | (Disabled) | | | | |
| 000086H | PWM control register 3 | PWC3 | R/W | Stepping motor controller 3 | 000000X0B |
| 000087H | (Disabled) | | | | |
| 000088H | LCD output control register 3 | LOCR3 | R/W | LCDC | XXXXX111B |
| 000089H | (Disabled) | | | | |
| 00008AH | A/D setting register 0 | ADSR0 | R/W | A/D converter | 00000000B |
| 00008BH | A/D setting register 1 | ADSR1 | R/W | | 00000000B |
| 00008CH | Port input level select 0 | PIL0 | R/W | Port input level select | 00000000B |
| 00008DH | Port input level select 1 | PIL1 | R/W | | XXXX0000B |
| 00008EH | Port input level select 2 | PIL2 | R/W | | XXXX0000B |
| 00008FH to 00009DH | (Disabled) | | | | |
| 00009EH | Program address detection control register | PACSR | R/W | Address match detection | XXXX0X0XB |
| 00009FH | Delayed Interrupt/Release Register | DIRR | R/W | Delay interrupt | XXXXXXX0B |
| 0000A0H | Power saving mode control register | LPMCR | R/W | Power saving control circuit | 00011000B |
| 0000A1H | Clock select register | CKSCR | R/W, R | | 11111100B |
| 0000A2H to 0000A7H | (Disabled) | | | | |
| 0000A8H | Watchdog timer control register | WDTC | R, W | Watchdog timer | XXXXX111B |
| 0000A9H | Time-base timer control register | TBTC | R/W, W | Time-base timer | 1XX00100B |
| 0000AAH | Watch timer control register | WTC | R/W, W, R | Watch timer (sub clock) | 10001000B |
| 0000ABH to 0000ADH | (Disabled) | | | | |
| 0000AEH | Flash memory control status register | FMCS | R/W | Flash interface | 000X0000B |
| 0000AFH | (Disabled) | | | | |

*(Continued)*

**List of Control Registers(2)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 000040H | 000070H | 0039C0H | 0039D0H | Message buffer valid register | BVALR | R/W | 00000000B |
| 000041H | 000071H | 0039C1H | 0039D1H | | | | 00000000B |
| 000042H | 000072H | 0039C2H | 0039D2H | Transmit request register | TREQR | R/W | 00000000B |
| 000043H | 000073H | 0039C3H | 0039D3H | | | | 00000000B |
| 000044H | 000074H | 0039C4H | 0039D4H | Transmit cancel register | TCANR | W | 00000000B |
| 000045H | 000075H | 0039C5H | 0039D5H | | | | 00000000B |
| 000046H | 000076H | 0039C6H | 0039D6H | Transmit complete register | TCR | R/W | 00000000B |
| 000047H | 000077H | 0039C7H | 0039D7H | | | | 00000000B |
| 000048H | 000078H | 0039C8H | 0039D8H | Receive complete register | RCR | R/W | 00000000B |
| 000049H | 000079H | 0039C9H | 0039D9H | | | | 00000000B |
| 00004AH | 00007AH | 0039CAH | 0039DAH | Remote request receive register | RRTRR | R/W | 00000000B |
| 00004BH | 00007BH | 0039CBH | 0039DBH | | | | 00000000B |
| 00004CH | 00007CH | 0039CCH | 0039DCH | Receive overrun register | ROVRR | R/W | 00000000B |
| 00004DH | 00007DH | 0039CDH | 0039DDH | | | | 00000000B |
| 00004EH | 00007EH | 0039CEH | 0039DEH | Receive interrupt enable register | RIER | R/W | 00000000B |
| 00004FH | 00007FH | 0039CFH | 0039DFH | | | | 00000000B |
| 003C08H | 003D08H | 003E08H | 003F08H | IDE register | IDER | R/W | XXXXXXXXB |
| 003C09H | 003D09H | 003E09H | 003F09H | | | | XXXXXXXXB |
| 003C0AH | 003D0AH | 003E0AH | 003F0AH | Transmit RTR register | TRTRR | R/W | 00000000B |
| 003C0BH | 003D0BH | 003E0BH | 003F0BH | | | | 00000000B |
| 003C0CH | 003D0CH | 003E0CH | 003F0CH | Remote frame receive wait register | RFWTR | R/W | XXXXXXXXB |
| 003C0DH | 003D0DH | 003E0DH | 003F0DH | | | | XXXXXXXXB |
| 003C0EH | 003D0EH | 003E0EH | 003F0EH | Transmit interrupt enable register | TIER | R/W | 00000000B |
| 003C0FH | 003D0FH | 003E0FH | 003F0FH | | | | 00000000B |
| 003C10H | 003D10H | 003E10H | 003F10H | Acceptance mask select register | AMSR | R/W | XXXXXXXXB |
| 003C11H | 003D11H | 003E11H | 003F11H | | | | XXXXXXXXB |
| 003C12H | 003D12H | 003E12H | 003F12H | | | | XXXXXXXXB |
| 003C13H | 003D13H | 003E13H | 003F13H | | | | XXXXXXXXB |
| 003C14H | 003D14H | 003E14H | 003F14H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXXB |
| 003C15H | 003D15H | 003E15H | 003F15H | | | | XXXXXXXXB |
| 003C16H | 003D16H | 003E16H | 003F16H | | | | XXXXX---B |
| 003C17H | 003D17H | 003E17H | 003F17H | | | | XXXXXXXXB |
| 003C18H | 003D18H | 003E18H | 003F18H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXXB |
| 003C19H | 003D19H | 003E19H | 003F19H | | | | XXXXXXXXB |
| 003C1AH | 003D1AH | 003E1AH | 003F1AH | | | | XXXXX---B |
| 003C1BH | 003D1BH | 003E1BH | 003F1BH | | | | XXXXXXXXB |

**List of Message Buffers (ID Registers)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A00H to 003A1FH | 003B00H to 003B1FH | 003700H to 00371FH | 003800H to 00381FH | General-purpose RAM | — | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A20H | 003B20H | 003720H | 003820H | ID register 0 | IDR0 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A21H | 003B21H | 003721H | 003821H | | | | |
| 003A22H | 003B22H | 003722H | 003822H | | | | XXXXX---B XXXXXXXXB |
| 003A23H | 003B23H | 003723H | 003823H | | | | |
| 003A24H | 003B24H | 003724H | 003824H | ID register 1 | IDR1 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A25H | 003B25H | 003725H | 003825H | | | | |
| 003A26H | 003B26H | 003726H | 003826H | | | | XXXXX---B XXXXXXXXB |
| 003A27H | 003B27H | 003727H | 003827H | | | | |
| 003A28H | 003B28H | 003728H | 003828H | ID register 2 | IDR2 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A29H | 003B29H | 003729H | 003829H | | | | |
| 003A2AH | 003B2AH | 00372AH | 00382AH | | | | XXXXX---B XXXXXXXXB |
| 003A2BH | 003B2BH | 00372BH | 00382BH | | | | |
| 003A2CH | 003B2CH | 00372CH | 00382CH | ID register 3 | IDR3 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A2DH | 003B2DH | 00372DH | 00382DH | | | | |
| 003A2EH | 003B2EH | 00372EH | 00382EH | | | | XXXXX---B XXXXXXXXB |
| 003A2FH | 003B2FH | 00372FH | 00382FH | | | | |
| 003A30H | 003B30H | 003730H | 003830H | ID register 4 | IDR4 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A31H | 003B31H | 003731H | 003831H | | | | |
| 003A32H | 003B32H | 003732H | 003832H | | | | XXXXX---B XXXXXXXXB |
| 003A33H | 003B33H | 003733H | 003833H | | | | |
| 003A34H | 003B34H | 003734H | 003834H | ID register 5 | IDR5 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A35H | 003B35H | 003735H | 003835H | | | | |
| 003A36H | 003B36H | 003736H | 003836H | | | | XXXXX---B XXXXXXXXB |
| 003A37H | 003B37H | 003737H | 003837H | | | | |
| 003A38H | 003B38H | 003738H | 003838H | ID register 6 | IDR6 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A39H | 003B39H | 003739H | 003839H | | | | |
| 003A3AH | 003B3AH | 00373AH | 00383AH | | | | XXXXX---B XXXXXXXXB |
| 003A3BH | 003B3BH | 00373BH | 00383BH | | | | |
| 003A3CH | 003B3CH | 00373CH | 00383CH | ID register 7 | IDR7 | R/W | XXXXXXXXB XXXXXXXXB |
| 003A3DH | 003B3DH | 00373DH | 00383DH | | | | |
| 003A3EH | 003B3EH | 00373EH | 00383EH | | | | XXXXX---B XXXXXXXXB |
| 003A3FH | 003B3FH | 00373FH | 00383FH | | | | |

*(Continued)*

*(Continued)*

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A40H | 003B40H | 003740H | 003840H | ID register 8 | IDR8 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A41H | 003B41H | 003741H | 003841H | | | | |
| 003A42H | 003B42H | 003742H | 003842H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A43H | 003B43H | 003743H | 003843H | | | | |
| 003A44H | 003B44H | 003744H | 003844H | ID register 9 | IDR9 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A45H | 003B45H | 003745H | 003845H | | | | |
| 003A46H | 003B46H | 003746H | 003846H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A47H | 003B47H | 003747H | 003847H | | | | |
| 003A48H | 003B48H | 003748H | 003848H | ID register 10 | IDR10 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A49H | 003B49H | 003749H | 003849H | | | | |
| 003A4AH | 003B4AH | 00374AH | 00384AH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A4BH | 003B4BH | 00374BH | 00384BH | | | | |
| 003A4CH | 003B4CH | 00374CH | 00384CH | ID register 11 | IDR11 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A4DH | 003B4DH | 00374DH | 00384DH | | | | |
| 003A4EH | 003B4EH | 00374EH | 00384EH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A4FH | 003B4FH | 00374FH | 00384FH | | | | |
| 003A50H | 003B50H | 003750H | 003850H | ID register 12 | IDR12 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A51H | 003B51H | 003751H | 003851H | | | | |
| 003A52H | 003B52H | 003752H | 003852H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A53H | 003B53H | 003753H | 003853H | | | | |
| 003A54H | 003B54H | 003754H | 003854H | ID register 13 | IDR13 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A55H | 003B55H | 003755H | 003855H | | | | |
| 003A56H | 003B56H | 003756H | 003856H | | | | XXXXX---B<br>XXXXXXXXB |
| 003A57H | 003B57H | 003757H | 003857H | | | | |
| 003A58H | 003B58H | 003758H | 003858H | ID register 14 | IDR14 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A59H | 003B59H | 003759H | 003859H | | | | |
| 003A5AH | 003B5AH | 00375AH | 00385AH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A5BH | 003B5BH | 00375BH | 00385BH | | | | |
| 003A5CH | 003B5CH | 00375CH | 00385CH | ID register 15 | IDR15 | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 003A5DH | 003B5DH | 00375DH | 00385DH | | | | |
| 003A5EH | 003B5EH | 00375EH | 00385EH | | | | XXXXX---B<br>XXXXXXXXB |
| 003A5FH | 003B5FH | 00375FH | 00385FH | | | | |

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} = V_{CC}$*2 |
| | AVRH | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq$ AVRH*2 |
| | $DV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $DV_{CC} = V_{CC}$*2 |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | |
| Maximum clamp current | $I_{CLAMP}$ | – 4 | + 4 | mA | *7 |
| Total maximum clamp current | $\Sigma \lvert I_{CLAMP} \rvert$ | — | 40 | mA | *7 |
| "L" level maximum output current*4 | $I_{OL1}$ | — | 15 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OL2}$ | — | 40 | mA | P70 to P77 and P80 to P87 |
| "L" level average output current*5 | $I_{OLAV1}$ | — | 4 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OLAV2}$ | — | 30 | mA | P70 to P77 and P80 to P87 |
| "L" level maximum total output current | $\Sigma I_{OL1}$ | — | 100 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OL2}$ | — | 330 | mA | P70 to P77 and P80 to P87 |
| "L" level average total output current | $\Sigma I_{OLAV1}$ | — | 50 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OLAV2}$ | — | 250 | mA | P70 to P77 and P80 to P87 |
| "H" level maximum output current | $I_{OH1}$*4 | — | –15 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OH2}$*4 | — | –40 | mA | P70 to P77 and P80 to P87 |
| "H" level average output current | $I_{OHAV1}$*5 | — | –4 | mA | Except P70 to P77 and P80 to P87 |
| | $I_{OHAV2}$*5 | — | –30 | mA | P70 to P77 and P80 to P87 |
| "H" level maximum total output current | $\Sigma I_{OH1}$ | — | –100 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OH2}$ | — | –330 | mA | P70 to P77 and P80 to P87 |
| "H" level average total output current | $\Sigma I_{OHAV1}$*6 | — | –50 | mA | Except P70 to P77 and P80 to P87 |
| | $\Sigma I_{OHAV2}$*6 | — | –250 | mA | P70 to P77 and P80 to P87 |
| Power consumption | $P_D$ | — | 625 | mW | |
| Operating temperature | $T_A$ | – 40 | + 105 | °C | |
| Storage temperature | $T_{STG}$ | – 55 | + 150 | °C | |

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : $AV_{CC}$, AVRH must not exceed $V_{CC}$, and AVRH must not exceed $AV_{CC}$.
When using an evaluation product, $DV_{CC}$ must not exceed $V_{CC}$ (however, $DV_{CC}$ can be set to a higher voltage than $V_{CC}$ when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, $I_{CLAMP}$ is the applicable rating instead of $V_I$.

*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

*(Continued)*

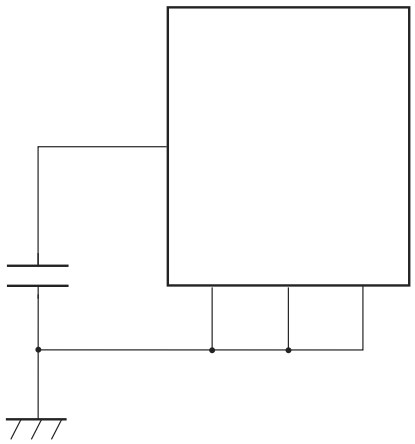
## 2. Recommended Operating Conditions

($V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ $AV_{CC}$ $DV_{CC}$ | 4.0 | 5.5 | V | The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| | | 4.4 | 5.5 | V | Maintain stop operation status<br>The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| Smoothing capacitor* | $C_S$ | 0.1 | 1.0 | µF | Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the $V_{CC}$ pin. |
| Operating temperature | $T_A$ | − 40 | + 105 | °C | |

* : Refer to the following diagram for details on the connection of the smoothing capacitor $C_S$.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

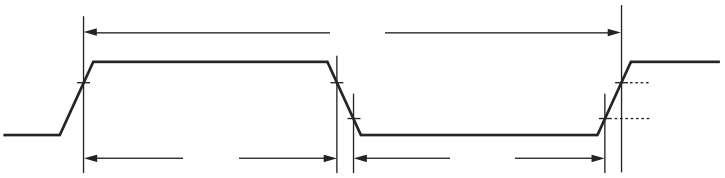
## 4. AC Characteristics

### (1) Clock timing

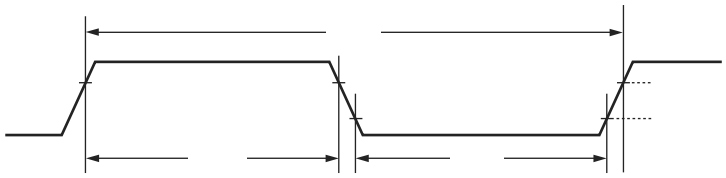
($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_C$ | X0, X1 | — | 3 | — | 16 | MHz | 1/2 (PLL stopped) When using the oscillator circuit |
| | | | | 3 | — | 32 | MHz | 1/2 (PLL stopped) When using an external clock |
| | | | | 4 | — | 32 | MHz | PLL multiplied by 1 |
| | | | | 3 | — | 16 | MHz | PLL multiplied by 2 |
| | | | | 3 | — | 10.7 | MHz | PLL multiplied by 3 |
| | | | | 3 | — | 8 | MHz | PLL multiplied by 4 |
| | | | | 3 | — | 5.33 | MHz | PLL multiplied by 6 |
| | | | | 3 | — | 4 | MHz | PLL multiplied by 8 |
| | $F_{LC}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | | 62.5 | — | 333 | ns | When using an oscillator |
| | | | | 31.25 | — | 333 | ns | External clock input |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | | 5 | — | — | ns | Use duty ratio of 50% ± 3% as a guideline |
| | $P_{WLH}$, $P_{WLL}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rise and fall time | tcr, tcf | X0 | | — | — | 5 | ns | When using an external clock signal |
| Internal operating clock frequency | $F_{CP}$ | — | | 1.5 | — | 32 | MHz | Using main clock (PLL clock) |
| | $F_{LCP}$ | — | | — | 8.192 | — | kHz | Using sub clock |
| Internal operating clock cycle time | $t_{CP}$ | — | | 31.25 | — | 666 | ns | Using main clock (PLL clock) |
| | $t_{LCP}$ | — | | — | 122.1 | — | µs | Using sub clock |

• X0, X1 clock timing

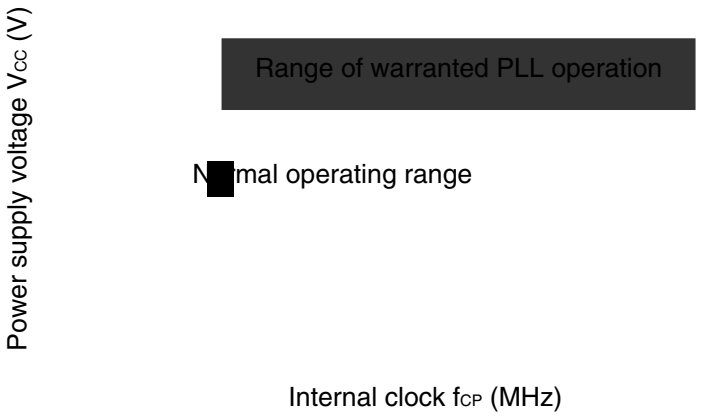


• X0A, X1A clock timing



• **Guaranteed PLL Operation Range**

Internal operating clock frequency vs. Power supply voltage

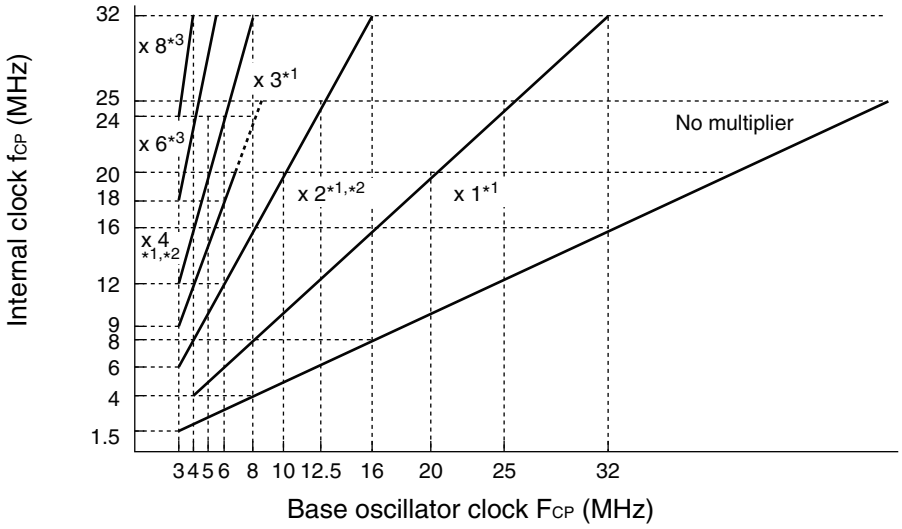



Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

*(Continued)*

*(Continued)*

Base oscillator frequency vs. Internal operating clock frequency




*1 : When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example] When using a base oscillator frequency of 24 MHz at PLL × 1 :
CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4,CS2 bit = "1"
[Example] When using a base oscillator frequency of 6 MHz at PLL × 3 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < $f_{CP}$ ≤ 32 MHz, the following settings are also supported.
PLL × 2 : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4 : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3 : When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example] When using a base oscillator frequency of 4 MHz at PLL × 6 :
CKSCR register : CS1 bit = "1", CS0 bit = "0"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"
[Example] When using a base oscillator frequency of 3 MHz at PLL × 8 :
CKSCR register : CS1 bit = "1", CS0 bit = "1"
PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

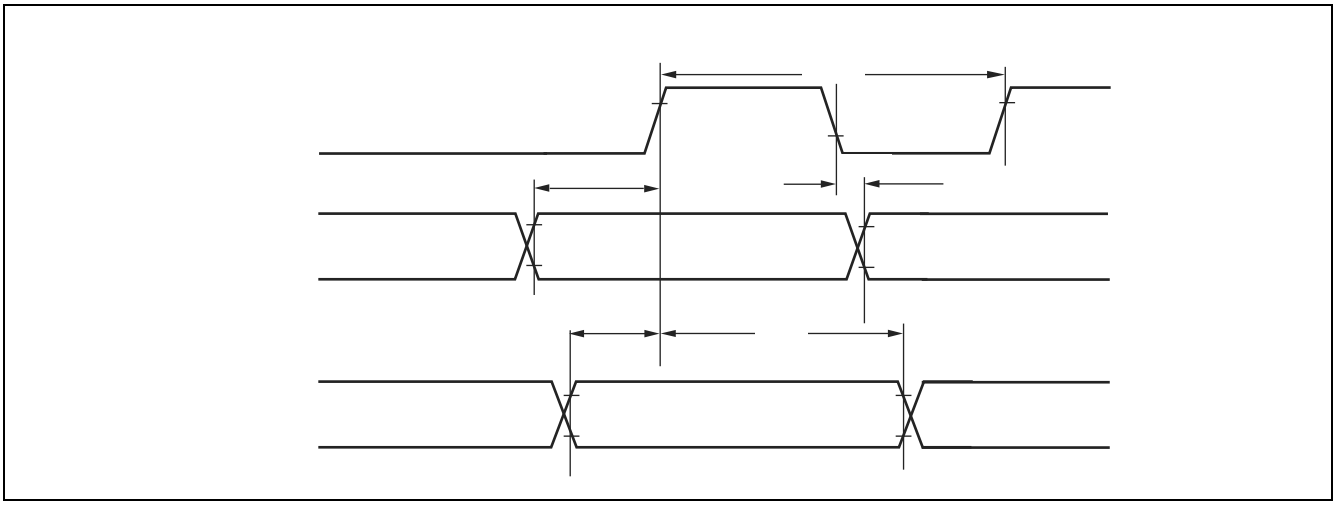
*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pin $C_L$ = 80 pF + 1TTL | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | – 50 | + 50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXI}$ | | | 0 | — | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
- $C_L$ is the load capacitance connected to the pin during testing.
- $t_{CP}$ is the internal operating clock cycle time. Refer to “ (1) Clock timing”.



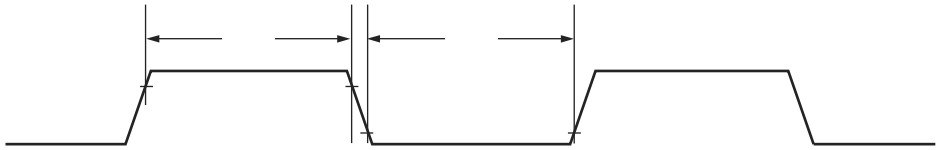
### (5) Timer input timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN0, TIN1,<br>IN0 to IN3 | — | 4 $t_{CP}$ | — | ns |

Note : $t_{CP}$ is the internal operating clock cycle time. Refer to " (1) Clock timing".

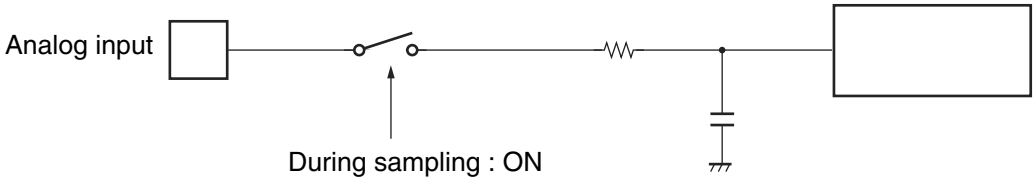
- Timer input timing



• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit




MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

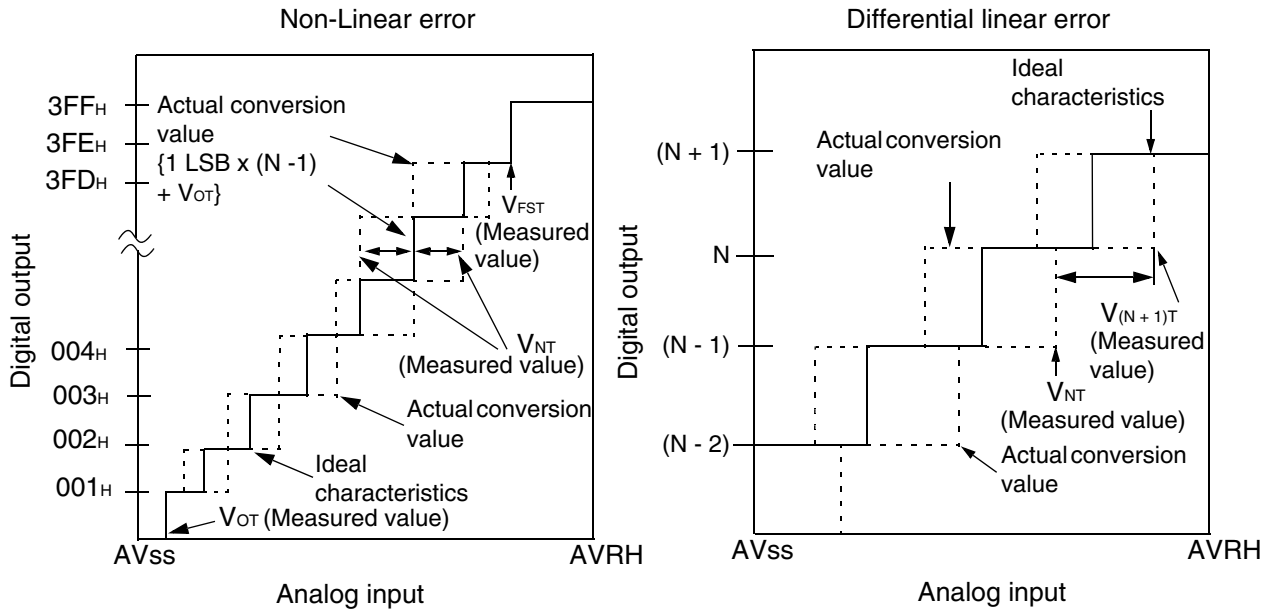
| | R | C |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.6 kΩ (Max) | 8.5 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 12.1 kΩ (Max) | 8.5 pF (Max) |

MB90V920-101/102

| | | |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.0 kΩ (Max) | 14.4 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 8.2 kΩ (Max) | 14.4 pF (Max) |

Note : The values are reference values.

*(Continued)*




$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

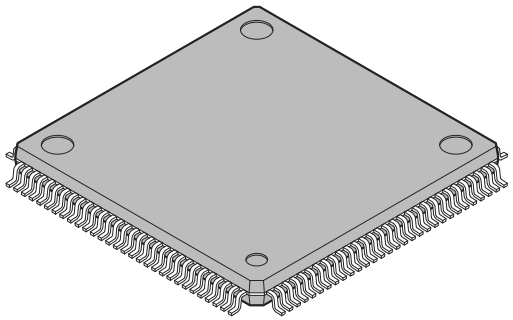
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
$V_{OT}$ : Voltage when digital output changes from $000_H$ to $001_H$
$V_{FST}$ : Voltage when digital output changes from $3FE_H$ to $3FF_H$

## ■ ORDERING INFORMATION

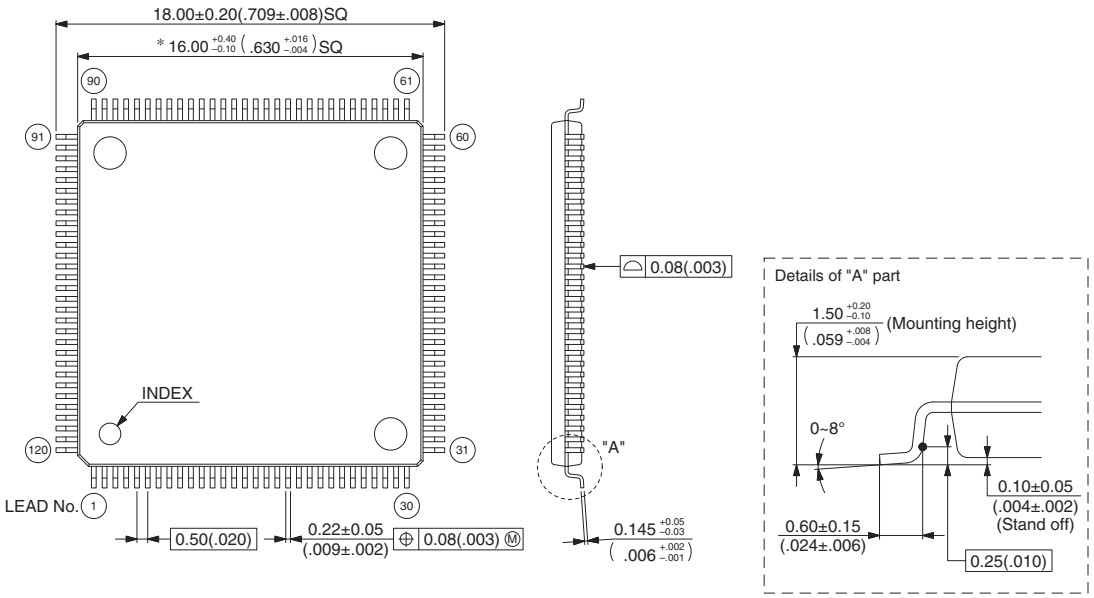
| Part number | Package | Remarks |
|---|---|---|
| MB90F922NCPMC<br>MB90F922NCSPMC<br>MB90922NCSPMC<br>MB90F923NCPMC<br>MB90F923NCSPMC<br>MB90F924NCPMC<br>MB90F924NCSPMC | 120-pin plastic LQFP<br>(FPT-120P-M21) | |
| MB90V920-101CR<br>MB90V920-102CR | 299-pin ceramic PGA<br>(PGA-299C-A01) | For evaluation |

## ■ PACKAGE DIMENSION

| 120-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 16.0 × 16.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.88 g |
| (FPT-120P-M21) | Code (Reference) | P-LFQFP120-16×16-0.50 |

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 12 | ■I/O CIRCUIT TYPE | Corrected the circuit type B. |
| 20 | ■ HANDLING DEVICES | Added the following items;<br>• Serial communication<br>• Characteristic difference between flash device and MASK ROM device |
| 31 | ■ I/O MAP | Corrected “Address: 003970$_H$”.<br>Clock supervisor control register → (Disabled) |
| 46 | ■ ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics | Added the item for “LCD output impedance”. |
| 68 | ■ ORDERING INFORMATION | Corrected the part numbers;<br>MB90V920-101 → MB90V920-101CR<br>MB90V920-102 → MB90V920-102CR |

The vertical lines marked in the left side of the page show the changes.