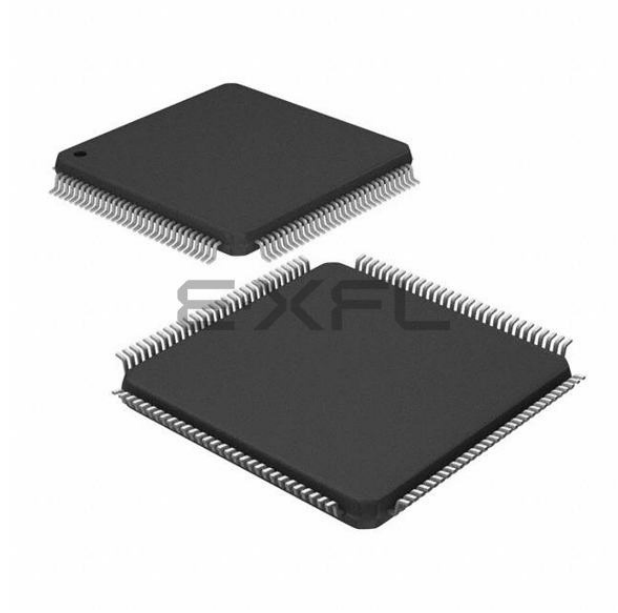
# Infineon Technologies - MB90922NCSPMC-GS-215E1 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 93 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-215e1 |

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 61 | P54 | I | General-purpose I/O port |
| | TX0 | | CAN interface 0 TX output pin |
| | TX2 | | CAN interface 2 TX output pin |
| | SGA1 | | Sound generator ch.1 SGA output pin |
| 63 | P55 | I | General-purpose I/O port |
| | RX0 | | CAN interface 0 RX input pin |
| | RX2 | | CAN interface 2 RX input pin |
| | INT2 | | INT2 external interrupt input pin |
| 91 | P56 | I | General-purpose I/O port |
| | SGO0 | | Sound generator ch.0 SGO output pin |
| | FRCK | | Free-run timer clock input pin |
| 92 | P57 | I | General-purpose I/O port |
| | SGA0 | | Sound generator ch.0 SGA output pin |
| 39 | P60 | H | General-purpose I/O port |
| | AN0 | | A/D converter input pin |
| 40 | P61 | H | General-purpose I/O port |
| | AN1 | | A/D converter input pin |
| 41 | P62 | H | General-purpose I/O port |
| | AN2 | | A/D converter input pin |
| 42 | P63 | H | General-purpose I/O port |
| | AN3 | | A/D converter input pin |
| 43 | P64 | H | General-purpose I/O port |
| | AN4 | | A/D converter input pin |
| 44 | P65 | H | General-purpose I/O port |
| | AN5 | | A/D converter input pin |
| 45 | P66 | H | General-purpose I/O port |
| | AN6 | | A/D converter input pin |
| 46 | P67 | H | General-purpose I/O port |
| | AN7 | | A/D converter input pin |
| 67 | P70 | L | General-purpose output-only port |
| | PWM1P0 | | Stepping motor controller ch.0 output pin |
| 68 | P71 | L | General-purpose output-only port |
| | PWM1M0 | | Stepping motor controller ch.0 output pin |
| 69 | P72 | L | General-purpose output-only port |
| | PWM2P0 | | Stepping motor controller ch.0 output pin |

*(Continued)*

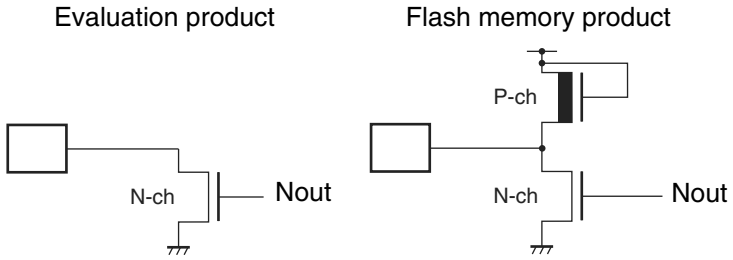
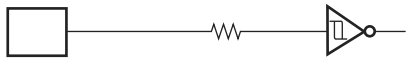
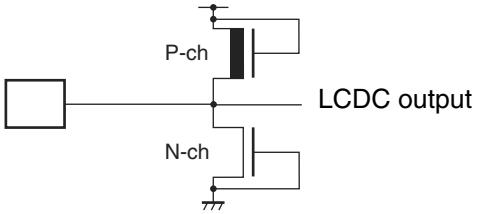
*(Continued)*

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 26 | PD2 | I | General-purpose I/O port |
| | SCK2 | | UART ch.2 serial clock I/O pin |
| 27 | PD3 | J | General-purpose I/O port |
| | SIN3 | | UART ch.3 serial data input pin |
| 28 | PD4 | I | General-purpose I/O port |
| | SOT3 | | UART ch.3 serial data output pin |
| 29 | PD5 | I | General-purpose I/O port |
| | SCK3 | | UART ch.3 serial clock I/O pin |
| 30 | PD6 | I | General-purpose I/O port |
| | TOT2 | | 16-bit reload timer ch.2 TOT output pin |
| 56 | PE0 | I | General-purpose I/O port |
| | TOT3 | | 16-bit reload timer ch.3 TOT output pin |
| 57 | PE1 | I | General-purpose I/O port |
| | TIN3 | | 16-bit reload timer ch.3 TIN input pin |
| 64 | PE2 | I | General-purpose I/O port |
| | SGO1 | | Sound generator ch.1 SGO output pin |
| 62 | RSTO | N | Internal reset signal output pin |
| 65, 75, 85 | DVCC | — | Power supply input pins dedicated for high current output buffer |
| 66, 76, 86 | DVSS | — | Power supply GND pins dedicated for high current output buffer |
| 35 | AVCC | — | A/D converter dedicated power supply input pin |
| 38 | AVSS | — | A/D converter dedicated power supply GND pin |
| 36 | AVRH | — | A/D converter Vref+ input pin. Vref- is fixed to AVSS. |
| 89 | MD0 | D | Mode setting input pin. Connect to VCC pin. |
| 88 | MD1 | D | Mode setting input pin. Connect to VCC pin. |
| 87 | MD2 | D/E*2 | Mode setting input pin. Connect to VSS pin. |
| 17 | C | — | External capacitor pin.<br>Connect a 0.1 μF capacitor between this pin and the VSS pin. |
| 15, 105 | VCC | — | Power supply input pins |
| 16, 47, 106 | VSS | — | GND power supply pins |

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| N |  | N-ch open-drain pin<br>$I_{OL}$ = 4 mA |
| O |  | Input-only pin<br>Automotive input<br>($V_{IH}/V_{IL}$ = 0.8 $V_{CC}$/0.5 $V_{CC}$) |
| P |  | LCDC output pin (COM pin) |

- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

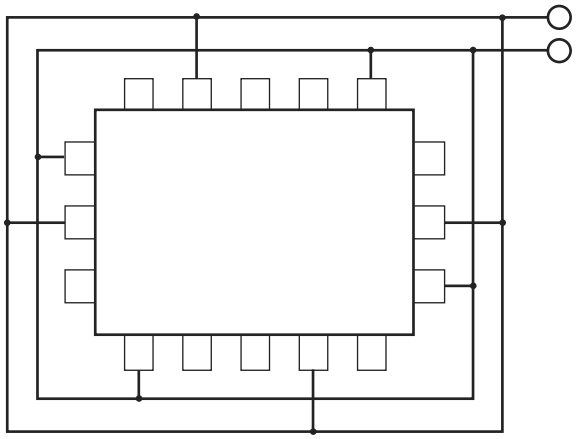
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply ($AV_{CC}$, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply ($V_{CC}$) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off ($V_{CC}$). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

- **Serial communication**

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000083H | (Disabled) | | | | |
| 000084H | PWM control register 2 | PWC2 | R/W | Stepping motor controller 2 | 000000X0B |
| 000085H | (Disabled) | | | | |
| 000086H | PWM control register 3 | PWC3 | R/W | Stepping motor controller 3 | 000000X0B |
| 000087H | (Disabled) | | | | |
| 000088H | LCD output control register 3 | LOCR3 | R/W | LCDC | XXXXX111B |
| 000089H | (Disabled) | | | | |
| 00008AH | A/D setting register 0 | ADSR0 | R/W | A/D converter | 00000000B |
| 00008BH | A/D setting register 1 | ADSR1 | R/W | | 00000000B |
| 00008CH | Port input level select 0 | PIL0 | R/W | Port input level select | 00000000B |
| 00008DH | Port input level select 1 | PIL1 | R/W | | XXXX0000B |
| 00008EH | Port input level select 2 | PIL2 | R/W | | XXXX0000B |
| 00008FH to 00009DH | (Disabled) | | | | |
| 00009EH | Program address detection control register | PACSR | R/W | Address match detection | XXXX0X0XB |
| 00009FH | Delayed Interrupt/Release Register | DIRR | R/W | Delay interrupt | XXXXXXX0B |
| 0000A0H | Power saving mode control register | LPMCR | R/W | Power saving control circuit | 00011000B |
| 0000A1H | Clock select register | CKSCR | R/W, R | | 11111100B |
| 0000A2H to 0000A7H | (Disabled) | | | | |
| 0000A8H | Watchdog timer control register | WDTC | R, W | Watchdog timer | XXXXX111B |
| 0000A9H | Time-base timer control register | TBTC | R/W, W | Time-base timer | 1XX00100B |
| 0000AAH | Watch timer control register | WTC | R/W, W, R | Watch timer (sub clock) | 10001000B |
| 0000ABH to 0000ADH | (Disabled) | | | | |
| 0000AEH | Flash memory control status register | FMCS | R/W | Flash interface | 000X0000B |
| 0000AFH | (Disabled) | | | | |

*(Continued)*

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---|---|---|---|---|---|
| 003944H | Input capture register 6 | IPCP6 | R | Input capture 6/7 | XXXXXXXXB |
| 003945H | | | | | XXXXXXXXB |
| 003946H | Input capture register 7 | IPCP7 | R | | XXXXXXXXB |
| 003947H | | | | | XXXXXXXXB |
| 003948H to 00394FH | (Disabled) | | | | |
| 003950H | Minute data register 2/Reload register 2 | TMR2/ TMRLR2 | R/W | 16-bit reload timer 2 | XXXXXXXXB |
| 003951H | | | | | XXXXXXXXB |
| 003952H | Minute data register 3/Reload register 3 | TMR3/ TMRLR3 | R/W | 16-bit reload timer 3 | XXXXXXXXB |
| 003953H | | | | | XXXXXXXXB |
| 003954H to 003957H | (Disabled) | | | | |
| 003958H | Sub second data register | WTBR | R/W | Real time watch timer | XXXXXXXXB |
| 003959H | | | | | XXXXXXXXB |
| 00395AH | | | | | XXXXXXXXB |
| 00395BH | Second data register | WTSR | R/W | | XX000000B |
| 00395CH | Minute data register | WTMR | R/W | | XX000000B |
| 00395DH | Hour data register | WTHR | R/W | | XXX00000B |
| 00395EH | Day data register | WTDR | R/W | | 00X00001B |
| 00395FH | (Disabled) | | | | |
| 003960H | LCD display RAM | VRAM | R/W | LCD controller/ driver | XXXXXXXXB |
| 003961H | | | | | XXXXXXXXB |
| 003962H | | | | | XXXXXXXXB |
| 003963H | | | | | XXXXXXXXB |
| 003964H | | | | | XXXXXXXXB |
| 003965H | | | | | XXXXXXXXB |
| 003966H | | | | | XXXXXXXXB |
| 003967H | | | | | XXXXXXXXB |
| 003968H | | | | | XXXXXXXXB |
| 003969H | | | | | XXXXXXXXB |
| 00396AH | | | | | XXXXXXXXB |
| 00396BH | | | | | XXXXXXXXB |
| 00396CH | | | | | XXXXXXXXB |
| 00396DH | | | | | XXXXXXXXB |
| 00396EH | | | | | XXXXXXXXB |
| 00396FH | | | | | XXXXXXXXB |

*(Continued)*

**List of Control Registers(2)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 000040H | 000070H | 0039C0H | 0039D0H | Message buffer valid register | BVALR | R/W | 00000000B |
| 000041H | 000071H | 0039C1H | 0039D1H | | | | 00000000B |
| 000042H | 000072H | 0039C2H | 0039D2H | Transmit request register | TREQR | R/W | 00000000B |
| 000043H | 000073H | 0039C3H | 0039D3H | | | | 00000000B |
| 000044H | 000074H | 0039C4H | 0039D4H | Transmit cancel register | TCANR | W | 00000000B |
| 000045H | 000075H | 0039C5H | 0039D5H | | | | 00000000B |
| 000046H | 000076H | 0039C6H | 0039D6H | Transmit complete register | TCR | R/W | 00000000B |
| 000047H | 000077H | 0039C7H | 0039D7H | | | | 00000000B |
| 000048H | 000078H | 0039C8H | 0039D8H | Receive complete register | RCR | R/W | 00000000B |
| 000049H | 000079H | 0039C9H | 0039D9H | | | | 00000000B |
| 00004AH | 00007AH | 0039CAH | 0039DAH | Remote request receive register | RRTRR | R/W | 00000000B |
| 00004BH | 00007BH | 0039CBH | 0039DBH | | | | 00000000B |
| 00004CH | 00007CH | 0039CCH | 0039DCH | Receive overrun register | ROVRR | R/W | 00000000B |
| 00004DH | 00007DH | 0039CDH | 0039DDH | | | | 00000000B |
| 00004EH | 00007EH | 0039CEH | 0039DEH | Receive interrupt enable register | RIER | R/W | 00000000B |
| 00004FH | 00007FH | 0039CFH | 0039DFH | | | | 00000000B |
| 003C08H | 003D08H | 003E08H | 003F08H | IDE register | IDER | R/W | XXXXXXXXB |
| 003C09H | 003D09H | 003E09H | 003F09H | | | | XXXXXXXXB |
| 003C0AH | 003D0AH | 003E0AH | 003F0AH | Transmit RTR register | TRTRR | R/W | 00000000B |
| 003C0BH | 003D0BH | 003E0BH | 003F0BH | | | | 00000000B |
| 003C0CH | 003D0CH | 003E0CH | 003F0CH | Remote frame receive wait register | RFWTR | R/W | XXXXXXXXB |
| 003C0DH | 003D0DH | 003E0DH | 003F0DH | | | | XXXXXXXXB |
| 003C0EH | 003D0EH | 003E0EH | 003F0EH | Transmit interrupt enable register | TIER | R/W | 00000000B |
| 003C0FH | 003D0FH | 003E0FH | 003F0FH | | | | 00000000B |
| 003C10H | 003D10H | 003E10H | 003F10H | Acceptance mask select register | AMSR | R/W | XXXXXXXXB |
| 003C11H | 003D11H | 003E11H | 003F11H | | | | XXXXXXXXB |
| 003C12H | 003D12H | 003E12H | 003F12H | | | | XXXXXXXXB |
| 003C13H | 003D13H | 003E13H | 003F13H | | | | XXXXXXXXB |
| 003C14H | 003D14H | 003E14H | 003F14H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXXB |
| 003C15H | 003D15H | 003E15H | 003F15H | | | | XXXXXXXXB |
| 003C16H | 003D16H | 003E16H | 003F16H | | | | XXXXX---B |
| 003C17H | 003D17H | 003E17H | 003F17H | | | | XXXXXXXXB |
| 003C18H | 003D18H | 003E18H | 003F18H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXXB |
| 003C19H | 003D19H | 003E19H | 003F19H | | | | XXXXXXXXB |
| 003C1AH | 003D1AH | 003E1AH | 003F1AH | | | | XXXXX---B |
| 003C1BH | 003D1BH | 003E1BH | 003F1BH | | | | XXXXXXXXB |

**List of Message Buffers (Data register)**

| Address | | | | Register | Abbre-viation | Access | Initial Value |
|---|---|---|---|---|---|---|---|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A80H to 003A87H | 003B80H to 003B87H | 003780H to 003787H | 003880H to 003887H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A88H to 003A8FH | 003B88H to 003B8FH | 003788H to 00378FH | 003888H to 00388FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A90H to 003A97H | 003B90H to 003B97H | 003790H to 003797H | 003890H to 003897H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003A98H to 003A9FH | 003B98H to 003B9FH | 003798H to 00379FH | 003898H to 00389FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AA0H to 003AA7H | 003BA0H to 003BA7H | 0037A0H to 0037A7H | 0038A0H to 0038A7H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AA8H to 003AAFH | 003BA8H to 003BAFH | 0037A8H to 0037AFH | 0038A8H to 0038AFH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AB0H to 003AB7H | 003BB0H to 003BB7H | 0037B0H to 0037B7H | 0038B0H to 0038B7H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AB8H to 003ABFH | 003BB8H to 003BBFH | 0037B8H to 0037BFH | 0038B8H to 0038BFH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AC0H to 003AC7H | 003BC0H to 003BC7H | 0037C0H to 0037C7H | 0038C0H to 0038C7H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AC8H to 003ACFH | 003BC8H to 003BCFH | 0037C8H to 0037CFH | 0038C8H to 0038CFH | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AD0H to 003AD7H | 003BD0H to 003BD7H | 0037D0H to 0037D7H | 0038D0H to 0038D7H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AD8H to 003ADFH | 003BD8H to 003BDFH | 0037D8H to 0037DFH | 0038D8H to 0038DFH | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AE0H to 003AE7H | 003BE0H to 003BE7H | 0037E0H to 0037E7H | 0038E0H to 0038E7H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AE8H to 003AEFH | 003BE8H to 003BEFH | 0037E8H to 0037EFH | 0038E8H to 0038EFH | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AF0H to 003AF7H | 003BF0H to 003BF7H | 0037F0H to 0037F7H | 0038F0H to 0038F7H | Data register 14 (8 bytes) | DTR14 | R/W | XXXXXXXXB to XXXXXXXXB |
| 003AF8H to 003AFFH | 003BF8H to 003BFFH | 0037F8H to 0037FFH | 0038F8H to 0038FFH | Data register 15 (8 bytes) | DTR15 | R/W | XXXXXXXXB to XXXXXXXXB |

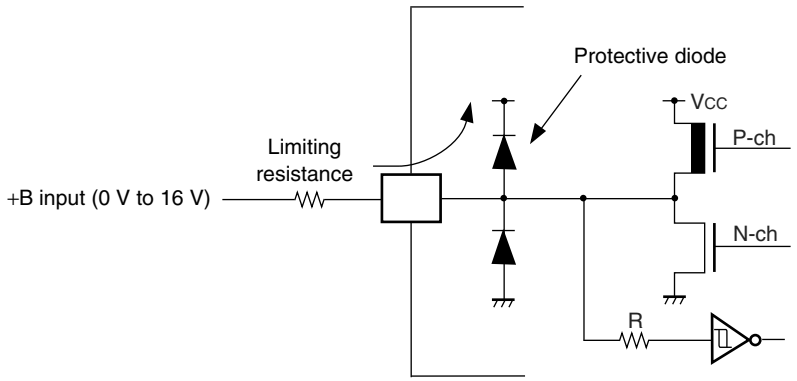
*(Continued)*

*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

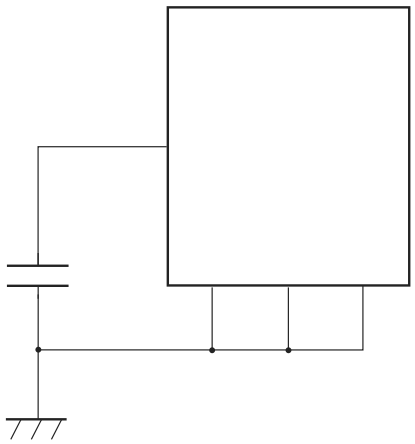
## 2. Recommended Operating Conditions

($V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ $AV_{CC}$ $DV_{CC}$ | 4.0 | 5.5 | V | The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| | | 4.4 | 5.5 | V | Maintain stop operation status<br>The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V. |
| Smoothing capacitor* | $C_S$ | 0.1 | 1.0 | µF | Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the $V_{CC}$ pin. |
| Operating temperature | $T_A$ | − 40 | + 105 | °C | |

* : Refer to the following diagram for details on the connection of the smoothing capacitor $C_S$.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 4. AC Characteristics

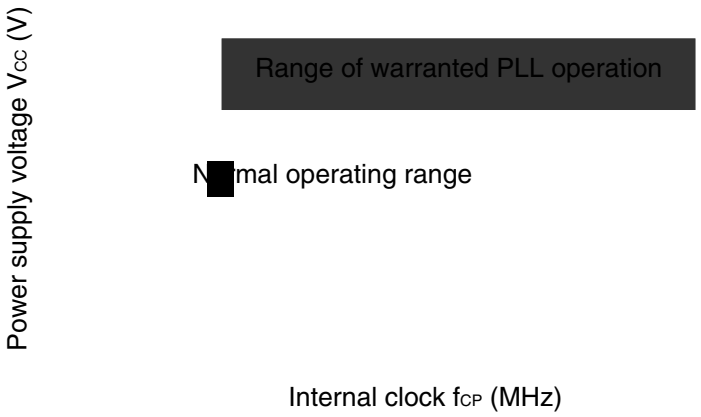
### (1) Clock timing

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $DV_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_C$ | X0, X1 | — | 3 | — | 16 | MHz | 1/2 (PLL stopped) When using the oscillator circuit |
| | | | | 3 | — | 32 | MHz | 1/2 (PLL stopped) When using an external clock |
| | | | | 4 | — | 32 | MHz | PLL multiplied by 1 |
| | | | | 3 | — | 16 | MHz | PLL multiplied by 2 |
| | | | | 3 | — | 10.7 | MHz | PLL multiplied by 3 |
| | | | | 3 | — | 8 | MHz | PLL multiplied by 4 |
| | | | | 3 | — | 5.33 | MHz | PLL multiplied by 6 |
| | | | | 3 | — | 4 | MHz | PLL multiplied by 8 |
| | $F_{LC}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | | 62.5 | — | 333 | ns | When using an oscillator |
| | | | | 31.25 | — | 333 | ns | External clock input |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | | 5 | — | — | ns | Use duty ratio of 50% ± 3% as a guideline |
| | $P_{WLH}$, $P_{WLL}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rise and fall time | tcr, tcf | X0 | | — | — | 5 | ns | When using an external clock signal |
| Internal operating clock frequency | $F_{CP}$ | — | | 1.5 | — | 32 | MHz | Using main clock (PLL clock) |
| | $F_{LCP}$ | — | | — | 8.192 | — | kHz | Using sub clock |
| Internal operating clock cycle time | $t_{CP}$ | — | | 31.25 | — | 666 | ns | Using main clock (PLL clock) |
| | $t_{LCP}$ | — | | — | 122.1 | — | µs | Using sub clock |

• **Guaranteed PLL Operation Range**

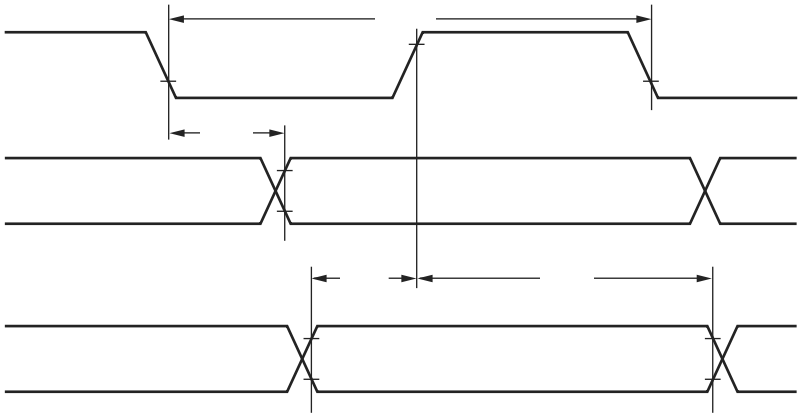
Internal operating clock frequency vs. Power supply voltage



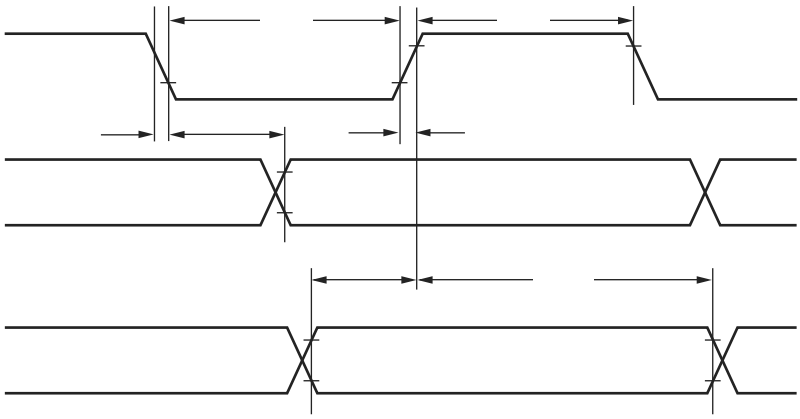

Notes : • For PLL 1 × only, use with tcp = 4 MHz or greater.
• Refer to “5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.

*(Continued)*

- Internal shift clock mode



- External shift clock mode



## 5. A/D Converter

### (1) Electrical Characteristics

($V_{CC}$ = $AV_{CC}$ = AVRH = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | – 3.0 | — | + 3.0 | LSB | |
| Non-linear error | — | — | – 2.5 | — | + 2.5 | LSB | |
| Differential linear error | — | — | – 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | V | 1 LSB = (AVRH – $AV_{SS}$) / 1024 |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH – 3.5 LSB | AVRH – 1.5 LSB | AVRH + 0.5 LSB | V | |
| Sampling time | $t_{SMP}$ | — | 0.4 | — | 16500 | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 1.0 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| Compare time | $t_{CMP}$ | — | 0.66 | — | — | µs | 4.5 V ≤ AVcc ≤ 5.5 V |
| | | | 2.2 | | | | 4.0 V ≤ AVcc ≤ 4.5 V |
| A/D conversion time | $t_{CNV}$ | — | 1.44 | — | — | µs | *1 |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | – 0.3 | — | + 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | 0 | — | AVRH | V | |
| Reference voltage | AV+ | AVRH | AVss + 2.7 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 2.3 | 6.0 | mA | |
| | $I_{AH}$ | | — | — | 5 | µA | *2 |
| Reference voltage supply current | $I_R$ | AVRH | — | 520 | 900 | µA | $V_{AVRH}$ = 5.0 V |
| | $I_{RH}$ | | — | — | 5 | µA | *2 |
| Inter-channel variation | — | AN0 to AN7 | — | — | 4 | LSB | |

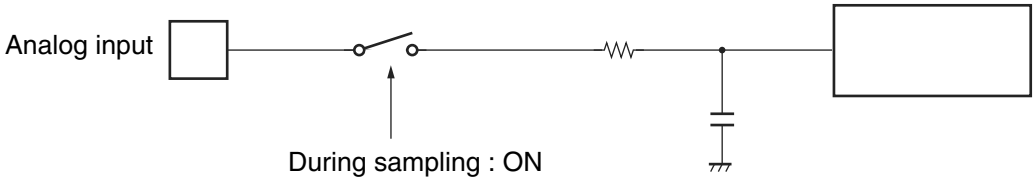
*1 : The time per channel (4.5 V ≤ $AV_{CC}$ ≤ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when $V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit




MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

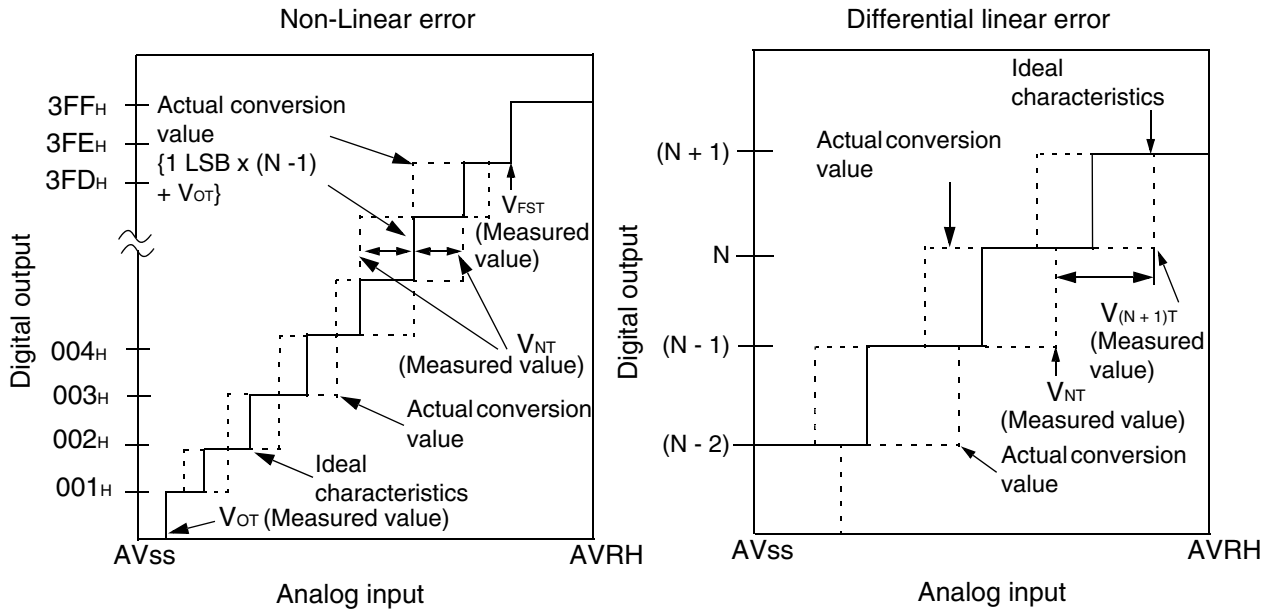
| | R | C |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.6 kΩ (Max) | 8.5 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 12.1 kΩ (Max) | 8.5 pF (Max) |

MB90V920-101/102

| | | |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V : | 2.0 kΩ (Max) | 14.4 pF (Max) |
| 4.0 V ≤ AVcc ≤ 4.5 V : | 8.2 kΩ (Max) | 14.4 pF (Max) |

Note : The values are reference values.

*(Continued)*




$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
$V_{OT}$ : Voltage when digital output changes from $000_H$ to $001_H$
$V_{FST}$ : Voltage when digital output changes from $3FE_H$ to $3FF_H$

## 6. Flash Memory Program/Erase Characteristics

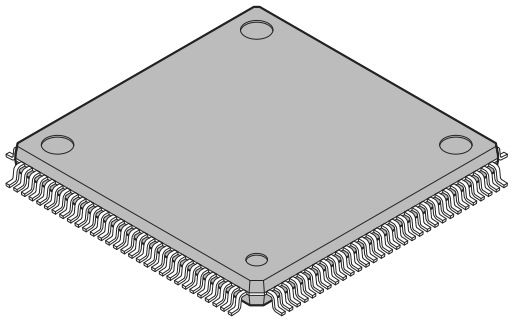
| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | — | 0.9 | 3.6 | s | Excludes pre-programming before erase |
| Word (16-bit width) programming time | | — | 23 | 370 | µs | Excludes system-level overhead |
| Chip programming time | $T_A$ = + 25 °C,<br>$V_{CC}$ = 5.0 V | — | 3.4 | 55 | s | |
| Erase/program cycle | — | 10000 | — | — | cycle | |
| Flash memory data retention time | Average<br>$T_A$ = + 85 °C | 20 | — | — | year | * |

* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

## ■ ORDERING INFORMATION

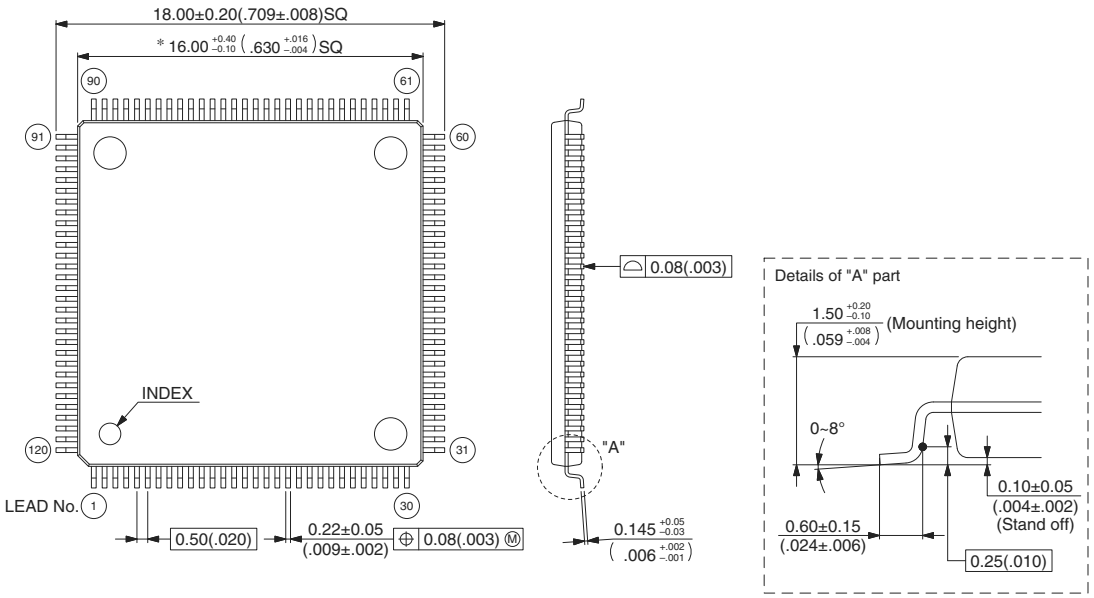
| Part number | Package | Remarks |
|---|---|---|
| MB90F922NCPMC<br>MB90F922NCSPMC<br>MB90922NCSPMC<br>MB90F923NCPMC<br>MB90F923NCSPMC<br>MB90F924NCPMC<br>MB90F924NCSPMC | 120-pin plastic LQFP<br>(FPT-120P-M21) | |
| MB90V920-101CR<br>MB90V920-102CR | 299-pin ceramic PGA<br>(PGA-299C-A01) | For evaluation |

## ■ PACKAGE DIMENSION

| 120-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 16.0 × 16.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.88 g |
| (FPT-120P-M21) | Code (Reference) | P-LFQFP120-16×16-0.50 |

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/