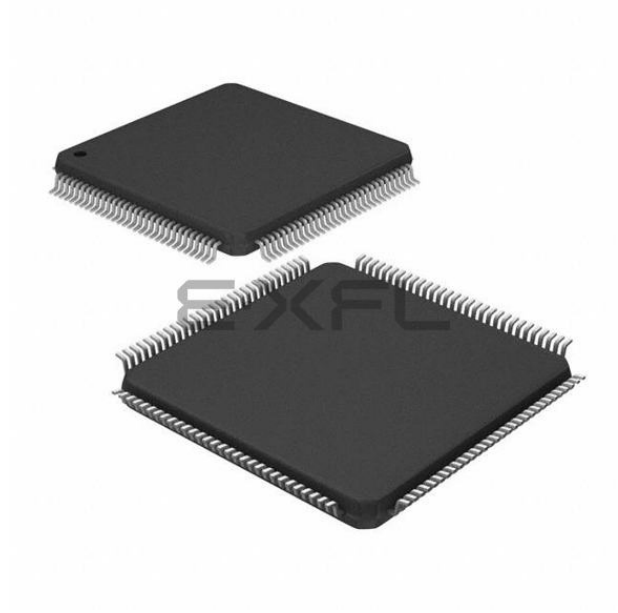
Infineon Technologies - MB90922NCSPMC-GS-217E1 Datasheet



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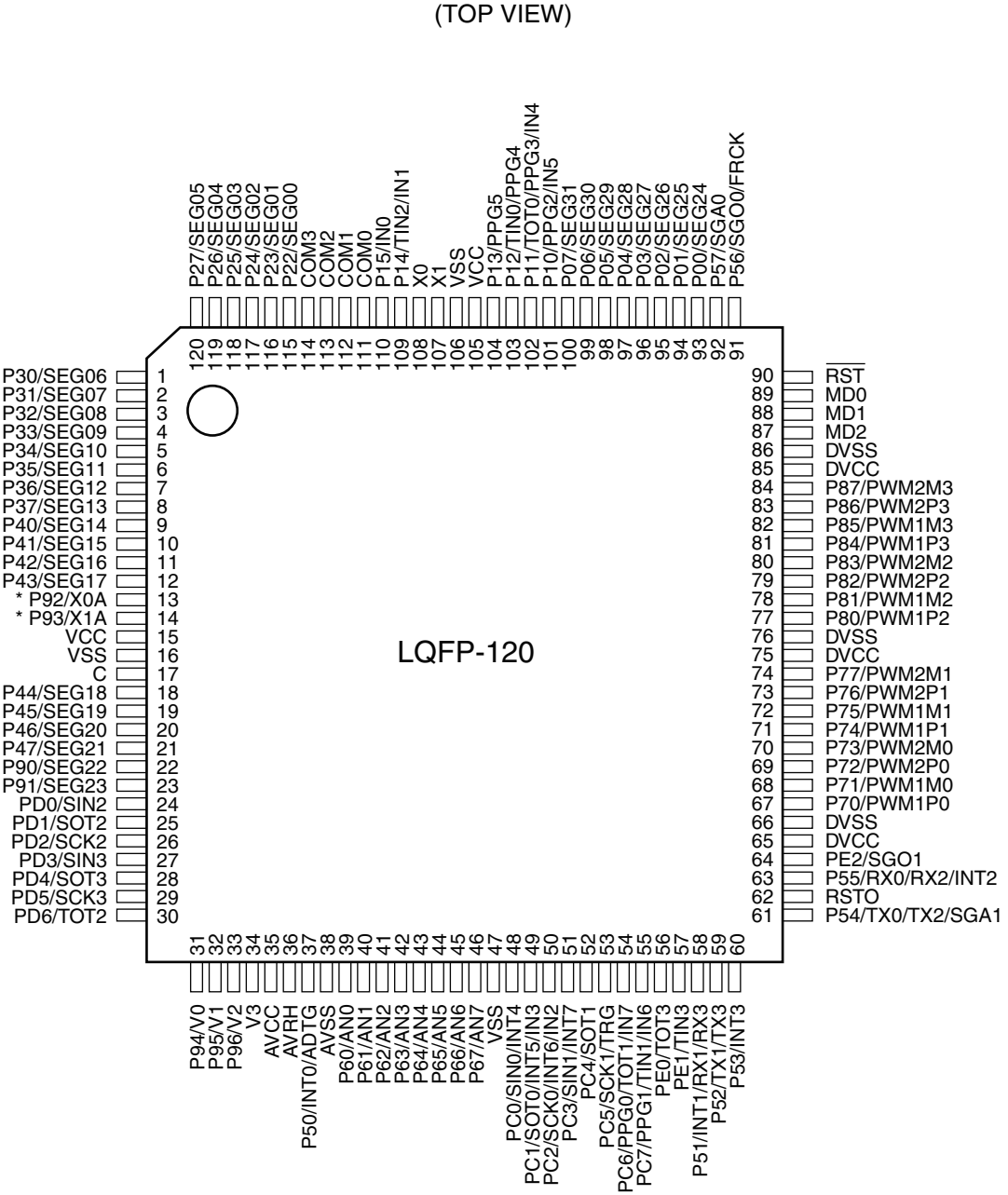
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-217e1

■ PIN ASSIGNMENT



(FPT-120P-M21)

* : MB90V920-101, MB90F922NCS,MB90F923NCS,MB90F924NCS,MB90922NCS : P92, P93
MB90V920-102, MB90F922NC,MB90F923NC,MB90F924NC : X0A, X1A

Pin no.	Pin name	I/O circuit type*1	Function
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin
52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin

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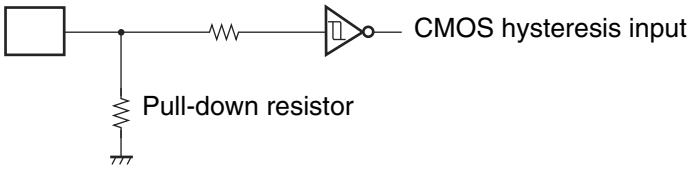
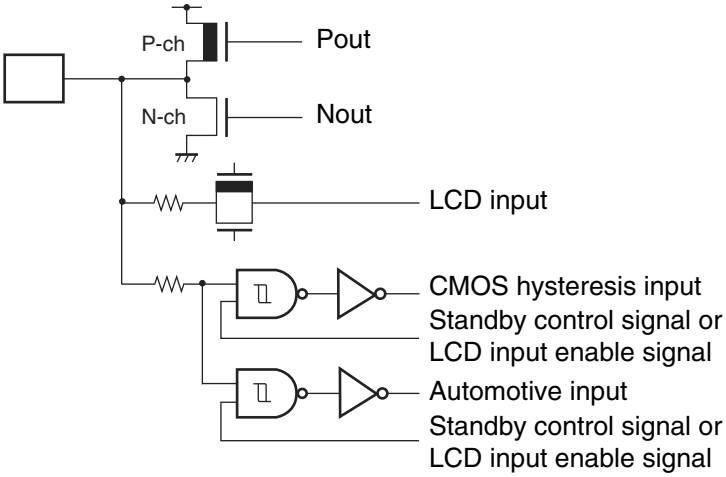
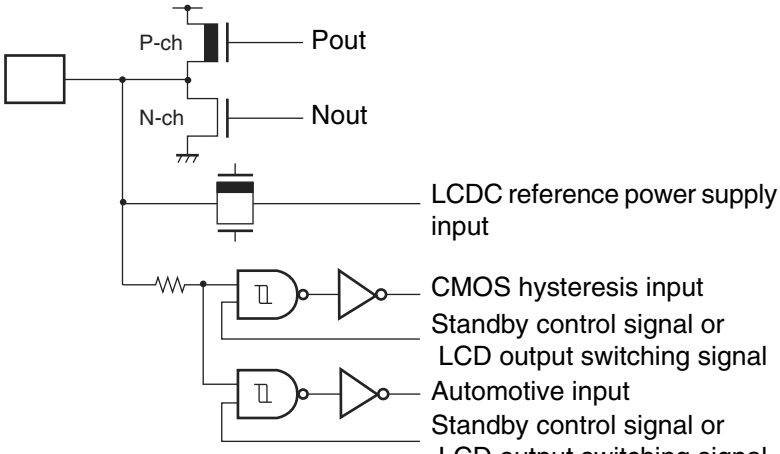
Type	Circuit	Remarks
E		Input-only pin (with pull-down resistance) • Attached pull-down resistance: approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.
F		LCD output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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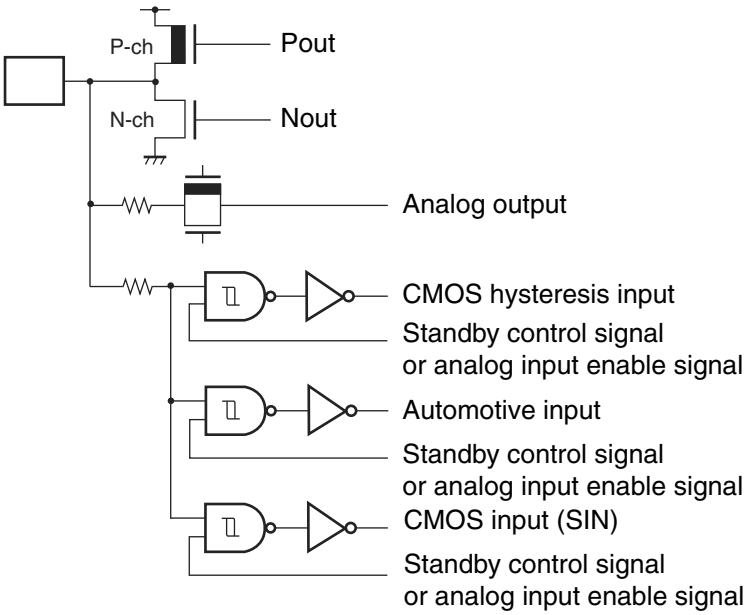
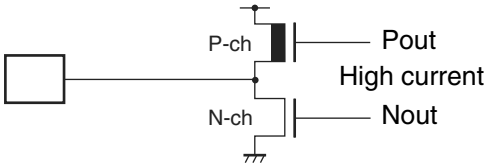
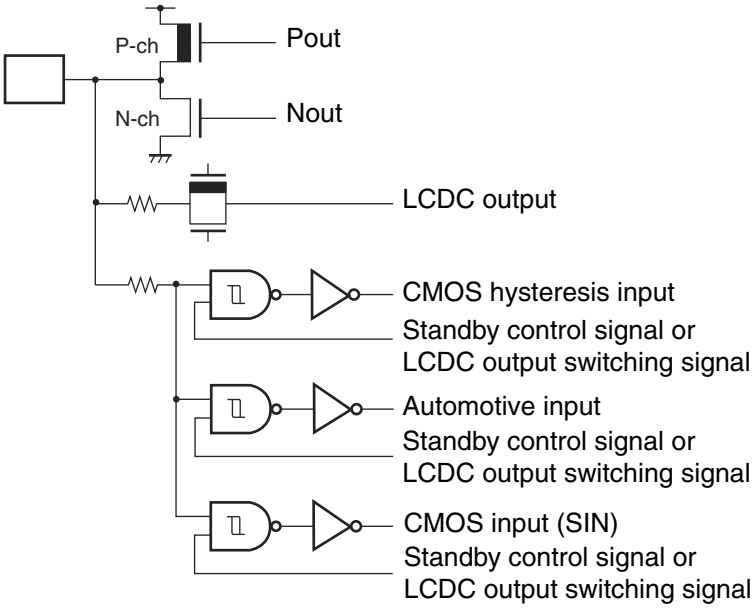
Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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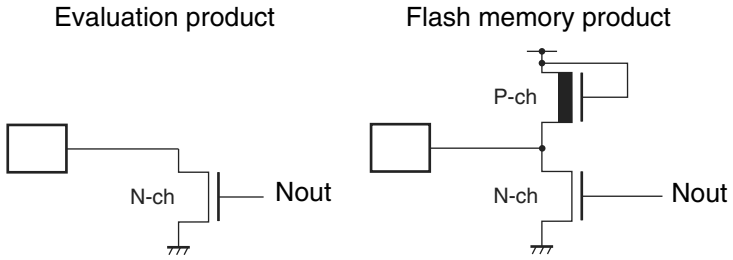
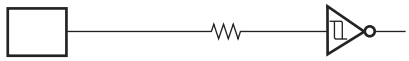
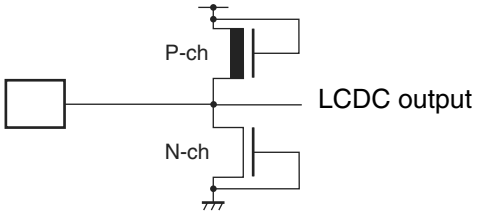
Type	Circuit	Remarks
N		N-ch open-drain pin I_{OL} = 4 mA
O		Input-only pin Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
P		LCDC output pin (COM pin)

- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

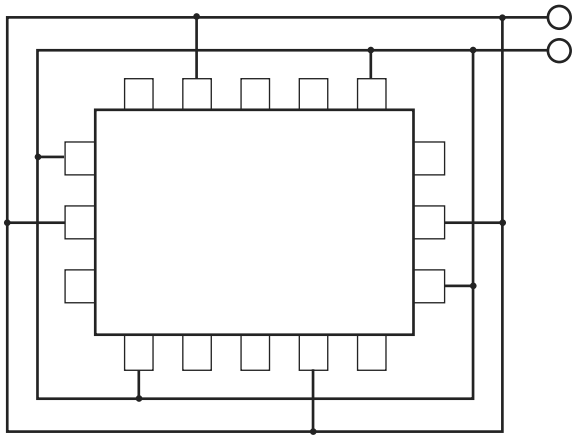
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH, 00000BH	(Disabled)				
00000CH	Port C data register	PDRC	R/W	Port C	XXXXXXXXB
00000DH	Port D data register	PDRD	R/W	Port D	XXXXXXXXB
00000EH	Port E data register	PDRE	R/W	Port E	XXXXXXXXB
00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 direction register	DDR1	R/W	Port 1	XX000000B
000012H	Port 2 direction register	DDR2	R/W	Port 2	000000XXB
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 direction register	DDR9	R/W	Port 9	X0000000B
00001AH	Analog input enable	ADER6	R/W	Port 6, A/D	11111111B
00001BH	(Disabled)				
00001CH	Port C direction register	DDRC	R/W	Port C	00000000B
00001DH	Port D direction register	DDRD	R/W	Port D	X0000000B
00001EH	Port E direction register	DDRE	R/W	Port E	XXXXX000B
00001FH	(Disabled)				
000020H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0B
000021H	Higher A/D control status register	ADCS1	R/W		0000000XB
000022H	Lower A/D control status register	ADCR0	R		00000000B
000023H	Higher A/D data register	ADCR1	R		XXXXXX00B

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003700H to 0037FFH	Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS"				
003800H to 0038FFH	Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS"				
003900H to 00391FH	(Disabled)				
003920H	PPG0 down counter register	PDCR0	R	16-bit PPG0	11111111B
003921H					11111111B
003922H	PPG0 cycle setting register	PCSR0	W		11111111B
003923H					11111111B
003924H	PPG0 duty setting register	PDUT0	W	16-bit PPG0	00000000B
003925H					00000000B
003926H	PPG0 output division setting register	PPGDIV0	R/W, R		11111100B
003927H	(Disabled)				
003928H	PPG1 down counter register	PDCR1	R	16-bit PPG1	11111111B
003929H					11111111B
00392AH	PPG1 cycle setting register	PCSR1	W		11111111B
00392BH					11111111B
00392CH	PPG1 duty setting register	PDUT1	W		00000000B
00392DH					00000000B
00392EH	PPG1output division setting register	PPGDIV1	R/W, R		11111100B
00392FH	(Disabled)				
003930H	PPG2 down counter register	PDCR2	R	16-bit PPG2	11111111B
003931H					11111111B
003932H	PPG2 cycle setting register	PCSR2	W		11111111B
003933H					11111111B
003934H	PPG2 duty setting register	PDUT2	W		00000000B
003935H					00000000B
003936H	PPG2 output division setting register	PPGDIV2	R/W, R		11111100B
003937H to 00393FH	(Disabled)				
003940H	Input capture register 4	IPCP4	R	Input capture 4/5	XXXXXXXXB
003941H					XXXXXXXXB
003942H	Input capture register 5	IPCP5	R		XXXXXXXXB
003943H					XXXXXXXXB

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003970H to 003973H	(Disabled)				
003974H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXXB
003975H	Amplitude data register 1	SGAR1	R/W		00000000B
003976H	Decrement grade register 1	SGDR1	R/W		XXXXXXXXB
003977H	Tone count register 1	SGTR1	R/W		XXXXXXXXB
003978H to 00397FH	(Disabled)				
003980H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXXB
003981H					XXXXXXXXB
003982H	PWM2 compare register 0	PWC20	R/W		XXXXXXXXB
003983H					XXXXXXXXB
003984H	PWM1 select register 0	PWS10	R/W		00000000B
003985H	PWM2 select register 0	PWS20	R/W		X0000000B
003986H, 003987H	(Disabled)				
003988H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXXB
003989H					XXXXXXXXB
00398AH	PWM2 compare register 1	PWC21	R/W		XXXXXXXXB
00398BH					XXXXXXXXB
00398CH	PWM1 select register 1	PWS11	R/W		00000000B
00398DH	PWM2 select register 1	PWS21	R/W		X0000000B
00398EH, 00398FH	(Disabled)				
003990H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXXB
003991H					XXXXXXXXB
003992H	PWM2 compare register 2	PWC22	R/W		XXXXXXXXB
003993H					XXXXXXXXB
003994H	PWM1 select register 2	PWS12	R/W		00000000B
003995H	PWM2 select register 2	PWS22	R/W		X0000000B
003996H, 003997H	(Disabled)				

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Address	Register name	Symbol	Read/write	Resource name	Initial value
003998H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXXB
003999H					XXXXXXXXB
00399AH	PWM2 compare register 3	PWC23	R/W		XXXXXXXXB
00399BH					XXXXXXXXB
00399CH	PWM1 select register 3	PWS13	R/W		00000000B
00399DH	PWM2 select register 3	PWS23	R/W		X0000000B
00399EH to 0039A5H	(Disabled)				
0039A6H	Flash write control register 0	FWR0	R/W	Flash I/F	00000000B
0039A7H	Flash write control register 1	FWR1			00000000B
0039A8H to 0039BFH	(Disabled)				
0039C0H to 0039DFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0039E0H to 0039FFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				
003A00H to 003AFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003B00H to 003BFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003C00H to 003CFFH	Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
003D00H to 003DFFH	Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
003E00H to 003EFFH	Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
003F00H to 003FFFH	Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS”				

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

List of Message Buffers (DLC Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A60H	003B60H	003760H	003860H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003B61H	003761H	003861H				
003A62H	003B62H	003762H	003862H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003B63H	003763H	003863H				
003A64H	003B64H	003764H	003864H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003B65H	003765H	003865H				
003A66H	003B66H	003766H	003866H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003B67H	003767H	003867H				
003A68H	003B68H	003768H	003868H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003B69H	003769H	003869H				
003A6AH	003B6AH	00376AH	00386AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003B6BH	00376BH	00386BH				
003A6CH	003B6CH	00376CH	00386CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003B6DH	00376DH	00386DH				
003A6EH	003B6EH	00376EH	00386EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003B6FH	00376FH	00386FH				
003A70H	003B70H	003770H	003870H	DLC register 8	DLCR8	R/W	----XXXXB
003A71H	003B71H	003771H	003871H				
003A72H	003B72H	003772H	003872H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003B73H	003773H	003873H				
003A74H	003B74H	003774H	003874H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003B75H	003775H	003875H				
003A76H	003B76H	003776H	003876H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003B77H	003777H	003877H				
003A78H	003B78H	003778H	003878H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003B79H	003779H	003879H				
003A7AH	003B7AH	00377AH	00387AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003B7BH	00377BH	00387BH				
003A7CH	003B7CH	00377CH	00387CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003B7DH	00377DH	00387DH				
003A7EH	003B7EH	00377EH	00387EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003B7FH	00377FH	00387FH				

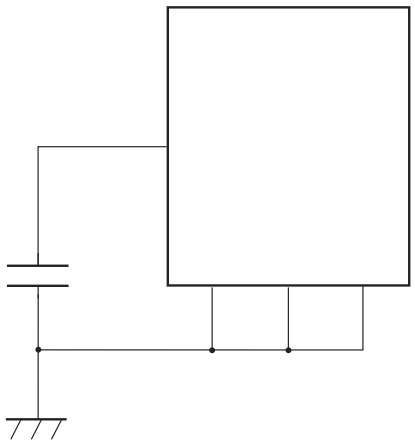
2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.0	5.5	V	The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
		4.4	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin.
Operating temperature	T_A	− 40	+ 105	°C	

* : Refer to the following diagram for details on the connection of the smoothing capacitor C_S.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(4) UART0/1/2/3 (LIN/SCI)

- **Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}			t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

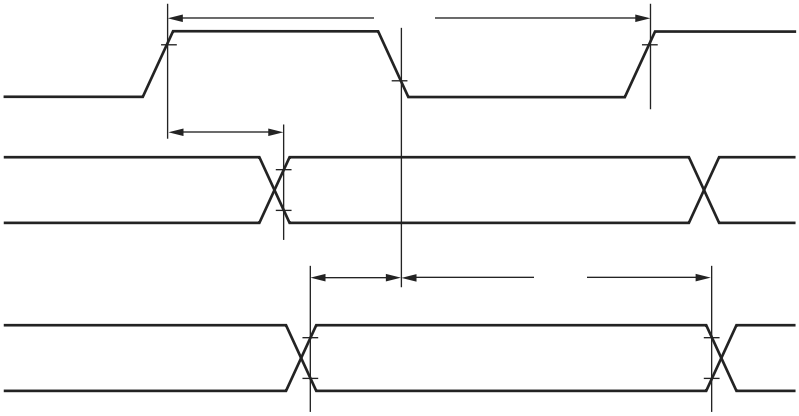
• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

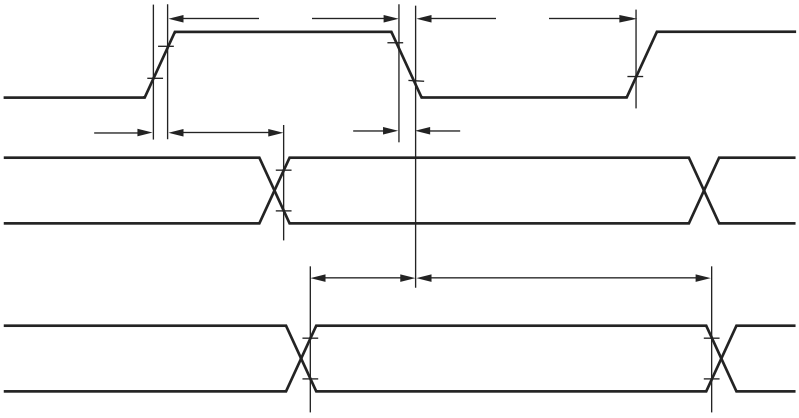
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}			t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Internal shift clock mode



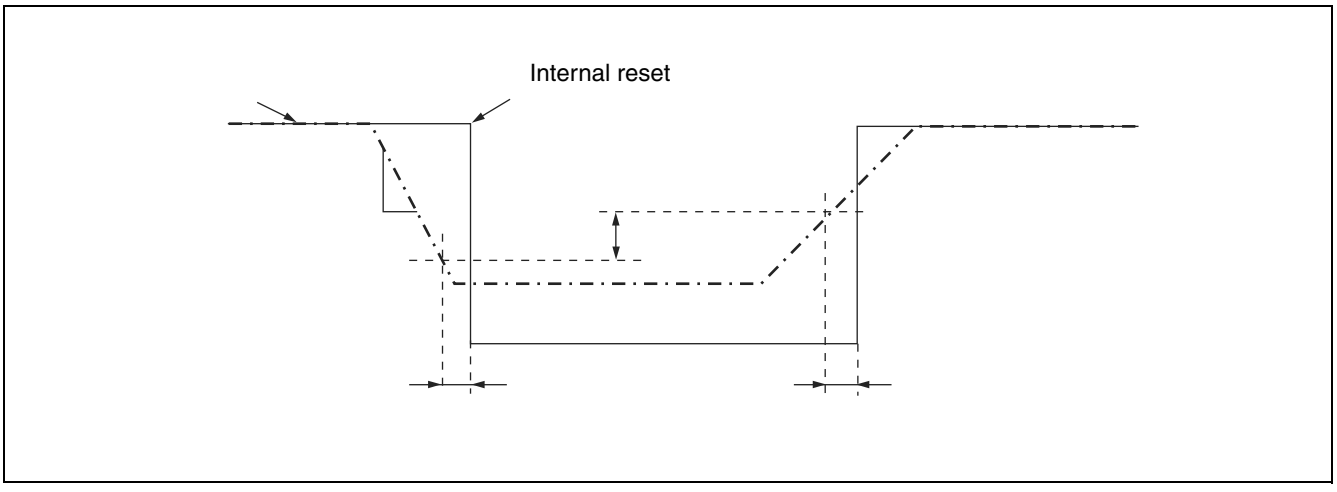
- External shift clock mode



(7) Low voltage detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

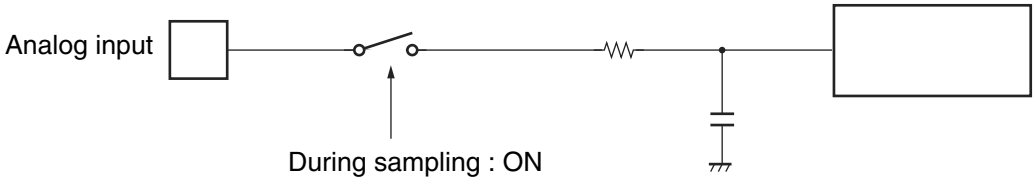
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V_{DL}	VCC	—	4.0	4.2	4.4	V	Flash memory product, during voltage drop
				3.7	4.0	4.3	V	Evaluation product, during voltage drop
Hysteresis width	V_{HYS}	VCC	—	190	—	—	mV	Flash memory product, during voltage rise
				0.1	—	—	V	Evaluation product, during voltage rise
Power supply voltage change rate	dV/dt	VCC	—	– 0.1	—	+ 0.1	V/µs	Flash memory product, dV/dt at low voltage reset
				–0.004	—	+ 0.004	V/µs	Flash memory product, dV/dt at standard value of low voltage detection/release voltage
				– 0.1	—	+ 0.02	V/µs	Evaluation product
Detection delay time	td	—	—	—	—	3.2	µs	Flash memory product, when dV/dt ≤ 0.004 V/µs
				—	—	35	µs	Evaluation product



• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

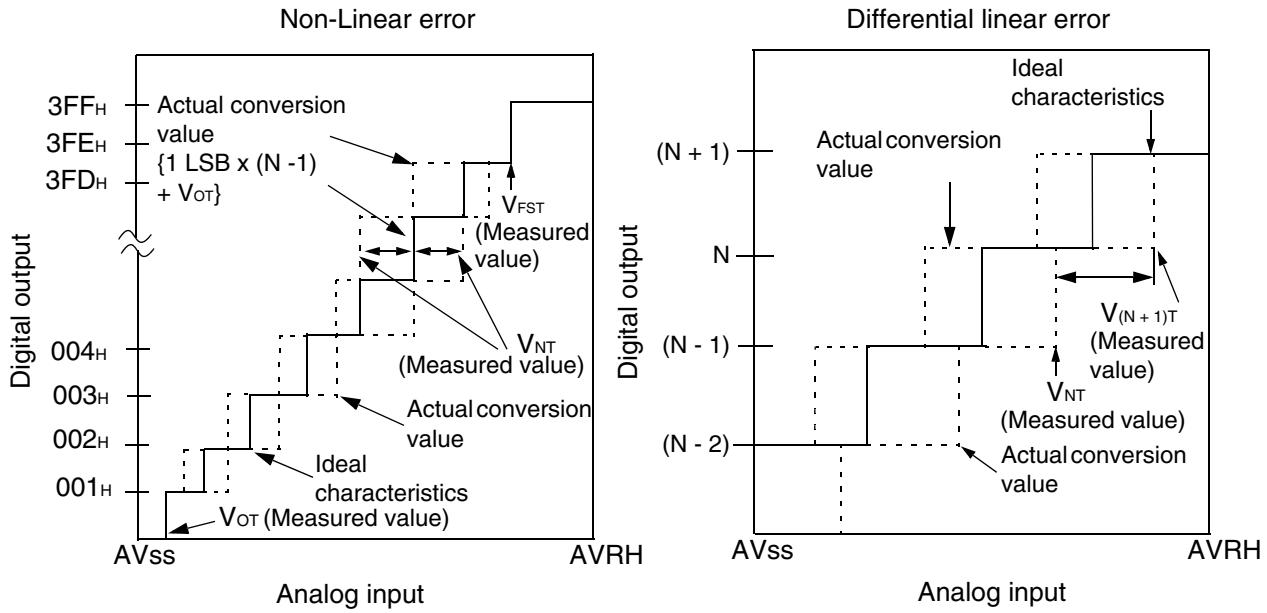
	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	12.1 kΩ (Max)	8.5 pF (Max)

MB90V920-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

Note : The values are reference values.

(Continued)



$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; • Serial communication • Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970$_H$”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR

The vertical lines marked in the left side of the page show the changes.