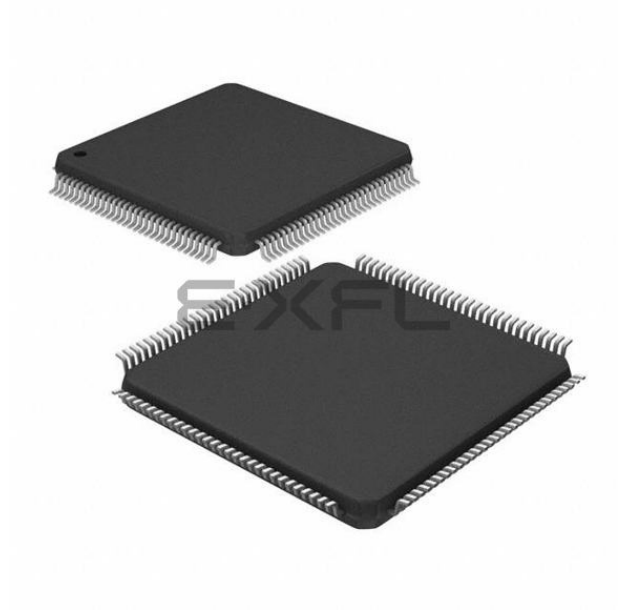
Infineon Technologies - MB90922NCSPMC-GS-220E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-220e1

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

Pin no.	Pin name	I/O circuit type*1	Function
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin

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Pin no.	Pin name	I/O circuit type*1	Function
61	P54	I	General-purpose I/O port
	TX0		CAN interface 0 TX output pin
	TX2		CAN interface 2 TX output pin
	SGA1		Sound generator ch.1 SGA output pin
63	P55	I	General-purpose I/O port
	RX0		CAN interface 0 RX input pin
	RX2		CAN interface 2 RX input pin
	INT2		INT2 external interrupt input pin
91	P56	I	General-purpose I/O port
	SGO0		Sound generator ch.0 SGO output pin
	FRCK		Free-run timer clock input pin
92	P57	I	General-purpose I/O port
	SGA0		Sound generator ch.0 SGA output pin
39	P60	H	General-purpose I/O port
	AN0		A/D converter input pin
40	P61	H	General-purpose I/O port
	AN1		A/D converter input pin
41	P62	H	General-purpose I/O port
	AN2		A/D converter input pin
42	P63	H	General-purpose I/O port
	AN3		A/D converter input pin
43	P64	H	General-purpose I/O port
	AN4		A/D converter input pin
44	P65	H	General-purpose I/O port
	AN5		A/D converter input pin
45	P66	H	General-purpose I/O port
	AN6		A/D converter input pin
46	P67	H	General-purpose I/O port
	AN7		A/D converter input pin
67	P70	L	General-purpose output-only port
	PWM1P0		Stepping motor controller ch.0 output pin
68	P71	L	General-purpose output-only port
	PWM1M0		Stepping motor controller ch.0 output pin
69	P72	L	General-purpose output-only port
	PWM2P0		Stepping motor controller ch.0 output pin

(Continued)

■ HANDLING DEVICES

• Strictly observe maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC}, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

• Supply voltage stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

• Precautions when turning the power on

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μs.

• Handling unused pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

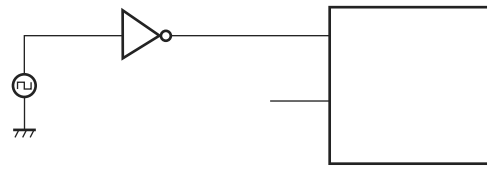
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

• Handling A/D converter power supply pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

• Notes on using an external clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

- **Serial communication**

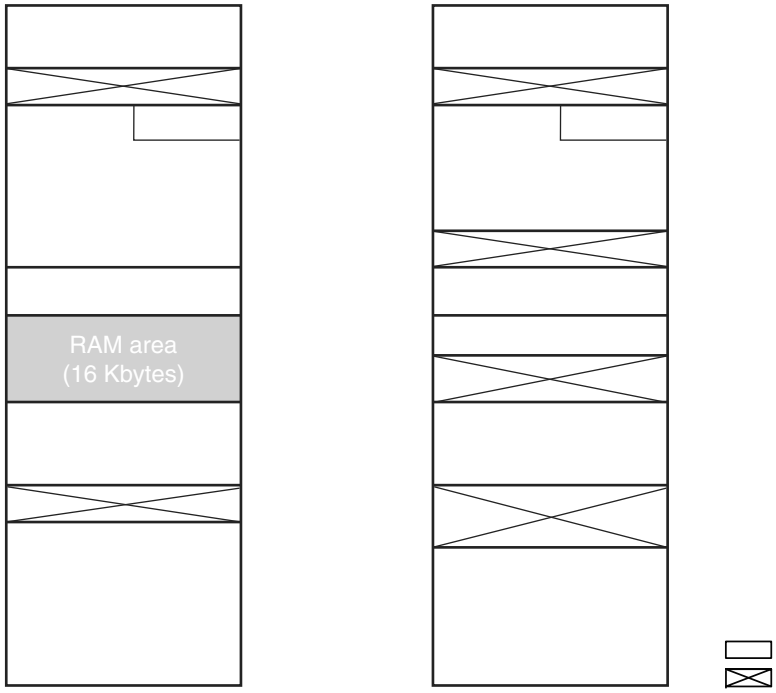
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000D4H	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000B
0000D5H	Higher timer control status register 2	TMCSR2H	R/W		XXX10000B
0000D6H	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000B
0000D7H	Higher timer control status register 3	TMCSR3H	R/W		XXX10000B
0000D8H	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000B
0000D9H	Higher sound control register 1	SGCRH1	R/W		0XXXX100B
0000DAH	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000B
0000DBH	Higher PPG3 control status register	PCNTH3	R/W		00000001B
0000DCH	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000B
0000DDH	Higher PPG4 control status register	PCNTH4	R/W		00000001B
0000DEH	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000B
0000DFH	Higher PPG5 control status register	PCNTH5	R/W		00000001B
0000E0H	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000B
0000E1H	Serial control register 2	SCR2	R/W, W		00000000B
0000E2H	Reception/transmission data register 2	RDR2/ TDR2	R/W		00000000B
0000E3H	Serial status register 2	SSR2	R/W, R		00001000B
0000E4H	Extended communication control register 2	ECCR2	R/W, R		000000XXB
0000E5H	Extended status control register 2	ESCR2	R/W		00000100B
0000E6H	Baud rate generator register 20	BGR20	R/W		00000000B
0000E7H	Baud rate generator register 21	BGR21	R/W, R		00000000B
0000E8H	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000B
0000E9H	Serial control register 3	SCR3	R/W, W		00000000B
0000EAH	Reception/transmission data register 3	RDR3/ TDR3	R/W		00000000B
0000EBH	Serial status register 3	SSR3	R/W, R		00001000B
0000ECH	Extended communication control register 3	ECCR3	R/W, R		000000XXB
0000EDH	Extended status control register 3	ESCR3	R/W		00000100B
0000EEH	Baud rate generator register 30	BGR30	R/W		00000000B
0000EFH	Baud rate generator register 31	BGR31	R/W, R		00000000B
001FF0H	Program address detection register 0	PADR0	R/W	Address match detection	XXXXXXXXB
001FF1H	Program address detection register 1	PADR0	R/W		XXXXXXXXB
001FF2H	Program address detection register 2	PADR0	R/W		XXXXXXXXB
001FF3H	Program address detection register 3	PADR1	R/W		XXXXXXXXB
001FF4H	Program address detection register 4	PADR1	R/W		XXXXXXXXB
001FF5H	Program address detection register 5	PADR1	R/W		XXXXXXXXB

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■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

List of Message Buffers (ID Registers)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A00H to 003A1FH	003B00H to 003B1FH	003700H to 00371FH	003800H to 00381FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003B20H	003720H	003820H	ID register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
003A21H	003B21H	003721H	003821H				
003A22H	003B22H	003722H	003822H				XXXXX---B XXXXXXXXB
003A23H	003B23H	003723H	003823H				
003A24H	003B24H	003724H	003824H	ID register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
003A25H	003B25H	003725H	003825H				
003A26H	003B26H	003726H	003826H				XXXXX---B XXXXXXXXB
003A27H	003B27H	003727H	003827H				
003A28H	003B28H	003728H	003828H	ID register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
003A29H	003B29H	003729H	003829H				
003A2AH	003B2AH	00372AH	00382AH				XXXXX---B XXXXXXXXB
003A2BH	003B2BH	00372BH	00382BH				
003A2CH	003B2CH	00372CH	00382CH	ID register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
003A2DH	003B2DH	00372DH	00382DH				
003A2EH	003B2EH	00372EH	00382EH				XXXXX---B XXXXXXXXB
003A2FH	003B2FH	00372FH	00382FH				
003A30H	003B30H	003730H	003830H	ID register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
003A31H	003B31H	003731H	003831H				
003A32H	003B32H	003732H	003832H				XXXXX---B XXXXXXXXB
003A33H	003B33H	003733H	003833H				
003A34H	003B34H	003734H	003834H	ID register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
003A35H	003B35H	003735H	003835H				
003A36H	003B36H	003736H	003836H				XXXXX---B XXXXXXXXB
003A37H	003B37H	003737H	003837H				
003A38H	003B38H	003738H	003838H	ID register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
003A39H	003B39H	003739H	003839H				
003A3AH	003B3AH	00373AH	00383AH				XXXXX---B XXXXXXXXB
003A3BH	003B3BH	00373BH	00383BH				
003A3CH	003B3CH	00373CH	00383CH	ID register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
003A3DH	003B3DH	00373DH	00383DH				
003A3EH	003B3EH	00373EH	00383EH				XXXXX---B XXXXXXXXB
003A3FH	003B3FH	00373FH	00383FH				

(Continued)

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Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40H	003B40H	003740H	003840H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003A41H	003B41H	003741H	003841H				
003A42H	003B42H	003742H	003842H				XXXXX---B XXXXXXXXB
003A43H	003B43H	003743H	003843H				
003A44H	003B44H	003744H	003844H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003A45H	003B45H	003745H	003845H				
003A46H	003B46H	003746H	003846H				XXXXX---B XXXXXXXXB
003A47H	003B47H	003747H	003847H				
003A48H	003B48H	003748H	003848H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003A49H	003B49H	003749H	003849H				
003A4AH	003B4AH	00374AH	00384AH				XXXXX---B XXXXXXXXB
003A4BH	003B4BH	00374BH	00384BH				
003A4CH	003B4CH	00374CH	00384CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
003A4DH	003B4DH	00374DH	00384DH				
003A4EH	003B4EH	00374EH	00384EH				XXXXX---B XXXXXXXXB
003A4FH	003B4FH	00374FH	00384FH				
003A50H	003B50H	003750H	003850H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003A51H	003B51H	003751H	003851H				
003A52H	003B52H	003752H	003852H				XXXXX---B XXXXXXXXB
003A53H	003B53H	003753H	003853H				
003A54H	003B54H	003754H	003854H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003A55H	003B55H	003755H	003855H				
003A56H	003B56H	003756H	003856H				XXXXX---B XXXXXXXXB
003A57H	003B57H	003757H	003857H				
003A58H	003B58H	003758H	003858H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003A59H	003B59H	003759H	003859H				
003A5AH	003B5AH	00375AH	00385AH				XXXXX---B XXXXXXXXB
003A5BH	003B5BH	00375BH	00385BH				
003A5CH	003B5CH	00375CH	00385CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
003A5DH	003B5DH	00375DH	00385DH				
003A5EH	003B5EH	00375EH	00385EH				XXXXX---B XXXXXXXXB
003A5FH	003B5FH	00375FH	00385FH				

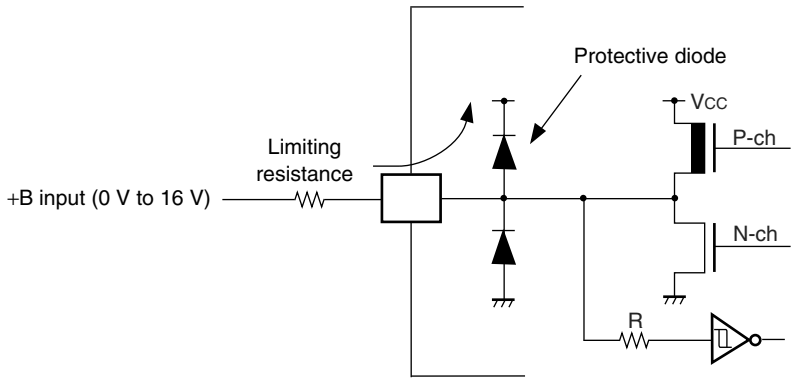
(Continued)

*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “ operating factor”.

*7 :
- Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

• Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

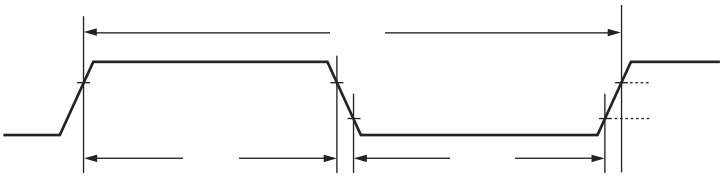
3. DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

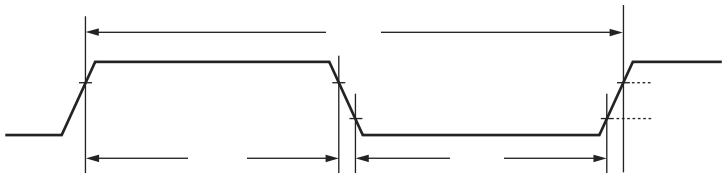
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHA}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHC}	—	—	0.7 V_{CC}	—	—	V	$\overline{RST}$ input pin (CMOS hysteresis)
"L" level input voltage	V_{ILA}	—	—	—	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	—	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	—	—	0.3 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
Power supply current*	I_{CC}	V_{CC}	Maximum operating frequency F_{CP} = 32 MHz, normal operation	—	35	45	mA	
			Maximum operating frequency F_{CP} = 32 MHz, writing Flash memory	—	55	65	mA	
	I_{CCS}		Operating frequency F_{CP} = 32 MHz, sleep mode	—	13	20	mA	
	I_{CTS}		Operating frequency F_{CP} = 2 MHz, time-base timer mode	—	0.6	1.0	mA	
	I_{CTSPLL}		Operating frequency F_{CP} = 32 MHz, PLL timer mode, External frequency = 4 MHz	—	2.5	4	mA	
	I_{CCL}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub clock operation	—	120	270	µA	
	I_{CCLS}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub sleep operation	—	100	200	µA	
	I_{CCT}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, watch mode	—	90	180	µA	
	I_{CCH}		T_A = + 25 °C, stop mode	—	80	170	µA	

(Continued)

• X0, X1 clock timing



• X0A, X1A clock timing



(2) Reset input

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

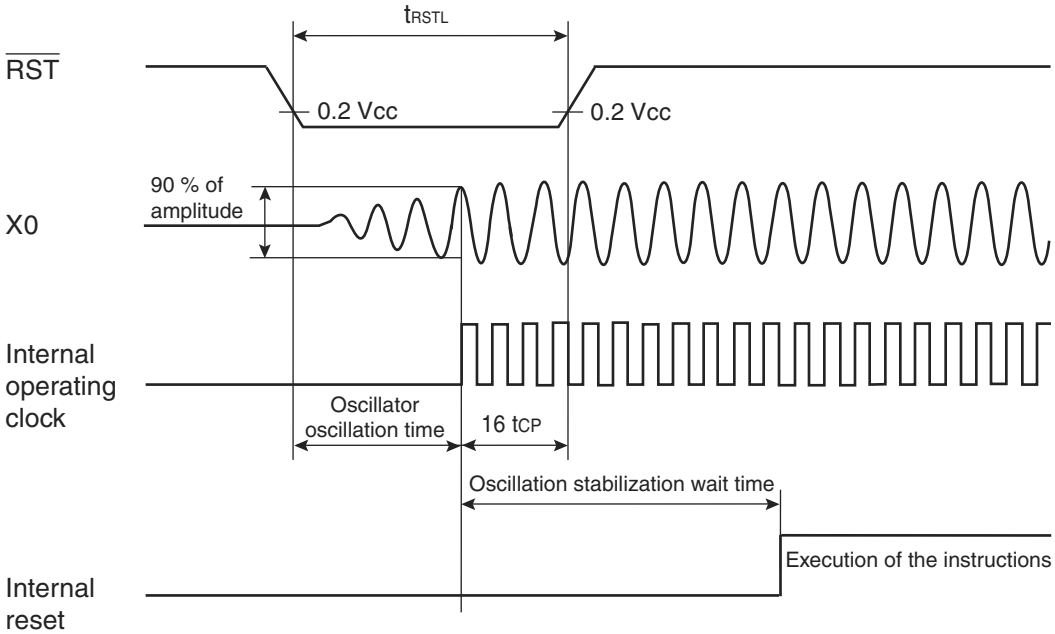
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	During normal operation
			Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	In time-base timer mode

*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

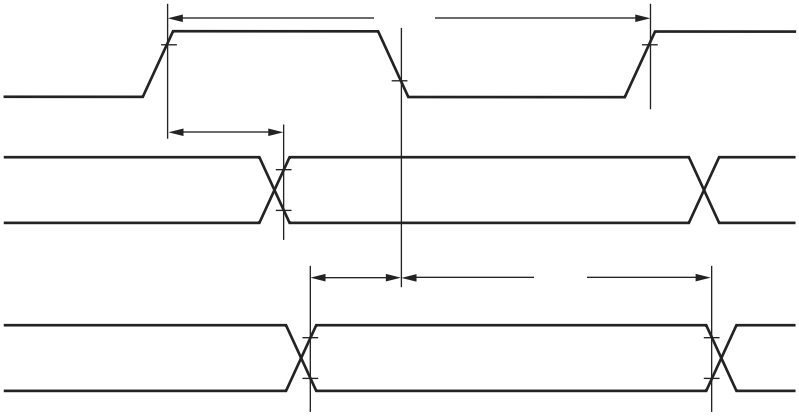
Note : t_{CP} is the internal operating clock cycle time. (Unit : ns)

• During normal operation

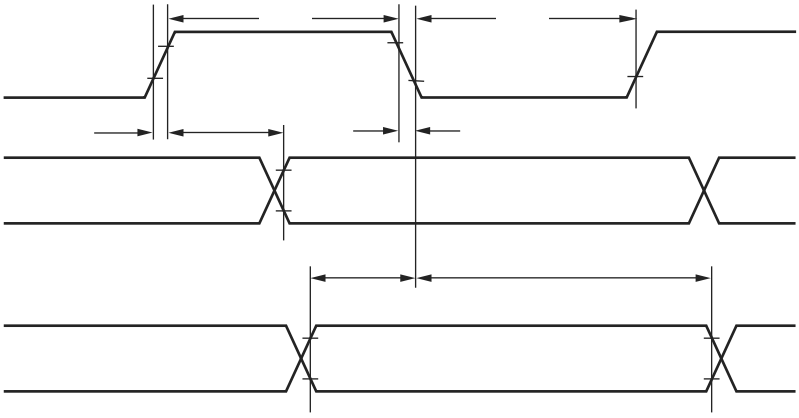
• In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



- Internal shift clock mode



- External shift clock mode



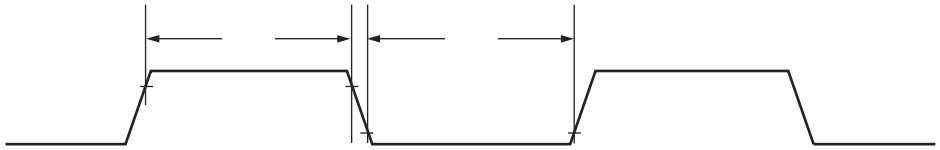
(5) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note : t_{CP} is the internal operating clock cycle time. Refer to " (1) Clock timing".

- Timer input timing



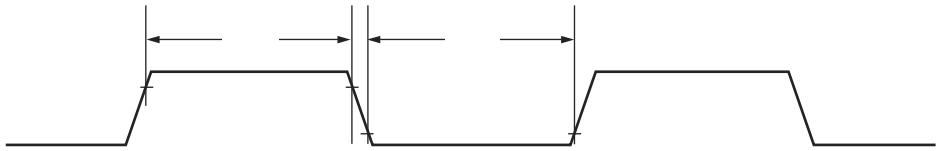
(6) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

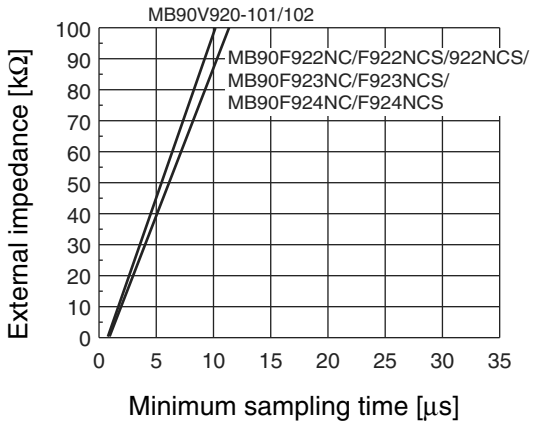
Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Trigger input timing

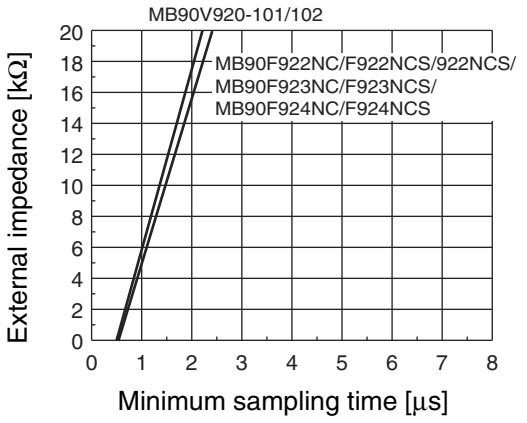


- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

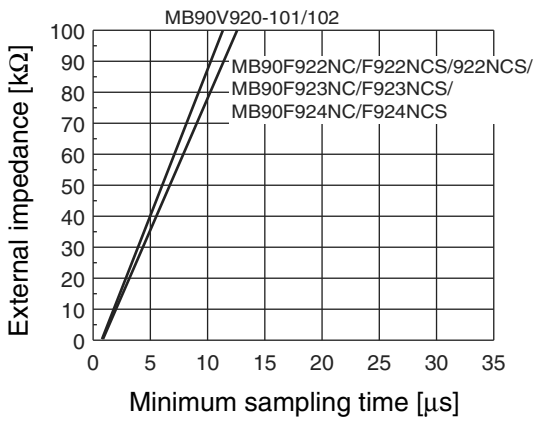


(External impedance = 0 kΩ to 20 kΩ)

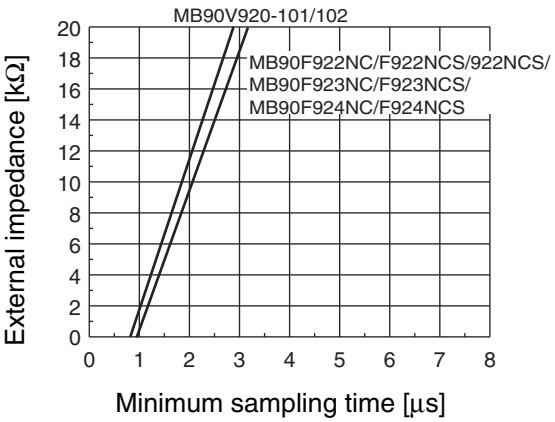


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)

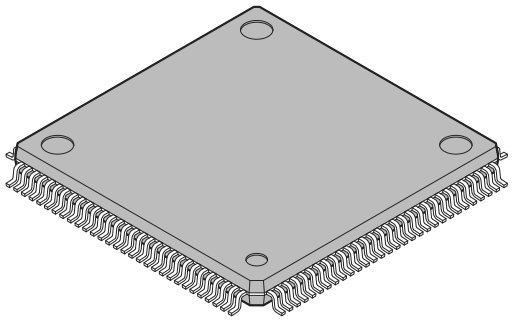


(External impedance = 0 kΩ to 20 kΩ)



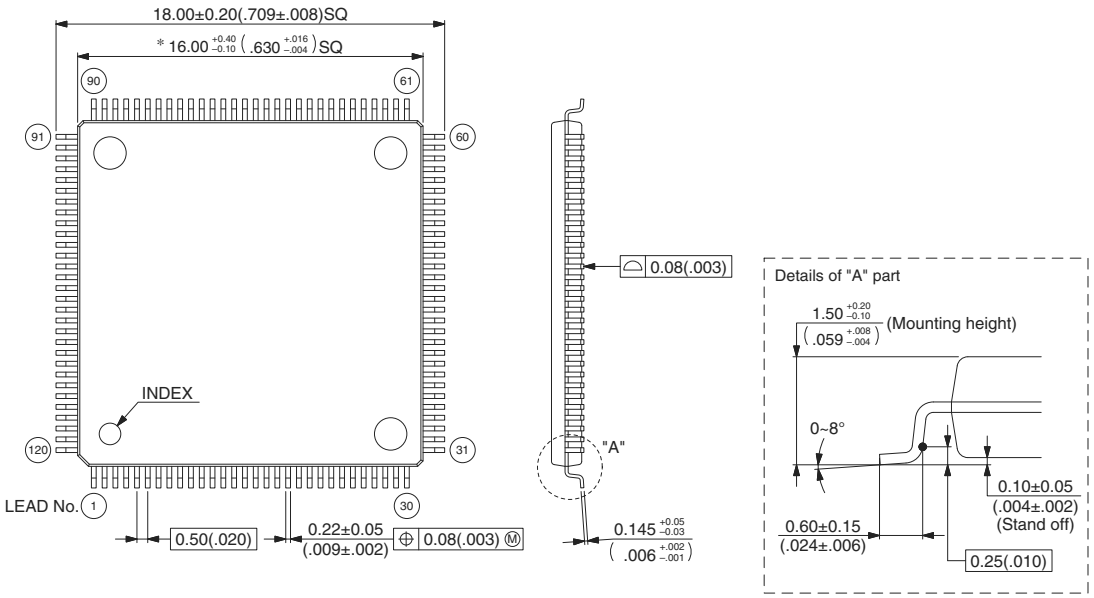
- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/