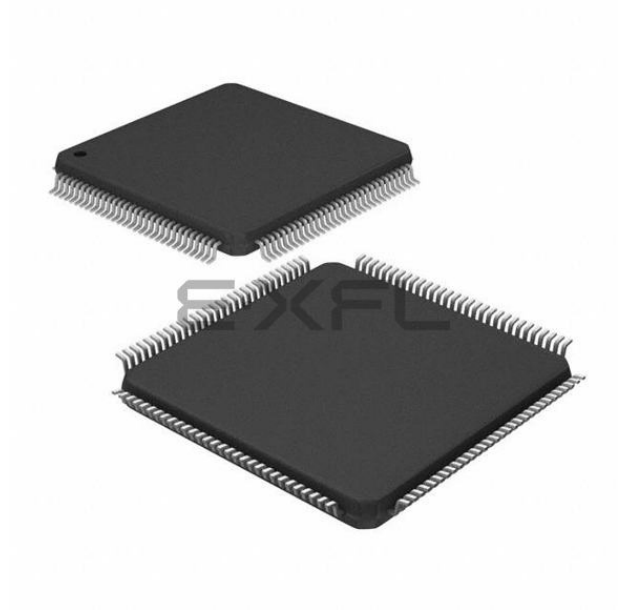
Infineon Technologies - MB90922NCSPMC-GS-224E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-224e1

(Continued)

- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at f_{CP} = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

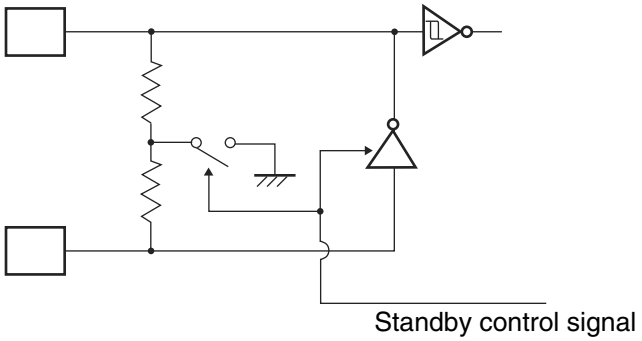
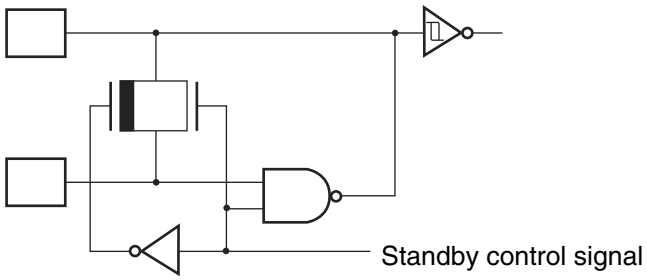
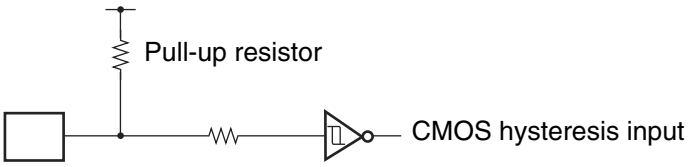
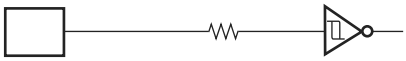
(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance : approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) • Attached pull-up resistor : approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.

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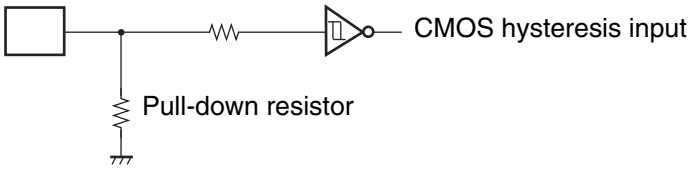
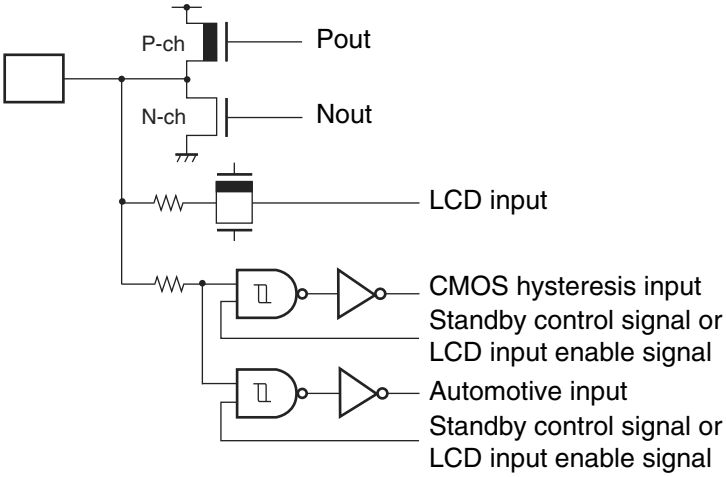
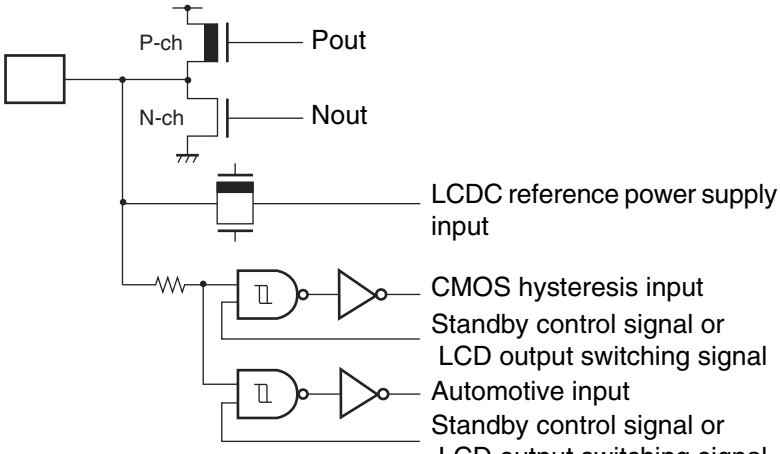
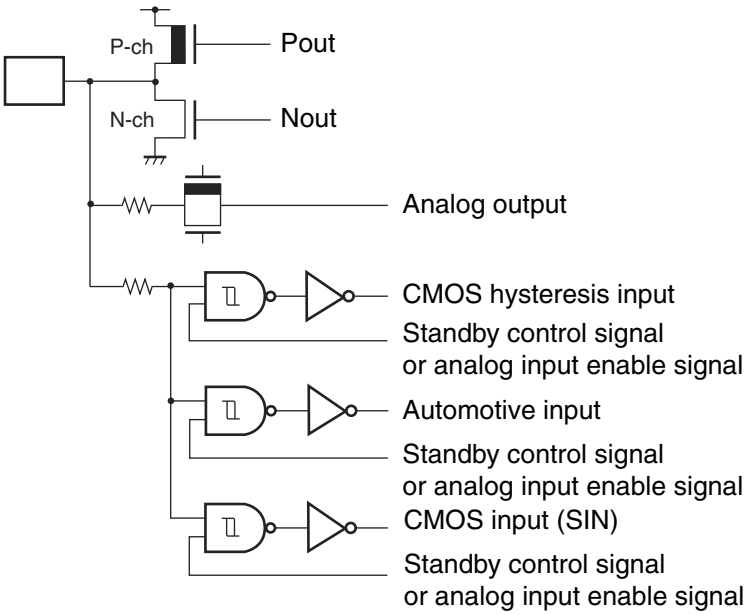
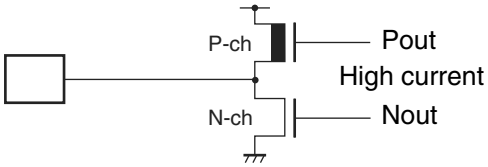
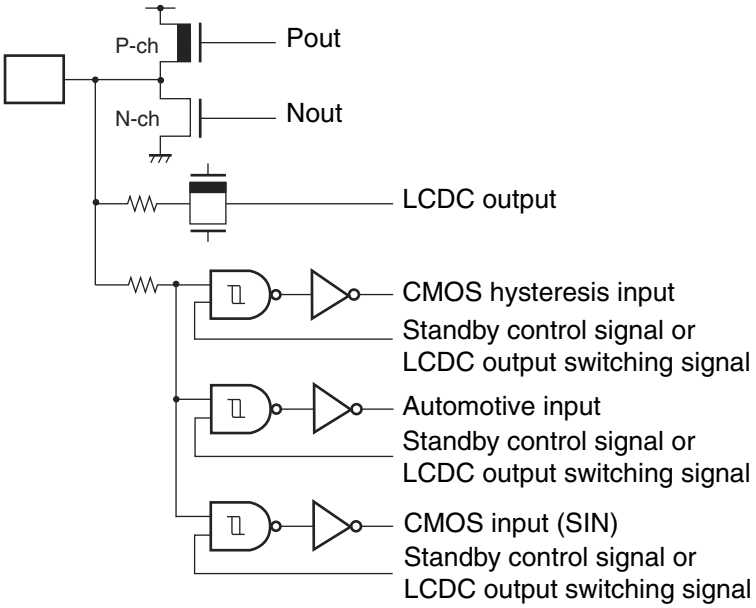
Type	Circuit	Remarks
E		Input-only pin (with pull-down resistance) • Attached pull-down resistance: approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.
F		LCD output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

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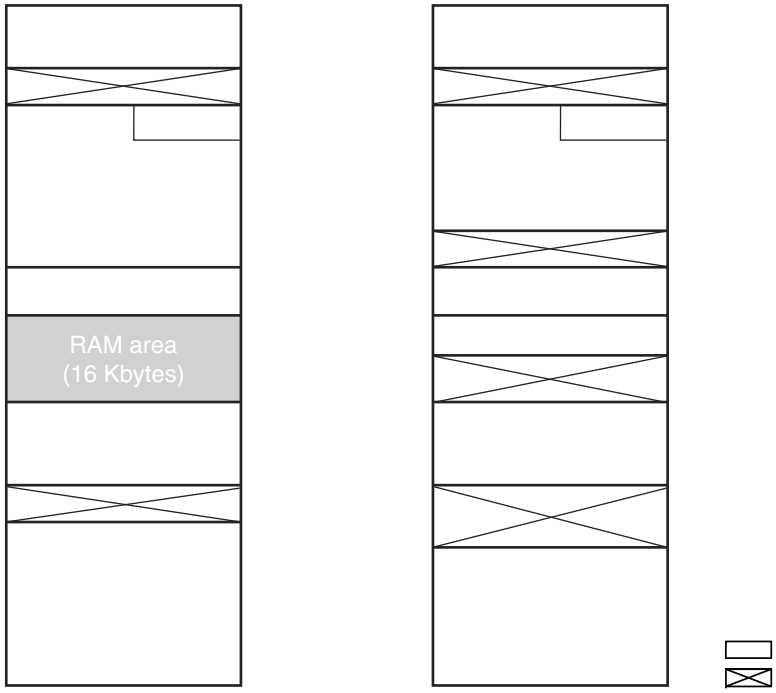
■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000083H	(Disabled)				
000084H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	000000X0B
000085H	(Disabled)				
000086H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	000000X0B
000087H	(Disabled)				
000088H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXX111B
000089H	(Disabled)				
00008AH	A/D setting register 0	ADSR0	R/W	A/D converter	00000000B
00008BH	A/D setting register 1	ADSR1	R/W		00000000B
00008CH	Port input level select 0	PIL0	R/W	Port input level select	00000000B
00008DH	Port input level select 1	PIL1	R/W		XXXX0000B
00008EH	Port input level select 2	PIL2	R/W		XXXX0000B
00008FH to 00009DH	(Disabled)				
00009EH	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0XB
00009FH	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	XXXXXXX0B
0000A0H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000B
0000A1H	Clock select register	CKSCR	R/W, R		11111100B
0000A2H to 0000A7H	(Disabled)				
0000A8H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111B
0000A9H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100B
0000AAH	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000B
0000ABH to 0000ADH	(Disabled)				
0000AEH	Flash memory control status register	FMCS	R/W	Flash interface	000X0000B
0000AFH	(Disabled)				

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111B
0000B1H	Interrupt control register 01	ICR01	R/W		00000111B
0000B2H	Interrupt control register 02	ICR02	R/W		00000111B
0000B3H	Interrupt control register 03	ICR03	R/W		00000111B
0000B4H	Interrupt control register 04	ICR04	R/W		00000111B
0000B5H	Interrupt control register 05	ICR05	R/W		00000111B
0000B6H	Interrupt control register 06	ICR06	R/W		00000111B
0000B7H	Interrupt control register 07	ICR07	R/W		00000111B
0000B8H	Interrupt control register 08	ICR08	R/W		00000111B
0000B9H	Interrupt control register 09	ICR09	R/W		00000111B
0000BAH	Interrupt control register 10	ICR10	R/W		00000111B
0000BBH	Interrupt control register 11	ICR11	R/W		00000111B
0000BCH	Interrupt control register 12	ICR12	R/W		00000111B
0000BDH	Interrupt control register 13	ICR13	R/W		00000111B
0000BEH	Interrupt control register 14	ICR14	R/W		00000111B
0000BFH	Interrupt control register 15	ICR15	R/W		00000111B
0000C0H to 0000C3H	(Disabled)				
0000C4H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000B
0000C5H	Serial control register 1	SCR1	R/W, W		00000000B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000B
0000C7H	Serial status register 1	SSR1	R/W, R		00001000B
0000C8H	Extended communication control register 1	ECCR1	R/W, R		000000XXB
0000C9H	Extended status control register 1	ESCR1	R/W		00000100B
0000CAH	Baud rate generator register 10	BGR10	R/W		00000000B
0000CBH	Baud rate generator register 11	BGR11	R/W, R		00000000B
0000CCH	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0B
0000CDH	Middle watch timer control register	WTCRM	R/W		00000000B
0000CEH	Higher watch timer control register	WTCRH	R/W		XXXXXX00B
0000CFH	Sub clock control register	PSCCR	W	Sub clock	XXXX0000B
0000D0H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000B
0000D1H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXB
0000D2H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000B
0000D3H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003944H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXXB
003945H					XXXXXXXXB
003946H	Input capture register 7	IPCP7	R		XXXXXXXXB
003947H					XXXXXXXXB
003948H to 00394FH	(Disabled)				
003950H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXXB
003951H					XXXXXXXXB
003952H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXXB
003953H					XXXXXXXXB
003954H to 003957H	(Disabled)				
003958H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXXB
003959H					XXXXXXXXB
00395AH					XXXXXXXXB
00395BH	Second data register	WTSR	R/W		XX000000B
00395CH	Minute data register	WTMR	R/W		XX000000B
00395DH	Hour data register	WTHR	R/W		XXX00000B
00395EH	Day data register	WTDR	R/W		00X00001B
00395FH	(Disabled)				
003960H	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXXB
003961H					XXXXXXXXB
003962H					XXXXXXXXB
003963H					XXXXXXXXB
003964H					XXXXXXXXB
003965H					XXXXXXXXB
003966H					XXXXXXXXB
003967H					XXXXXXXXB
003968H					XXXXXXXXB
003969H					XXXXXXXXB
00396AH					XXXXXXXXB
00396BH					XXXXXXXXB
00396CH					XXXXXXXXB
00396DH					XXXXXXXXB
00396EH					XXXXXXXXB
00396FH					XXXXXXXXB

(Continued)

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*2
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH*2
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$DV_{CC} = V_{CC}$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 4	+ 4	mA	*7
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	40	mA	*7
"L" level maximum output current*4	I_{OL1}	—	15	mA	Except P70 to P77 and P80 to P87
	I_{OL2}	—	40	mA	P70 to P77 and P80 to P87
"L" level average output current*5	I_{OLAV1}	—	4	mA	Except P70 to P77 and P80 to P87
	I_{OLAV2}	—	30	mA	P70 to P77 and P80 to P87
"L" level maximum total output current	ΣI_{OL1}	—	100	mA	Except P70 to P77 and P80 to P87
	ΣI_{OL2}	—	330	mA	P70 to P77 and P80 to P87
"L" level average total output current	ΣI_{OLAV1}	—	50	mA	Except P70 to P77 and P80 to P87
	ΣI_{OLAV2}	—	250	mA	P70 to P77 and P80 to P87
"H" level maximum output current	I_{OH1}*4	—	–15	mA	Except P70 to P77 and P80 to P87
	I_{OH2}*4	—	–40	mA	P70 to P77 and P80 to P87
"H" level average output current	I_{OHAV1}*5	—	–4	mA	Except P70 to P77 and P80 to P87
	I_{OHAV2}*5	—	–30	mA	P70 to P77 and P80 to P87
"H" level maximum total output current	ΣI_{OH1}	—	–100	mA	Except P70 to P77 and P80 to P87
	ΣI_{OH2}	—	–330	mA	P70 to P77 and P80 to P87
"H" level average total output current	ΣI_{OHAV1}*6	—	–50	mA	Except P70 to P77 and P80 to P87
	ΣI_{OHAV2}*6	—	–250	mA	P70 to P77 and P80 to P87
Power consumption	P_D	—	625	mW	
Operating temperature	T_A	– 40	+ 105	°C	
Storage temperature	T_{STG}	– 55	+ 150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : AV_{CC}, AVRH must not exceed V_{CC}, and AVRH must not exceed AV_{CC}.
When using an evaluation product, DV_{CC} must not exceed V_{CC} (however, DV_{CC} can be set to a higher voltage than V_{CC} when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, I_{CLAMP} is the applicable rating instead of V_I.

*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

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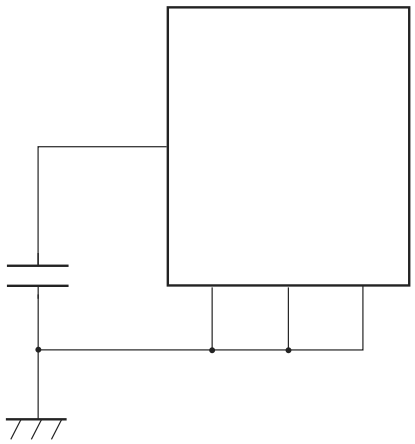
2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.0	5.5	V	The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
		4.4	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin.
Operating temperature	T_A	− 40	+ 105	°C	

* : Refer to the following diagram for details on the connection of the smoothing capacitor C_S.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = –30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product

(Continued)

(Continued)

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

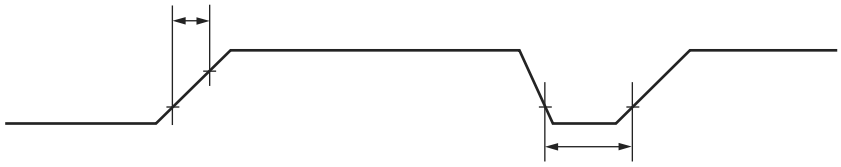
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCDC leakage current	I_{LCDC}	V0 to V3, COMm (m = 0 to 3) , SEGn, (n = 00 to 31)	—	—	—	5.0	µA	
LCD output impedance	Rvcom	COMn (n = 0 to 3)	—	—	—	4.5	kΩ	
	Rvseg	SEGn (n = 00 to 31)	—	—	—	17	kΩ	

* : Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

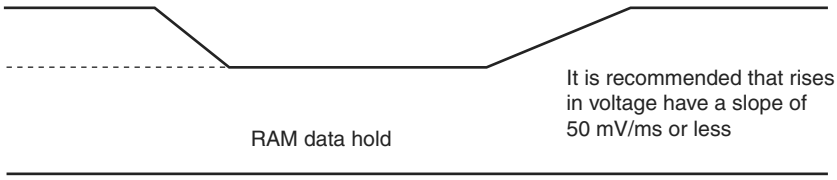
(3) Power-on reset

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	VCC	—	0.05	30	ms	
Power off time	t_{OFF}			1	—	ms	Waiting time until power-on



Note : Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



• **Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

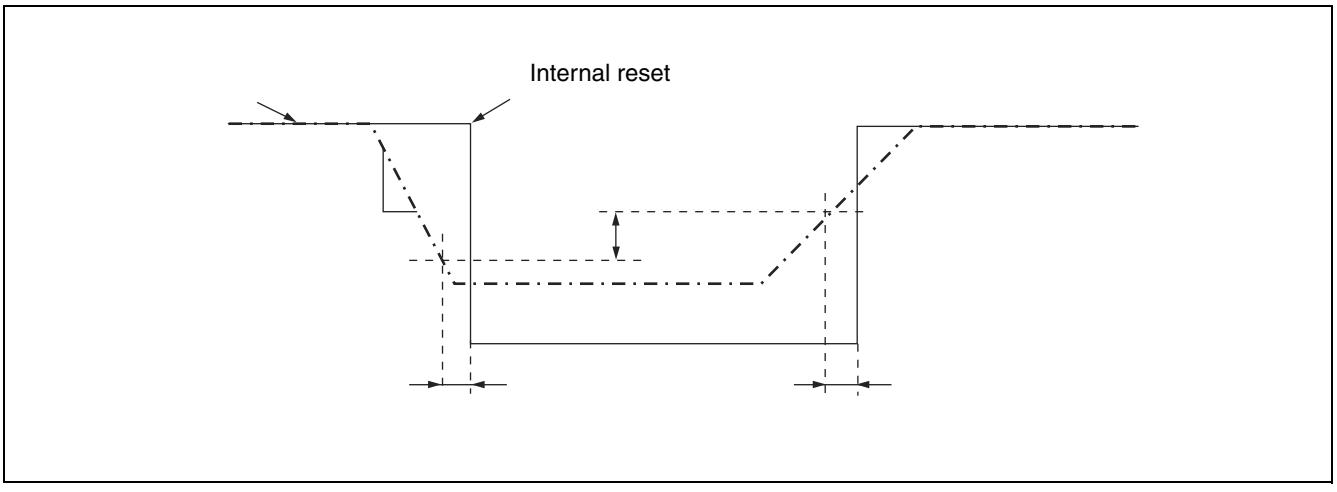
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}			t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
• C_L is the load capacitance connected to the pin during testing.
• t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

(7) Low voltage detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V_{DL}	VCC	—	4.0	4.2	4.4	V	Flash memory product, during voltage drop
				3.7	4.0	4.3	V	Evaluation product, during voltage drop
Hysteresis width	V_{HYS}	VCC	—	190	—	—	mV	Flash memory product, during voltage rise
				0.1	—	—	V	Evaluation product, during voltage rise
Power supply voltage change rate	dV/dt	VCC	—	– 0.1	—	+ 0.1	V/µs	Flash memory product, dV/dt at low voltage reset
				–0.004	—	+ 0.004	V/µs	Flash memory product, dV/dt at standard value of low voltage detection/release voltage
				– 0.1	—	+ 0.02	V/µs	Evaluation product
Detection delay time	td	—	—	—	—	3.2	µs	Flash memory product, when dV/dt ≤ 0.004 V/µs
				—	—	35	µs	Evaluation product



5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

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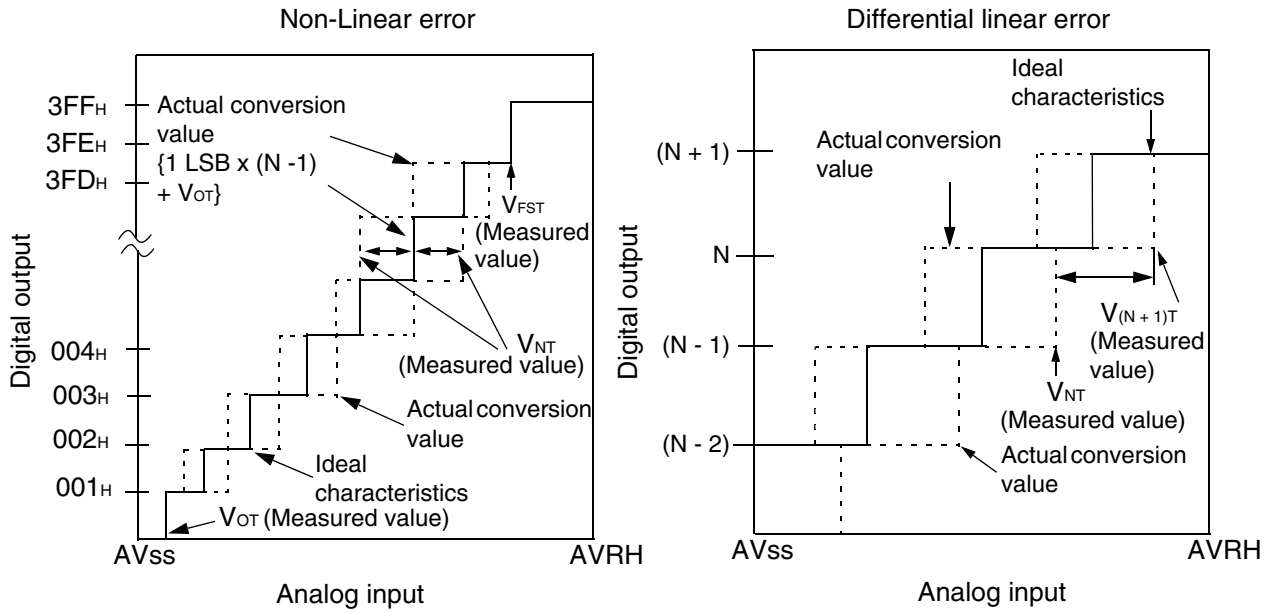

$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage when digital output changes from 000_H to 001_H
V_{FST} : Voltage when digital output changes from $3FE_H$ to $3FF_H$

■ MAJOR CHANGES IN THIS EDITION

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; • Serial communication • Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970$_H$”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR

The vertical lines marked in the left side of the page show the changes.

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