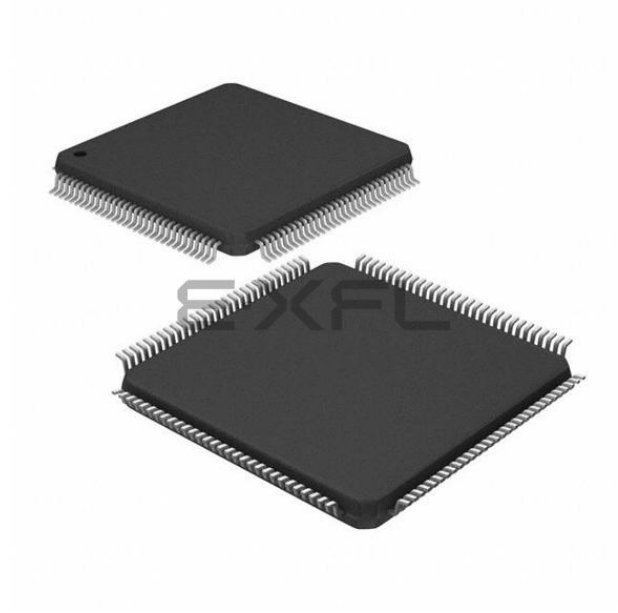
Infineon Technologies - MB90922NCSPMC-GS-243E1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90922ncspmc-gs-243e1

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

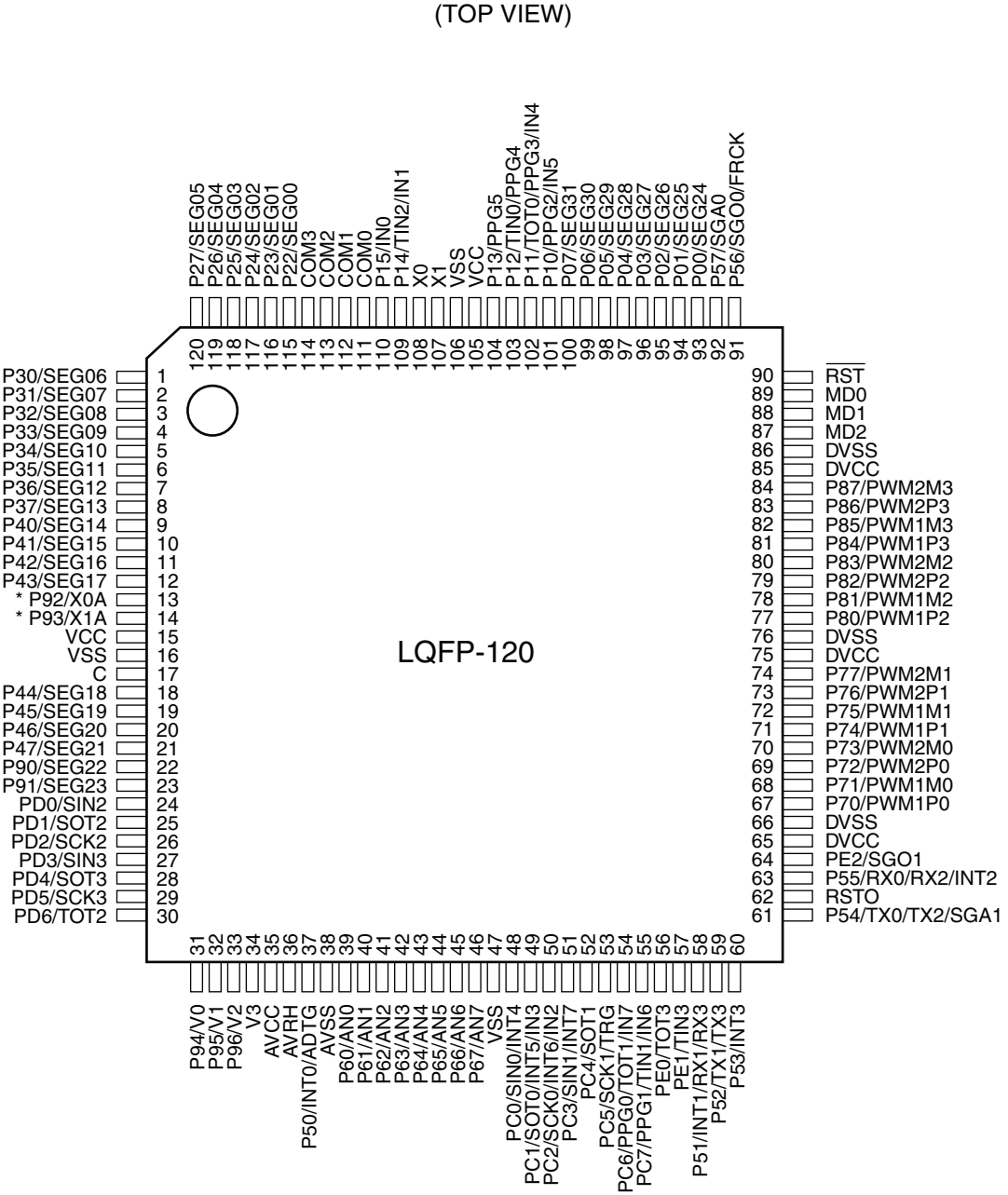
(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.9

■ PIN ASSIGNMENT



(FPT-120P-M21)

* : MB90V920-101, MB90F922NCS,MB90F923NCS,MB90F924NCS,MB90922NCS : P92, P93
MB90V920-102, MB90F922NC,MB90F923NC,MB90F924NC : X0A, X1A

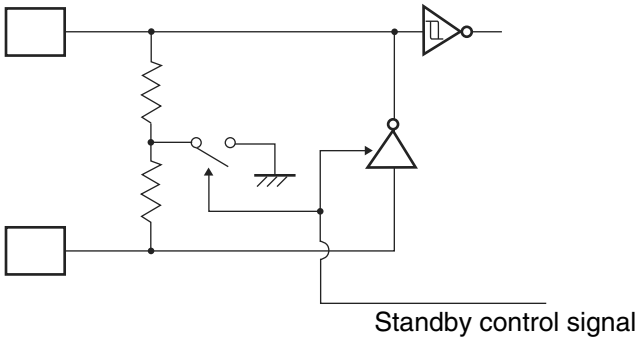
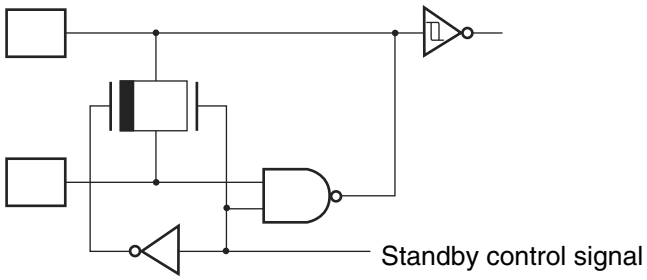
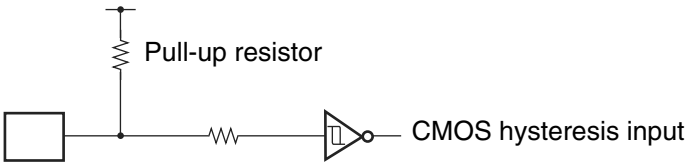
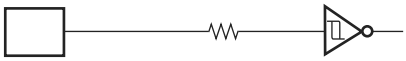
Pin no.	Pin name	I/O circuit type*1	Function
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin

(Continued)

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance : approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) • Attached pull-up resistor : approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.

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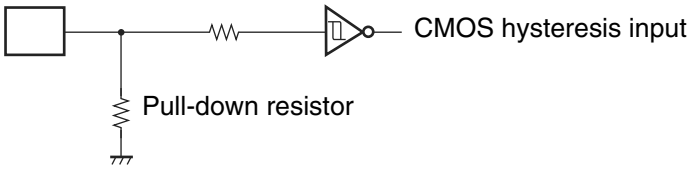
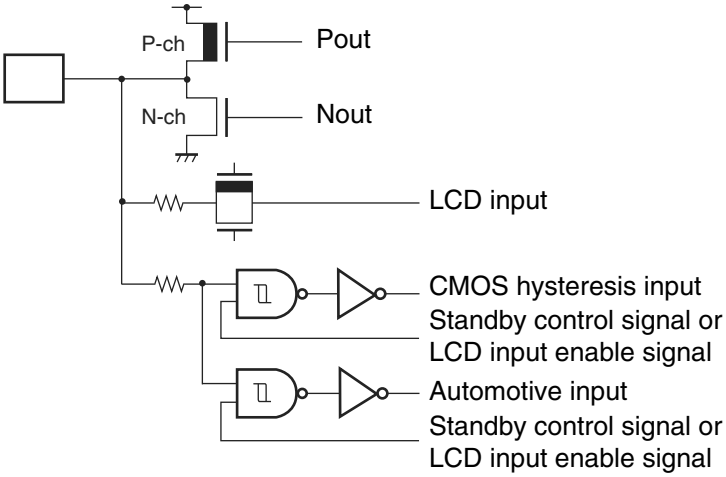
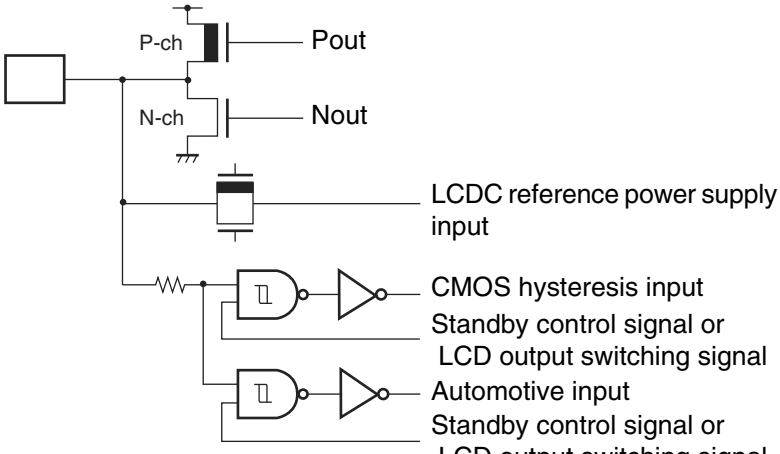
Type	Circuit	Remarks
E		Input-only pin (with pull-down resistance) • Attached pull-down resistance: approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.
F		LCD output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

■ HANDLING DEVICES

• Strictly observe maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC}, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

• Supply voltage stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

• Precautions when turning the power on

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μs.

• Handling unused pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

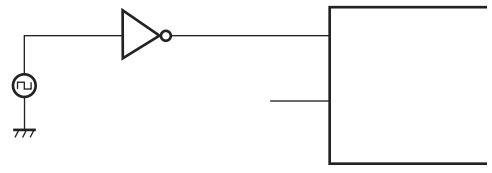
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

• Handling A/D converter power supply pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

• Notes on using an external clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

• **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

• **Crystal oscillator circuit**

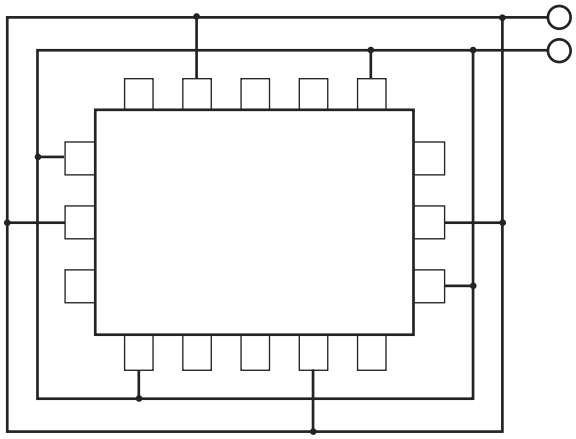
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



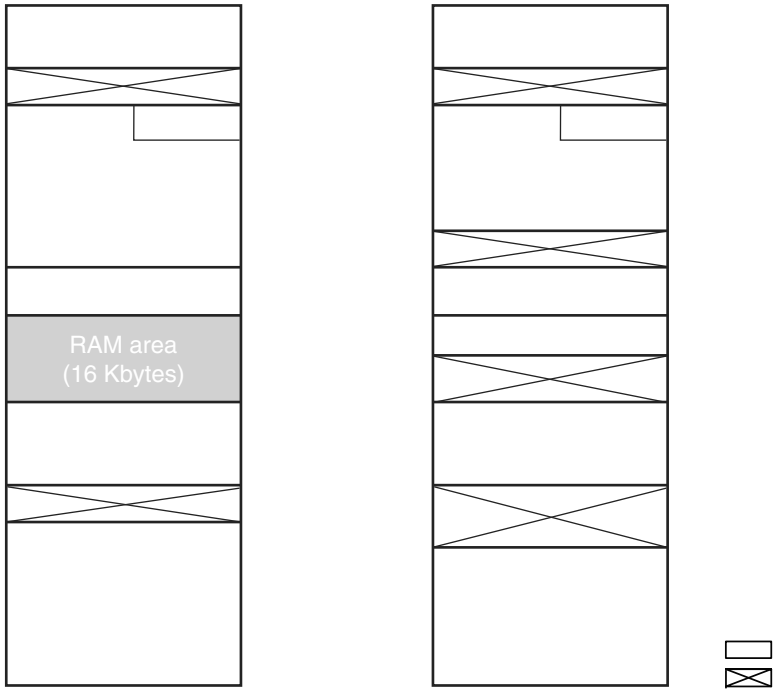
Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

• **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ MEMORY MAP



MB90F922 / MB90922
MB90F923 / MB90F924

Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000054H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000B
000055H	Higher timer control status register 1	TMCSR1H	R/W		XXX10000B
000056H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
000057H					XXXXXXXXB
000058H	LCD output control register 1	LOCR1	R/W	LCDC	11111111B
000059H	LCD output control register 2	LOCR2	R/W		00000000B
00005AH	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	00000000B
00005BH	Higher sound control register 0	SGCRH0	R/W		0XXXX100B
00005CH	Frequency data register 0	SGFR0	R/W		XXXXXXXXB
00005DH	Amplitude data register 0	SGAR0	R/W		00000000B
00005EH	Decrement grade register 0	SGDR0	R/W		XXXXXXXXB
00005FH	Tone count register 0	SGTR0	R/W		XXXXXXXXB
000060H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXXB
000061H					XXXXXXXXB
000062H	Input capture register 1	IPCP1	R		XXXXXXXXB
000063H					XXXXXXXXB
000064H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXXB
000065H					XXXXXXXXB
000066H	Input capture register 3	IPCP3	R		XXXXXXXXB
000067H					XXXXXXXXB
000068H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000B
000069H	Input capture edge register 0/1	ICE01	R/W		XXX0X0XXB
00006AH	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000B
00006BH	Input capture edge register 2/3	ICE23	R/W		XXXXXXXXB
00006CH	Lower LCD control register	LCRL	R/W	LCD controller/ driver	00010000B
00006DH	Higher LCD control register	LCRH	R/W		00000000B
00006EH	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	00111000B
00006FH	ROM mirror	ROMM	W	ROM mirror	XXXXXXX1B
000070H to 00007FH	Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS"				
000080H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	000000X0B
000081H	(Disabled)				
000082H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	000000X0B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111B
0000B1H	Interrupt control register 01	ICR01	R/W		00000111B
0000B2H	Interrupt control register 02	ICR02	R/W		00000111B
0000B3H	Interrupt control register 03	ICR03	R/W		00000111B
0000B4H	Interrupt control register 04	ICR04	R/W		00000111B
0000B5H	Interrupt control register 05	ICR05	R/W		00000111B
0000B6H	Interrupt control register 06	ICR06	R/W		00000111B
0000B7H	Interrupt control register 07	ICR07	R/W		00000111B
0000B8H	Interrupt control register 08	ICR08	R/W		00000111B
0000B9H	Interrupt control register 09	ICR09	R/W		00000111B
0000BAH	Interrupt control register 10	ICR10	R/W		00000111B
0000BBH	Interrupt control register 11	ICR11	R/W		00000111B
0000BCH	Interrupt control register 12	ICR12	R/W		00000111B
0000BDH	Interrupt control register 13	ICR13	R/W		00000111B
0000BEH	Interrupt control register 14	ICR14	R/W		00000111B
0000BFH	Interrupt control register 15	ICR15	R/W		00000111B
0000C0H to 0000C3H	(Disabled)				
0000C4H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000B
0000C5H	Serial control register 1	SCR1	R/W, W		00000000B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		00000000B
0000C7H	Serial status register 1	SSR1	R/W, R		00001000B
0000C8H	Extended communication control register 1	ECCR1	R/W, R		000000XXB
0000C9H	Extended status control register 1	ESCR1	R/W		00000100B
0000CAH	Baud rate generator register 10	BGR10	R/W		00000000B
0000CBH	Baud rate generator register 11	BGR11	R/W, R		00000000B
0000CCH	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0B
0000CDH	Middle watch timer control register	WTCRM	R/W		00000000B
0000CEH	Higher watch timer control register	WTCRH	R/W		XXXXXX00B
0000CFH	Sub clock control register	PSCCR	W	Sub clock	XXXX0000B
0000D0H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000B
0000D1H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXXB
0000D2H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000B
0000D3H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003944H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXXB
003945H					XXXXXXXXB
003946H	Input capture register 7	IPCP7	R		XXXXXXXXB
003947H					XXXXXXXXB
003948H to 00394FH	(Disabled)				
003950H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXXB
003951H					XXXXXXXXB
003952H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXXB
003953H					XXXXXXXXB
003954H to 003957H	(Disabled)				
003958H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXXB
003959H					XXXXXXXXB
00395AH					XXXXXXXXB
00395BH	Second data register	WTSR	R/W		XX000000B
00395CH	Minute data register	WTMR	R/W		XX000000B
00395DH	Hour data register	WTHR	R/W		XXX00000B
00395EH	Day data register	WTDR	R/W		00X00001B
00395FH	(Disabled)				
003960H	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXXB
003961H					XXXXXXXXB
003962H					XXXXXXXXB
003963H					XXXXXXXXB
003964H					XXXXXXXXB
003965H					XXXXXXXXB
003966H					XXXXXXXXB
003967H					XXXXXXXXB
003968H					XXXXXXXXB
003969H					XXXXXXXXB
00396AH					XXXXXXXXB
00396BH					XXXXXXXXB
00396CH					XXXXXXXXB
00396DH					XXXXXXXXB
00396EH					XXXXXXXXB
00396FH					XXXXXXXXB

(Continued)

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

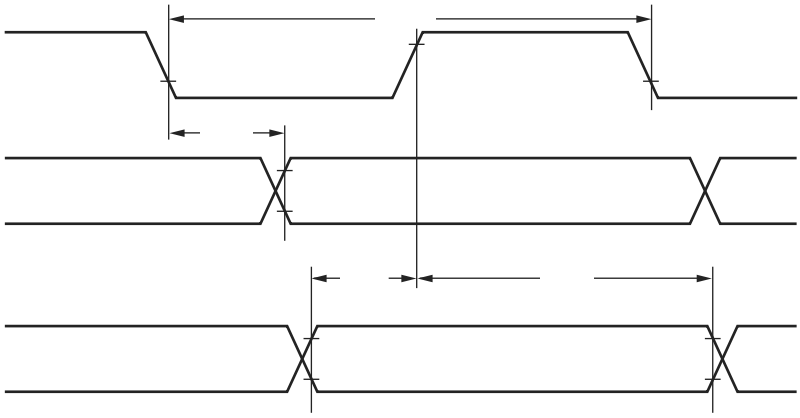
List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003C00H	003D00H	003E00H	003F00H	Control status register	CSR	R/W, R	00---000B 0----0-1B
003C01H	003D01H	003E01H	003F01H				
003C02H	003D02H	003E02H	003F02H	Last event indicator register	LEIR	R/W	--------B 000-0000B
003C03H	003D03H	003E03H	003F03H				
003C04H	003D04H	003E04H	003F04H	RX/TX error counter	RTEC	R	00000000B 00000000B
003C05H	003D05H	003E05H	003F05H				
003C06H	003D06H	003E06H	003F06H	Bit timing register	BTR	R/W	-1111111B 11111111B
003C07H	003D07H	003E07H	003F07H				

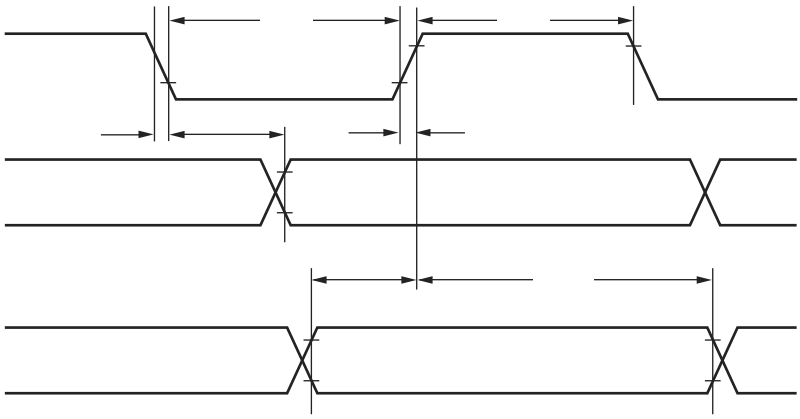
(Continued)

Address				Register	Abbre-viation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
003A40H	003B40H	003740H	003840H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003A41H	003B41H	003741H	003841H				
003A42H	003B42H	003742H	003842H				XXXXX---B XXXXXXXXB
003A43H	003B43H	003743H	003843H				
003A44H	003B44H	003744H	003844H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003A45H	003B45H	003745H	003845H				
003A46H	003B46H	003746H	003846H				XXXXX---B XXXXXXXXB
003A47H	003B47H	003747H	003847H				
003A48H	003B48H	003748H	003848H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003A49H	003B49H	003749H	003849H				
003A4AH	003B4AH	00374AH	00384AH				XXXXX---B XXXXXXXXB
003A4BH	003B4BH	00374BH	00384BH				
003A4CH	003B4CH	00374CH	00384CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
003A4DH	003B4DH	00374DH	00384DH				
003A4EH	003B4EH	00374EH	00384EH				XXXXX---B XXXXXXXXB
003A4FH	003B4FH	00374FH	00384FH				
003A50H	003B50H	003750H	003850H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003A51H	003B51H	003751H	003851H				
003A52H	003B52H	003752H	003852H				XXXXX---B XXXXXXXXB
003A53H	003B53H	003753H	003853H				
003A54H	003B54H	003754H	003854H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003A55H	003B55H	003755H	003855H				
003A56H	003B56H	003756H	003856H				XXXXX---B XXXXXXXXB
003A57H	003B57H	003757H	003857H				
003A58H	003B58H	003758H	003858H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003A59H	003B59H	003759H	003859H				
003A5AH	003B5AH	00375AH	00385AH				XXXXX---B XXXXXXXXB
003A5BH	003B5BH	00375BH	00385BH				
003A5CH	003B5CH	00375CH	00385CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
003A5DH	003B5DH	00375DH	00385DH				
003A5EH	003B5EH	00375EH	00385EH				XXXXX---B XXXXXXXXB
003A5FH	003B5FH	00375FH	00385FH				

- Internal shift clock mode



- External shift clock mode



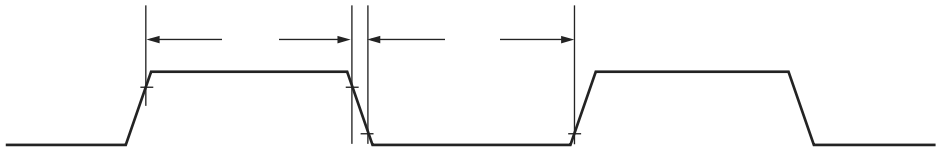
(6) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to “ (1) Clock timing”.

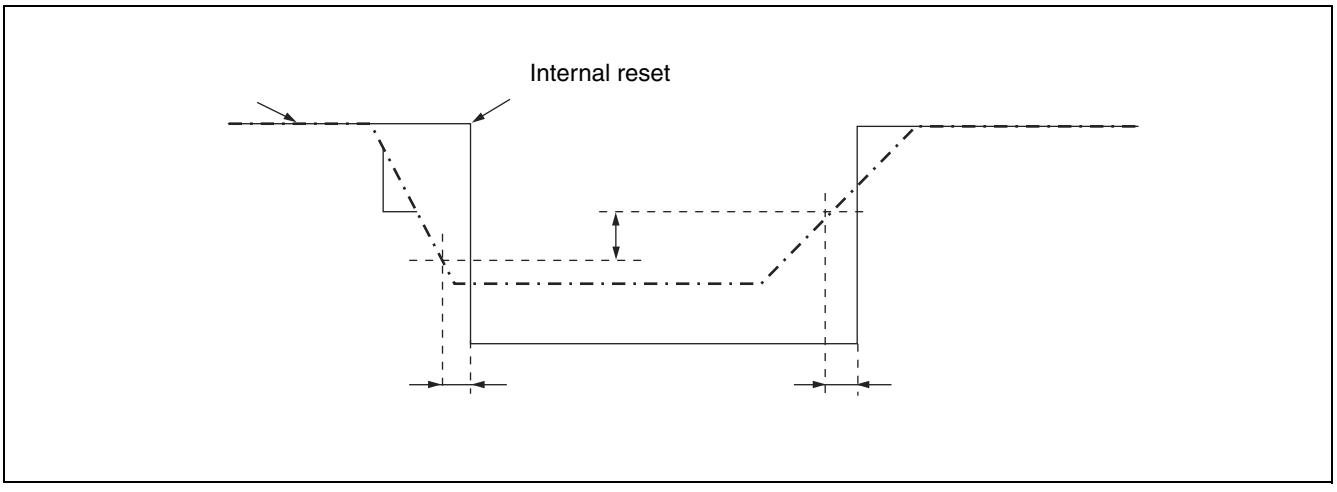
- Trigger input timing



(7) Low voltage detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

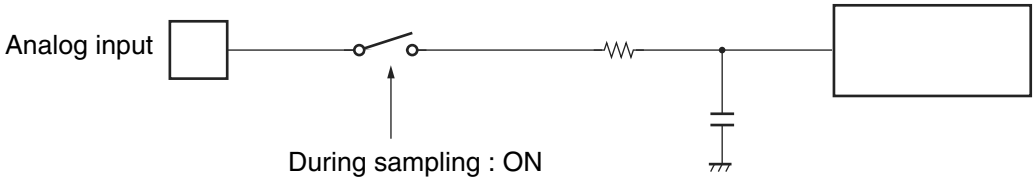
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V_{DL}	VCC	—	4.0	4.2	4.4	V	Flash memory product, during voltage drop
				3.7	4.0	4.3	V	Evaluation product, during voltage drop
Hysteresis width	V_{HYS}	VCC	—	190	—	—	mV	Flash memory product, during voltage rise
				0.1	—	—	V	Evaluation product, during voltage rise
Power supply voltage change rate	dV/dt	VCC	—	– 0.1	—	+ 0.1	V/µs	Flash memory product, dV/dt at low voltage reset
				–0.004	—	+ 0.004	V/µs	Flash memory product, dV/dt at standard value of low voltage detection/release voltage
				– 0.1	—	+ 0.02	V/µs	Evaluation product
Detection delay time	td	—	—	—	—	3.2	µs	Flash memory product, when dV/dt ≤ 0.004 V/µs
				—	—	35	µs	Evaluation product



• **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	12.1 kΩ (Max)	8.5 pF (Max)

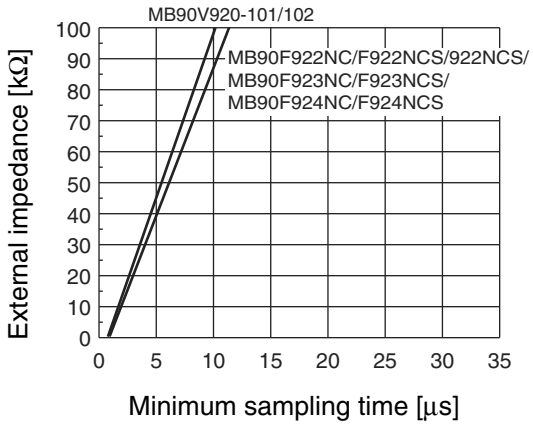
MB90V920-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

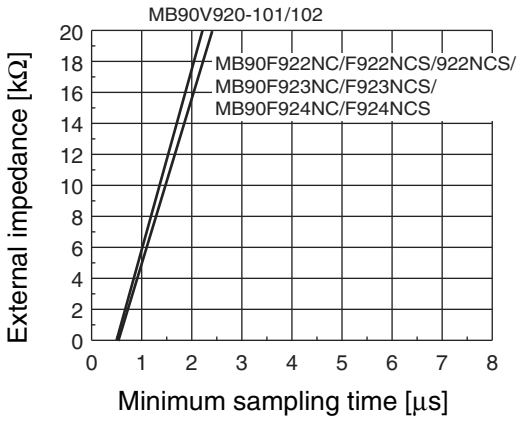
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

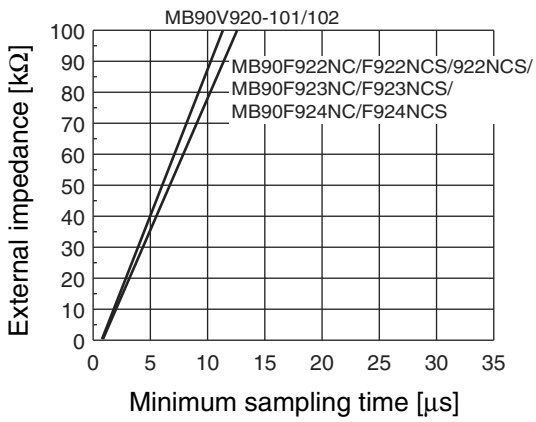


(External impedance = 0 kΩ to 20 kΩ)

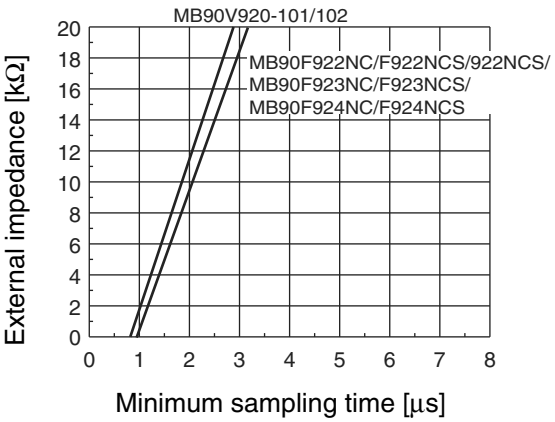


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
  As |AVRH - AVSS| becomes smaller, the relative errors grow larger.