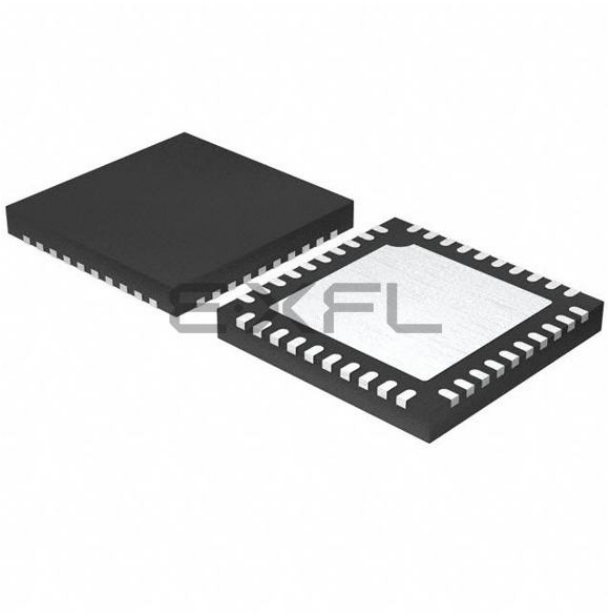

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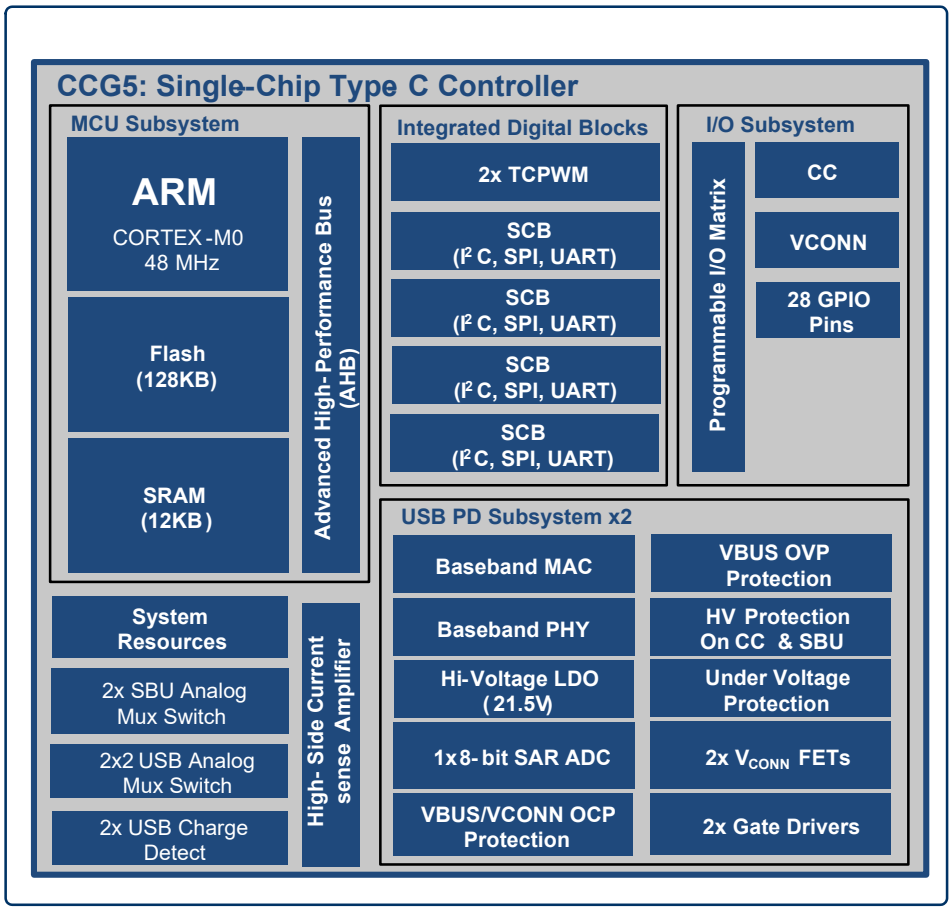
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	12K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	28
Voltage - Supply	2.75V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd5125-40lqxit

Logic Block Diagram



Contents

VCONN FET

CCG5 has two power supply inputs, V5V_P1 and V5V_P2 pins, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs for each PD port to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on the CC1 and CC2 pins for the EMCA cables. CCG5 also supports integrated OCP on VCONN.

ADC

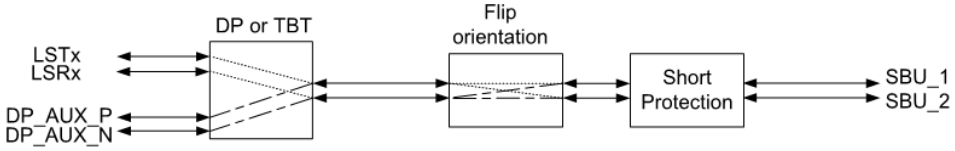
The USB-PD subsystem contains one 8-bit successive approximation register (SAR) for analog-to-digital conversions (ADC). The ADCs include an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip have access to the ADCs through the chip-wide analog mux bus. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux bus.

SBU Mux

The SBU switch mux contains 2x1 Mux and a single 2x2 cross bar SBU switch per the Type-C port. The 2x1 MUX enables you to select between the Display Port or Thunderbolt alternate mode and the single-ended 2x2 switch enables you to route signals to the appropriate SBU1/2 based on CC (Type-C plug) orientation.

The AUX port of the SBU switch supports only differential signals. Non-differential signals on the AUX port cause signal coupling at the output of the SBU switch. The LS port of the SBU switch supports both non-differential and differential signals.

Figure 2. CCG5 SBU Crossbar Switch Block Diagram



USB HS Mux

The HS Mux contains a 2×2 cross bar switch to route the system D± lines to the Type-C top or bottom ports based on the CC (Type-C plug) orientation. The unused D± top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

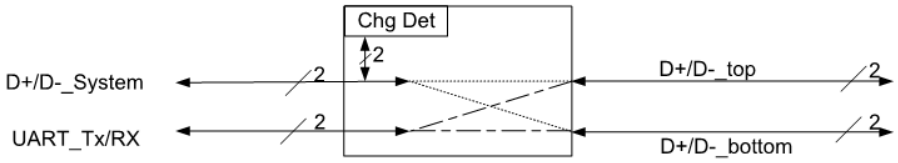
The HS Mux also contains charger detection/emulation for detecting USB BC 1.2 (source only) and Apple terminations. The charger detection block is connected to the D± from the system as shown in Figure 3.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- Trace lengths of HS signals shall be no more than 2 inches from the USB 2.0 host to the CCG5 device. Similarly, trace length from the CCG5 device to Type-C connector pins shall be no more than 2 inches.
- The differential impedance across the DP/DM signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

Increasing the trace length by more than 2 inches on either side of the CCG5 device degrades the HS eye diagram.

Figure 3. CCG5 DP/DM Switch Block Diagram



Overvoltage and Undervoltage Protection on VBUS

CCG5 implements an undervoltage/overvoltage (UV/OV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detector have programmable thresholds and is controlled by the firmware.

Overcurrent Protection on VBUS

CCG5 integrates a high-side current sense amplifier to detect overcurrent on the VBUS. Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor connected between the “CSP_Px” and “CSN_Px” pins.

VBUS Discharge

CCG5 also has integrated VBUS discharge FETs and resistors for each port. It is used to discharge VBUS to meet the USB-PD specification timing on a detach condition and negative voltage transition.

VBUS Regulator

CCG5 can operate from three power supplies – V_{SYS}, V_{BUS_P1}, and V_{BUS_P2}. CCG5 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The V_{SYS} always takes priority over VBUS_P1/VBUS_P2. In the absence of V_{SYS}, the regulator powers CCG5 either from VBUS_P1 or VBUS_P2.

PFET Gate Driver for VBUS

CCG5 supports the consumer-side and provider-side external power FET Drivers for PFET. The VBUS_P_CTRL and VBUS_C_CTRL gate drivers can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

Charger Detect

CCG5 integrates battery charger emulation and detection for USB BC.1.2, Apple charge (source only).

IEC Compliant VBUS, CC, D±, and SBU Lines

The chip supports IEC-compliant ESD protection on VBUS, CC, D±, and SBU lines.

High-Voltage Tolerant SBU and CC Lines

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG5 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG5 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG5 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

SRAM

CCG5 supports 12-KB SRAM.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG5 has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a Master/slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG5 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 2, SCB 3 and SCB 4 blocks of EZ-PD CCG5 are not completely compliant with the I^2C spec in the following:

- The GPIO cells for SCB 2 to SCB 4 I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 10-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG5 has up to two TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (TCPWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG5 has 28 GPIOs that includes the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from only SCB 1 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI

Group Name	Pin Name	Port	Ball Location	Description
USB Type-C Port 1	CC1_P1	Analog	K2	USB PD connector detect/Configuration Channel 1
	CC2_P1	Analog	H2	USB PD connector detect/Configuration Channel 2
USB Type-C Port 2	CC1_P2	Analog	K9	USB PD connector detect/Configuration Channel 1
	CC2_P2	Analog	K10	USB PD connector detect/Configuration Channel 2
MUX Type-C Port 1	AUX_P_P1	Analog	B11	Auxiliary signal for DisplayPort
	AUX_N_P1	Analog	C11	Auxiliary signal for DisplayPort
	LSRX_P1	Analog	A11	Thunderbolt Link Management UART Rx
	LSTX_P1	Analog	A10	Thunderbolt Link Management UART Tx
	SBU1_P1	Analog	A3	Sideband Use signal
	SBU2_P1	Analog	A4	Sideband Use signal
	DMINUS_SYS_P1	Analog	A7	USB 2.0 DM from the Host System
	DPLUS_SYS_P1	Analog	A6	USB 2.0 DP from the Host System
	UART_RX_P1/GPIO	P4.1	A9	UART Rx from Host System/GPIO
	UART_TX_P1/GPIO	P4.0	A8	UART Tx from Host system/GPIO
	DMINUS_BOT_P1	Analog	C1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P1	Analog	B1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P1	Analog	A2	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP_P1	Analog	A1	USB 2.0 DP from Top of Type-C Connector
MUX Type-C Port 2	AUX_P_P2	Analog	D11	Auxiliary signal for DisplayPort
	AUX_N_P2	Analog	E11	Auxiliary signal for DisplayPort
	LSRX_P2	Analog	L11	Thunderbolt Link Management UART Rx
	LSTX_P2	Analog	K11	Thunderbolt Link Management UART Tx
	SBU1_P2	Analog	E1	Sideband Use signal
	SBU2_P2	Analog	F1	Sideband Use signal
	DMINUS_SYS_P2	Analog	G11	USB 2.0 DM from the Host System
	DPLUS_SYS_P2	Analog	F11	USB 2.0 DP from the Host System
	UART_RX_P2/GPIO	P0.2	J11	UART Rx from Host System/GPIO
	UART_TX_P2/GPIO	P0.1	H11	UART Tx from Host system/GPIO
	DMINUS_BOT_P2	Analog	L1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P2	Analog	K1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P2	Analog	H1	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP_P2	Analog	G1	USB 2.0 DP from Top of Type-C Connector
VBUS Control Type-C Port1	VBUS_P_CTRL_P1	Analog	K3	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF
	VBUS_C_CTRL_P1	Analog	K4	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF

Application Diagrams

Figure 8 and Figure 9 illustrate the Dual Type-C Port and Single Type-C port Thunderbolt Notebook DRP application diagrams using a CCG5 device respectively. The Type-C port can be used as a power provider/power consumer.

The CCG5 device communicates with the embedded controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of the internal battery. It also updates the Thunderbolt Controller via I^2C to route the High-speed signals coming from the Type-C port to the USB host (during normal mode) or the Graphics processor unit (during Display port Alternate mode) or the Thunderbolt Host (during Thunderbolt Alternate mode) based on the alternate mode negotiation.

For the dual Type-C notebook application (Figure 8), these Type-C ports can be power providers or power consumers simultaneously. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the USB Host controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the Link management. CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

The CCG5 device has an integrated VCONN FET for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. The 10 mΩ resistor between the 5 V supply and FETs is used for overcurrent detection on the VBUS. The VBUS_P_CTRL pin of CCG5 has an in-built VBUS monitoring circuit that can detect OVP and UVP on VBUS.

CCG5 also has an in-built VBUS discharge circuit that is used to quickly discharge VBUS after the Type-C connection is detached. The internal resistance (as listed in Table 41) of this VBUS discharge circuit is expected to be sufficient for typical CCG5 applications. However, customers can include an optional VBUS discharge circuit as shown in Figure 7 using any available GPIO. This optional circuit can be added to the design if the discharge time using the in-built VBUS discharge circuit needs to be further reduced; that is, VBUS transition time from higher to lower voltages can be further reduced using the external VBUS discharge circuit shown in Figure 7. This optional external circuit comprises of a N-channel MOSFET and the CCG5 device can be used to enable or disable it as appropriate.

Figure 7. Optional External VBUS Discharge Circuit

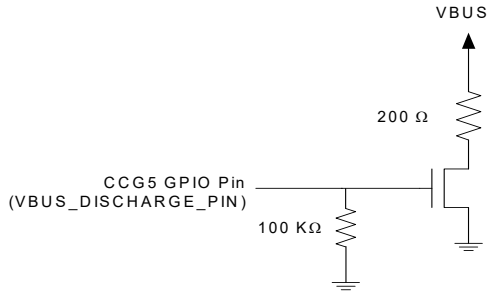


Figure 9 illustrates a Single Port Thunderbolt Notebook DRP application diagram using CYPD5125-40LQXIT.

Figure 9. CCG5 in a Single Port Notebook Application using CYPD5125-40LQXIT

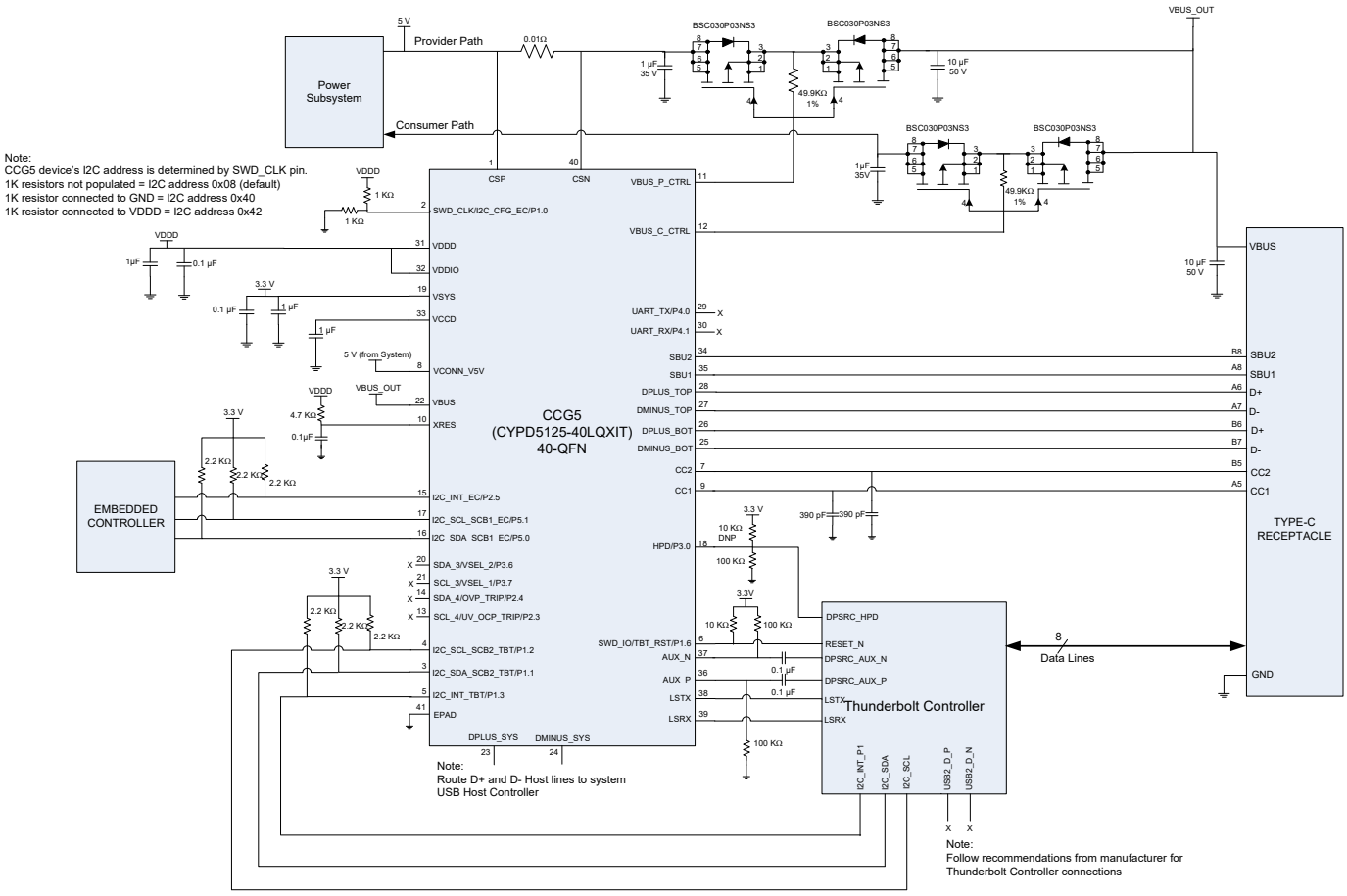
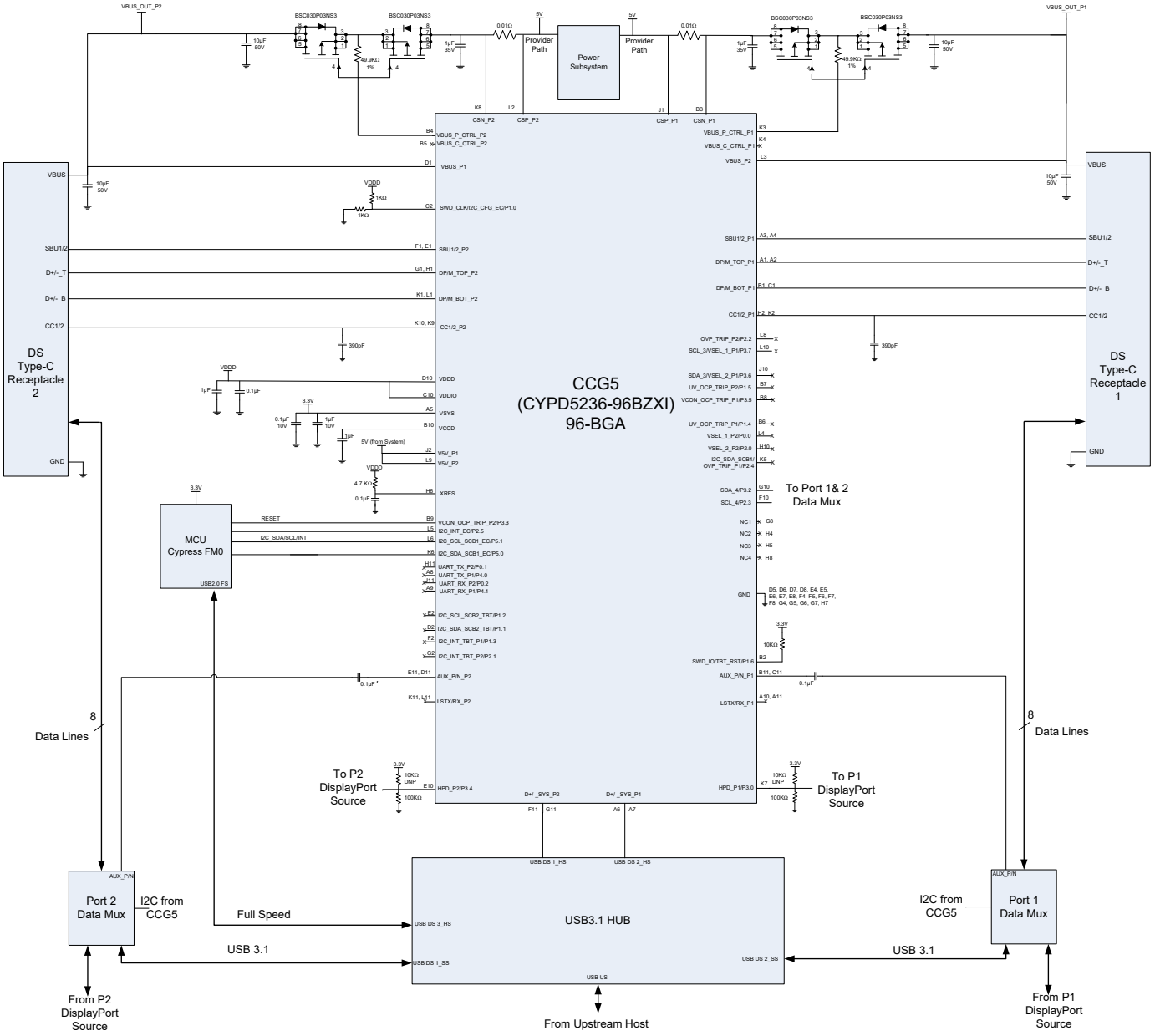


Figure 11 illustrates the Dual Type-C Port dock downstream application diagram using a CCG5 device. The CCG5 negotiates power contract with the connected device on the downstream Type-C port and controls the power system. It also controls the data mux via I^2C based on the alternate mode negotiation to source USB SuperSpeed and/or DisplayPort on the downstream Type-C port. As mentioned above, CCG5 device offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

Figure 11. CCG5 in a Dual port Dock Downstream Port Application using CYPD5236-96BXZI



Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings[3]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–	–	6	V	Absolute max
$V_{5V\_P1\_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{5V\_P2\_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_P1\_MAX}$	Max VBUS voltage relative to Vss	–	–	24	V	
$V_{BUS\_P2\_MAX}$	Max VBUS voltage relative to Vss	–	–	24	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	V_{DDD}	V	
V_{GPIO_ABS}	Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (AUX, LS, SBU1/2 pins)	–0.5	–	V_{DDIO} + 0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	Applicable for all pins except SBU pins
ESD_HBM_SBU[4]	Electrostatic discharge human body model for SBU1, SBU2 pins	1100	–	–	V	Only applicable to SBU pins
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2, contact discharge	8000	–	–	V	Contact Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2, air discharge	15000	–	–	V	Air Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
VCC_PIN_ABS	Max voltage on CC1 and CC2 pins	–	–	24	V	Absolute max
VSBU_PIN_ABS	Max voltage on SBU1 and SBU2 pins	–	–	24	V	
VGPIO_OVT_ABS	OVT GPIO voltage	–0.5	–	6	V	Absolute maximum for OVT pins K6 and L6 of BGA, pins 16 and 17 of QFN

Notes
3. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
4. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

Table 26. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.cc_shvt.1	vSwing	Transmitter Output High Voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter Output Low Voltage		–	0.075	V	–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.cc_shvt.4	zBmcRx	Receiver Input Impedance	10	–		MΩ	Guaranteed by design
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	165.6	–	194.4	µA	–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	303.6	–	356.4	µA	–
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery (upstream facing port)	4.08	–	6.12	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7	V	–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31	V	–
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.30	FS_0p53	Voltage threshold for Fast Swap Detect	0.49	–	0.58	V	–

Analog to Digital Converter

Table 27. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generate from bandgap

SBU

Table 35. SBU Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.20sbu.1	Ron1	On resistances for Aux switch at 3.3 V input	–	4	7	Ω	–
SID.DC.20sbu.2	Ron2	On resistances for Aux switch at 1 V input	–	3	5	Ω	–
SID.DC.20sbu.4	Ileak1	Pin leakage current for SBU1, SBU2	–4.5	–	4.5	µA	–
SID.DC.20sbu.5	Ileak2	Pin leakage current for LSTX, LSRX, AUX_P, AUX_N	–1	–	1	µA	–
SID.DC.20sbu.6	Rpu_aux_1	Pull-up resistance on AUX_P/N	80	–	320	KΩ	–
SID.DC.20sbu.7	Rpu_aux_2	Pull-up resistance on AUX_P/N	0.8	–	1.4	MΩ	–
SID.DC.20sbu.8	Rpd_aux_1	Pull-down resistance on AUX_P/N	80	–	120	KΩ	–
SID.DC.20sbu.9	Rpd_aux_2	Pull-down resistance on AUX_P/N	0.3	–	1.2	MΩ	–
SID.DC.20sbu.10	Rpd_aux_3	Pull-down resistance on AUX_P/N	250	–	611	KΩ	–
SID.DC.20sbu.11	Rpd_aux_4	Pull-down resistance on AUX_P/N	0.3	–	6.11	MΩ	–
SID.DC.20sbu.16	OVP_threshold	Over-voltage protection detection threshold above V_{DDIO}	200	–	1200	mV	–
SID.DC.20sbu.17	lsx_ron_3p3	On resistances of LSTX/LSRX to SBU1/2 switch at 3.3 V input	–	8.5	17	Ω	–
SID.DC.20sbu.18	lsx_ron_1	On resistances of LSTX/LSRX to SBU1/2 switch at 1 V input	–	5.5	11	Ω	–
SID.DC.20sbu.19	aux_ron_flat_fs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V)	–	–	2.5	Ω	Guaranteed by design
SID.DC.20sbu.20	aux_ron_flat_hs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design
SID.DC.20sbu.21	lsx_ron_flat_fs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V)	–	–	5	Ω	Guaranteed by design
SID.DC.20sbu.22	lsx_ron_flat_hs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design

Table 36. SBU Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20sbu.1	Con	Switch ON capacitance	–	–	120	pF	–
SID.AC.20sbu.2	Coff	Switch OFF capacitance - Connector side	–	–	80	pF	–
SID.AC.20sbu.3	Off_isolation	Switch isolation at F = 1 MHz	–50	–		dB	–
SID.AC.20sbu.4	T_{ON}	SBU Switch turn-on time	–	–	200	µs	–
SID.AC.20sbu.5	T_{OFF}	SBU Switch turn-off time	–	–	400	µs	Guaranteed by design
SID.AC.20sbu.6	Off_isolation_tran	Coupling on sbu1,2 terminated to 50 ohm, switch-OFF, Rail-to-rail toggling on LSTX/LSRX	–60	–	60	mV	Guaranteed by design
SID.AC.20sbu.7	X_talk_AC	Cross talk of Switch at F=1 MHz SBU1/2 to SBU2/1	–50	–	–	dB	Guaranteed by design
SID.AC.20sbu.8	X_talk_tran	Check voltage coupling on SBU2(1) when Data is transferred from LSTX (RX) to SBU1 (2)	–70	–	70	mV	Guaranteed by design

Table 37. DP/DM Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.dpdm.1	Ron_HS	DPDM On resistance for SYS lines (0 to 0.5 V) - HS mode	–	–	8	Ω	–
SID.DC.dpdm.2	Ron_FS	DPDM On resistance for SYS lines (0 to 3.3 V) - FS mode	–	–	12	Ω	–
SID.DC.dpdm.5	Con_FS	Switch On capacitance at FS at 6 MHz	–	–	50	pF	Guaranteed by design
SID.DC.dpdm.6	Con_HS	Switch on capacitance at HS at 240 MHz	–	–	10	pF	–
SID.DC.dpdm.9	Ileak_pin	pin leakage at DP/DM connector side and host side	–	–	1	µA	–
SID.DC.dpdm.10	RON_UART	DPDM On resistance for UART lines (0 to 3.3 V)	–	–	17	Ω	–
SID.DC.dpdm.11	RON_FLAT_HS	DPDM On Flat resistance in HS mode (0 to 0.4 V)	–	–	0.5	Ω	Guaranteed by design
SID.DC.dpdm.12	RON_FLAT_FS	DPDM On flat resistance in FS mode (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design
SID.DC.dpdm.13	RON_FLAT_UART	DPDM UART On flat resistance (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design

Table 38. DP/DM Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.dpdm.5	T_{ON}	DP/DM Switch turn-on time	–	–	200	µs	–
SID.AC.dpdm.6	T_{OFF}	DP/DM Switch turn-off time	–	–	0.4	µs	Guaranteed by design
SID.AC.dpdm.7	T_{ON_VPUMP}	DP/DM charge pump startup time	–	–	200	µs	Guaranteed by characterization
SID.AC.dpdm.8	Off_isolation_HS	Switch-off isolation for HS	–20	–	–	db	Guaranteed by design
SID.AC.dpdm.9	Off_isolation_FS	Switch-off isolation for FS	–50	–	–	db	Guaranteed by design
SID.AC.dpdm.10	X_talk	Cross talk of Switch From FS to HS at F = 12 MHz	–50	–	–	db	Guaranteed by design
SID.AC.dpdm.11	uart_coupling	peak to peak coupling of UART signal to DP lines. (UART swinging from 0 to 3.3 V)	–	–	20	mV	Guaranteed by design

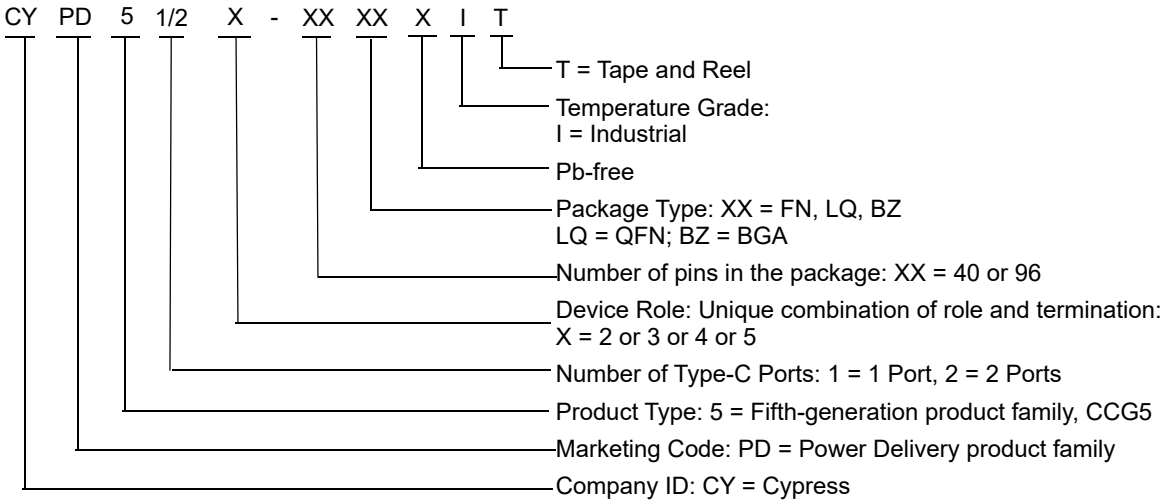
Ordering Information

Table 42 lists the EZ-PD CCG5 part numbers and features.

Table 42. EZ-PD CCG5 Ordering Information

Part Number	Application	Type-C Ports	Dead Battery Termination	Termination Resistor	Role	Package
CYPD5125-40LQXIT	Notebooks, Desktops	1	Yes	R_P[5], R_D[6], R_{D-DB}[7]	DRP	40-pin QFN
CYPD5135-40LQXIT	Dock	1	No	R_P[5], R_D[6]	DRP	40-pin QFN
CYPD5225-96BZXI	Notebooks, Desktops	2	Yes	R_P[5], R_D[6], R_{D-DB}[7]	DRP	96-ball BGA
CYPD5225-96BZXIT						
CYPD5235-96BZXI	Dock, Upstream port	2	No	R_P[5], R_D[6]	DRP	96-ball BGA
CYPD5235-96BZXIT						
CYPD5236-96BZXI	Dock, Downstream port	2	No	R_P[5], R_D[6]	DRP	96-ball BGA
CYPD5236-96BZXIT						

Ordering Code Definitions



Notes
5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting an accessory or upstream facing port.
7. Termination resistor denoting dead-battery termination.

Packaging

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
T_{JA}	Package θ_{JA} (96-ball BGA)	–	–	–	56	°C/W
T_{JC}	Package θ_{JC} (96-ball BGA)	–	–	–	18.5	°C/W
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	19.3	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	13.6	°C/W

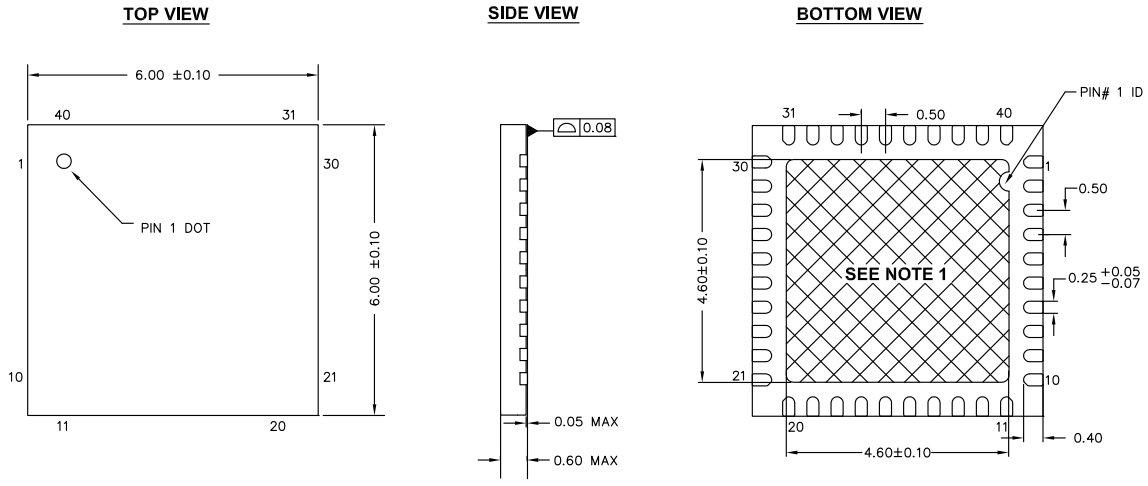
Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
96-ball BGA	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
96-ball BGA	MSL 3
40-pin QFN	MSL 3

Figure 12. 40-Pin QFN (6 × 6 × 0.6 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659

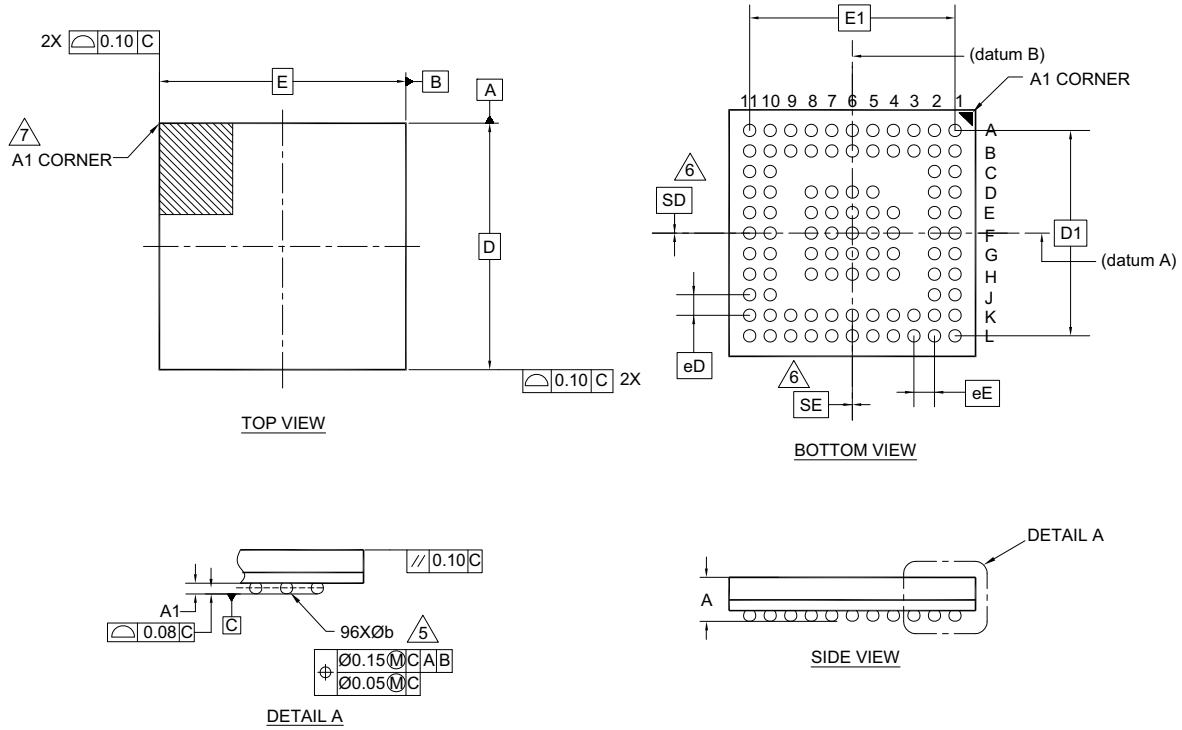


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 13. 96-Ball BGA (6 × 6 × 1.0 mm), Package Outline, 002-10631



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	96		
∅ b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-225.

002-10631 *A

Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
BOD	Brown out Detect
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG5 pins used to connect to a USB port
XRES	external reset I/O pin

Document History Page

Document Title: EZ-PD™ CCG5, USB Type-C Port Controller Document Number: 002-17682				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5528106	SOBI	12/07/2016	New datasheet
*A	5606273	SOBI	01/27/2017	Updated EZ-PD™ CCG5, USB Type-C Port Controller and Features. Updated Logic Block Diagram. Updated USB-PD Subsystem (SS) and reordered the Functional Overview section. Updated GPIO. Updated 40-Pin QFN Pin Map (Top View) for CYPD5125-40LQXIT.
*B	5694572	SOBI	06/03/2017	Changed datasheet status to Preliminary. Added Errata. Added Table 4 through Table 7. Added Table 9 through Table 41 in Device-Level Specifications. Updated Logic Block Diagram, GPIO, and VBUS Discharge. Updated Table 2, Table 3, Table 8, and Table 46. Updated Figure 5 through Figure 9. Updated Figure 13 (spec 002-10631 Rev. ** to *A) in Packaging. Updated compliance with USB spec in Sales, Solutions, and Legal Information. Updated template.

*C	5885413	VGT	09/27/2017	Updated USB HS Mux and SBU Mux in Functional Overview.
				Updated Flash in CPU and Memory Subsystem.
				Updated Power System Overview.
				Updated description of BGA pin P2.4 to support SCB4 I2C data.
				Changed SID.PWR#1_A; VDDD from 3 V to 3.15 V for DFP application.
				Changed SID.AC.dpdm.3; Trise_HS from 630 ps max to 300 ps min.
				Changed SID.AC.dpdm.4, Tfall_HS from 630 ps max to 300 ps min.
				Updated SID.PWR#23 - changed V_{SYS} to V_{SYS_UFP} and changed range to 2.7 to 5.5 V.
				Added SID.PWR#23_A for DFP/DRP application.
				Changed max value for SID.20VREG.8, $V_{BUSLOADREG}$, from 0.2 to 0.3.
				Updated SID.ADC.2, SID.ADC.4 to ±1.5.
				Updated SID.PWR#18 description to extend to SBU, DPDM mux pins.
				Updated SID.PWR#2 - changed V_{DDD_MAX} to V_{SYS_MAX}.
				Removed min value from SID.PWR#14, VDDIO_MAX.
				Added min spec of -25mA for SID.PWR#19, Igpio_abs.
				Removed ADC.AC spec.
				Updated SID.DC.20vconn.11, OVP_hysteresis max.
				Added SID.DC.20vconn.14, OVP_threshold_on.
				Added SID.AC.dpdm.10, SID.AC.dpdm.11.
				Changed min value of SID.AC.dpdm.1, BW_3dB_HS from 1000 to 700.
				Changed max value of SID.DC.dpdm.12, SID.DC.dpdm.13 from 4 to 3.
				Changed max value of SID.DC.dpdm.2, RON_FS to 12.
				Corrected values for SID.AC.dpdm.8, SID.AC.dpdm.9.
				Added SID.AC.20sbu.6, SID.AC.20sbu.8, and SID.AC.20sbu.8.

Document Title: EZ-PD™ CCG5, USB Type-C Port Controller Document Number: 002-17682				
*C (contd.)	5885413	VGT	09/27/2017	Updated SID.DC.20sbu.12, SID.DC.20sbu.15, SID.DC.20sbu.6, SID.DC.20sbu.7, SID.DC.20sbu.7A, SID.DC.20sbu.8, SID.DC.20sbu.9, SID.DC.20sbu.10, SID.DC.20sbu.11, SID.DC.20sbu.3, and SID.DC.20sbu.3. Changed SBU pins ESD voltage to 750 V. Added new Table 28, new Table 29, Table 43 through Table 45. Updated Figure 5, Figure 8, Figure 9. Added Figure 7. Removed ADC AC specifications and CSA AC specifications (Table 28 and Table 32 from previous revision). Removed Errata.
*D	5943992	VGT	10/24/2017	Added "Thunderbolt hosts and devices" in Applications. Updated Figure 1 to correctly depict "2 x ADC" for entire CCG5. Updated description of VDDD pin in Table 2 and Table 3. Updated the description for pin P2.4 in Table 3. Added "CYPD5235-96BZXI" and "CYPD5236-96BZXI" part numbers to the description of Table 3 and Figure 6. Updated $V_{BUS\_P1\_MAX}$ and $V_{BUS\_P2\_MAX}$ values to 24 in Table 8. Updated min value of ESD_HBM_SBU spec from 750 to 1100 V in Table 8. Added "Applicable for all pins except SBU pins" in description of "ESD_HBM" parameter in Table 8. Updated description of $V_{GPIO\_OVT\_ABS}$ in Table 8. Updated description of ESD_IEC_CON and ESD_IEC_AIR parameters in Table 8. Changed SID.PWR#13 min value from 1.7 to V_{DDD} in Table 9. Updated min value of SID.PWR#23 to 2.75 in Table 9. Updated pin description, values, and details/conditions of parameters SID.PWR#1 and SID.PWR#1_A to better define V_{DDD} supply in Table 9. Replace V_{DDD} with V_{SYS} in supply name and conditions for IDD parameters listed in Table 9. Updated Conditions for SID.CLK#4 to “All V_{DDD}” in Table 10. Removed SID.PWR#20 in Table 10. Added Guaranteed by Design for SID178 and SID180 in Table 20. Added description for SID.MEM#8 in Table 20. Added description for SID.CLK#13 and SID.CLK#13A in Table 24. Added Guaranteed by Design for SID.DC.cc_shvt.4 in Table 26. Deleted details and conditions for SID.DC.cc_shvt.14 in Table 26. Removed SID.DC.cc_SHVT.19 in Table 26. Updated spec values in Table 32. Added Guaranteed by Design for SID.AC.PGDO.2 in Table 34. Added Guaranteed by Design for SID.DC.20sbu.19 through SID.DC.20sbu.22 and removed SID.AC.20sbu.3 in Table 35. Added Guaranteed by Design for SID.AC.20SBU.5 in Table 36. Updated max value for SID.AC.20SBU.8 in Table 36. Removed SID.DC.dpdm.3 and SID.DC.dpdm.4 and added Guaranteed by Design for SID.DC.dpdm.5 and SID.DC.dpdm.11 through SID.DC.dpdm.13 in Table 37. Updated SID.DC.dpdm.12 and SID.DC.dpdm.13 max value in Table 37. Removed SID.AC.dpdm.1, SID.AC.dpdm.2, SID.AC.dpdm.3, and SID.AC.dpdm.4 in Table 38.

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