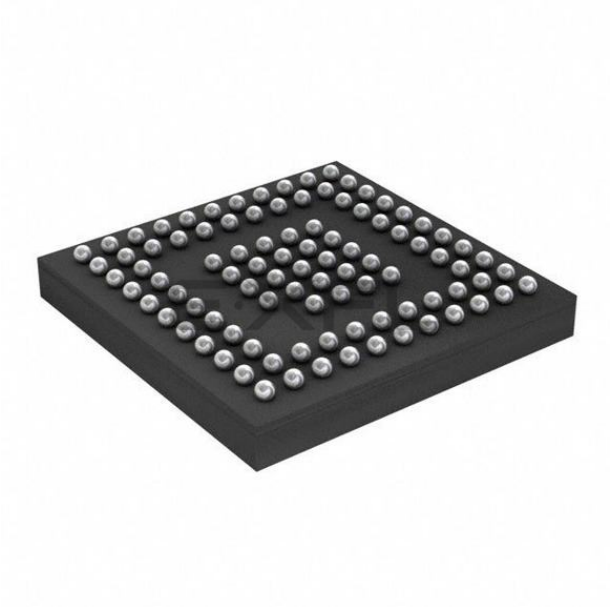

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	12K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	28
Voltage - Supply	2.75V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	96-VFBGA
Supplier Device Package	96-BGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd5236-96bzxi

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VBUS Regulator

CCG5 can operate from three power supplies – V_{SYS}, V_{BUS_P1}, and V_{BUS_P2}. CCG5 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The V_{SYS} always takes priority over VBUS_P1/VBUS_P2. In the absence of V_{SYS}, the regulator powers CCG5 either from VBUS_P1 or VBUS_P2.

PFET Gate Driver for VBUS

CCG5 supports the consumer-side and provider-side external power FET Drivers for PFET. The VBUS_P_CTRL and VBUS_C_CTRL gate drivers can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

Charger Detect

CCG5 integrates battery charger emulation and detection for USB BC.1.2, Apple charge (source only).

IEC Compliant VBUS, CC, D±, and SBU Lines

The chip supports IEC-compliant ESD protection on VBUS, CC, D±, and SBU lines.

High-Voltage Tolerant SBU and CC Lines

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG5 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG5 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG5 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

SRAM

CCG5 supports 12-KB SRAM.

Pinouts

Table 2. Pinout for CYPD5125-40LQXIT

Group Name	Pin Name	Port	Pin	Description
USB Type-C	CC1	Analog	9	USB PD connector detect/Configuration Channel 1
	CC2	Analog	7	USB PD connector detect/Configuration Channel 2
Mux	DPLUS_SYS	Analog	23	USB 2.0 DP from the Host System
	DMINUS_SYS	Analog	24	USB 2.0 DM from the Host System
	UART_TX/GPIO	P4.0	29	UART TX from Host System/GPIO
	UART_RX/GPIO	P4.1	30	UART RX from Host System/GPIO
	DPLUS_BOT	Analog	26	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_BOT	Analog	25	USB 2.0 DM from Bottom of Type-C Connector
	DMINUS_TOP	Analog	27	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP	Analog	28	USB 2.0 DP from Top of Type-C Connector
	SBU2	Analog	34	Sideband Use signal
	SBU1	Analog	35	Sideband Use signal
	AUX_P	Analog	36	Auxiliary signal for DisplayPort
	AUX_N	Analog	37	Auxiliary signal for DisplayPort
	LSTX	Analog	38	Thunderbolt Link Management UART Rx
	LSRX	Analog	39	Thunderbolt Link Management UART Tx
VBUS Control	VBUS_P_CTRL	Analog	11	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF
	VBUS_C_CTRL	Analog	12	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C port1 0: Path ON High Z: Path OFF
VBUS OCP	CSP	Analog	1	Current Sense positive Input for VBUS side external Rsense
	CSN	Analog	40	Current sense negative for other side of external Rsense
GPIOs and Serial Interfaces	SWD_IO/AR_RST/GPIO	P1.6	6	SWD I/O/GPIO
	SWD_CLK/I2C_CFG_EC/ GPIO	P1.0	2	SWD Clock/ I^2C config line. I^2C config line is used to select the I^2C address of HPI interface. The state of line decides the 7 bit I^2C address for HPI. I^2C Config Line Floating: 0x08 Pulled up with 1 KW: 0x42 Pulled down with 1 KW: 0x40
	I2C_SDA_SCB2_TBT/GPIO	P1.1	3	SCB2 I^2C Data/GPIO
	I2C_SCL_SCB2_TBT/GPIO	P1.2	4	SCB2 I^2C Clock/GPIO
	I2C_INT_TBT/GPIO	P1.3	5	TBT interrupt for port 1/GPIO
	OVP_TRIP/I2C_SDA_SCB4/GPIO	P2.4	14	VBUS overvoltage output indicator for port 1/SCB4 I^2C Data
	UV_OCP_TRIP/I2C_SCL_SCB4/GPIO	P2.3	13	VBUS undervoltage or OCP Output Indicator for Port1 / SCB4 I^2C Clock / GPIO
	I2C_SDA_SCB1_EC/GPIO	P5.0	16	SCB1 I^2C Data / GPIO
	I2C_SCL_SCB1_EC/GPIO	P5.1	17	SCB1 I^2C Clock / GPIO
	I2C_INT_EC/GPIO	P2.5	15	Embedded Controller interrupt/GPIO
	HPD/GPIO	P3.0	18	Hot Plug Detect I/O for port 1/GPIO
	I2C_SDA_SCB3 / GPIO / VSEL_2	P3.6	20	SCB3 I^2C Data or GPIO or voltage selection control for VBUS
	I2C_SCL_SCB3 / GPIO /VSEL_1	P3.7	21	SCB3 I^2C Clock or GPIO or voltage selection control for VBUS
Reset	XRES	Analog	10	Reset input (Active LOW)

Table 2. Pinout for CYPD5125-40LQXIT *(continued)*

Group Name	Pin Name	Port	Pin	Description
Power	VBUS	Power	22	VBUS Input for Port 1 (4 V to 21.5 V)
	VSYS	Power	19	2.75 V to 5.5 V supply for the system
	VDDD	Power	31	VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V 2. VBUS powered - 3.15 V to 3.6 V
	VDDIO	Power	32	At system-level short the VDDD to VDDIO
	VCCD	Power	33	1.8 V regulator output for filter capacitor. This pin cannot drive external load.
	V5V	Power	8	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1
Ground	VSS	Ground	EPAD	Ground

Figure 5. 40-Pin QFN Pin Map (Top View) for CYPD5125-40LQXIT

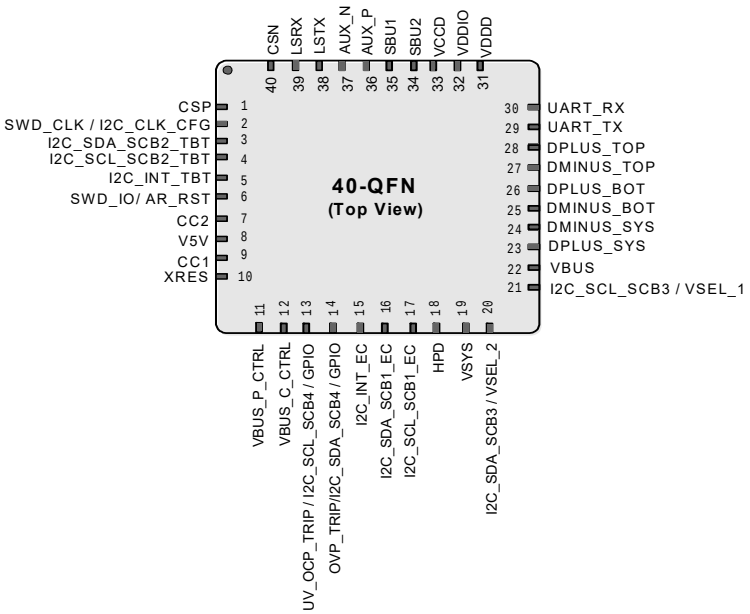


Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI

Group Name	Pin Name	Port	Ball Location	Description
USB Type-C Port 1	CC1_P1	Analog	K2	USB PD connector detect/Configuration Channel 1
	CC2_P1	Analog	H2	USB PD connector detect/Configuration Channel 2
USB Type-C Port 2	CC1_P2	Analog	K9	USB PD connector detect/Configuration Channel 1
	CC2_P2	Analog	K10	USB PD connector detect/Configuration Channel 2
MUX Type-C Port 1	AUX_P_P1	Analog	B11	Auxiliary signal for DisplayPort
	AUX_N_P1	Analog	C11	Auxiliary signal for DisplayPort
	LSRX_P1	Analog	A11	Thunderbolt Link Management UART Rx
	LSTX_P1	Analog	A10	Thunderbolt Link Management UART Tx
	SBU1_P1	Analog	A3	Sideband Use signal
	SBU2_P1	Analog	A4	Sideband Use signal
	DMINUS_SYS_P1	Analog	A7	USB 2.0 DM from the Host System
	DPLUS_SYS_P1	Analog	A6	USB 2.0 DP from the Host System
	UART_RX_P1/GPIO	P4.1	A9	UART Rx from Host System/GPIO
	UART_TX_P1/GPIO	P4.0	A8	UART Tx from Host system/GPIO
	DMINUS_BOT_P1	Analog	C1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P1	Analog	B1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P1	Analog	A2	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP_P1	Analog	A1	USB 2.0 DP from Top of Type-C Connector
MUX Type-C Port 2	AUX_P_P2	Analog	D11	Auxiliary signal for DisplayPort
	AUX_N_P2	Analog	E11	Auxiliary signal for DisplayPort
	LSRX_P2	Analog	L11	Thunderbolt Link Management UART Rx
	LSTX_P2	Analog	K11	Thunderbolt Link Management UART Tx
	SBU1_P2	Analog	E1	Sideband Use signal
	SBU2_P2	Analog	F1	Sideband Use signal
	DMINUS_SYS_P2	Analog	G11	USB 2.0 DM from the Host System
	DPLUS_SYS_P2	Analog	F11	USB 2.0 DP from the Host System
	UART_RX_P2/GPIO	P0.2	J11	UART Rx from Host System/GPIO
	UART_TX_P2/GPIO	P0.1	H11	UART Tx from Host system/GPIO
	DMINUS_BOT_P2	Analog	L1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P2	Analog	K1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P2	Analog	H1	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP_P2	Analog	G1	USB 2.0 DP from Top of Type-C Connector
VBUS Control Type-C Port1	VBUS_P_CTRL_P1	Analog	K3	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF
	VBUS_C_CTRL_P1	Analog	K4	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF

Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI *(continued)*

Group Name	Pin Name	Port	Ball Location	Description
VBUS Control Type-C Port2	VBUS_P_CTRL_P2	Analog	B4	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 2. 0: Path ON High Z: Path OFF
	VBUS_C_CTRL_P2	Analog	B5	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 2. 0: Path ON High Z: Path OFF
VBUS OCP	CSP_P1	Analog	J1	Current Sense Positive Input for P1
	CSN_P1	Analog	B3	Current Sense Negative Input for P1
	CSP_P2	Analog	L2	Current Sense Positive Input for P2
	CSN_P2	Analog	K8	Current Sense Negative Input for P2
GPIOs and Serial Interfaces	GPIO	P3.1	L7	GPIO
	I2C_S-DA_SCB4/OVP_TRIP_P1/GPIO	P2.4	K5	VBUS overvoltage output indicator for Port 1 / SCB4 I2C Data/ GPIO
	OVP_TRIP_P2 / GPIO	P2.2	L8	VBUS overvoltage output indicator for Port 2 / GPIO
	VSEL_1_P2 / GPIO	P0.0	L4	Voltage selection control for VBUS on Port 2 / GPIO
	UV_OCP_TRIP_P1/GPIO	P1.4	B6	VBUS undervoltage of OCP output indicator for Port 1/GPIO
	HPD_P1/GPIO	P3.0	K7	Hot Plug Detect I/O for Port 1 /GPIO
	HPD_P2/GPIO	P3.4	E10	Hot Plug Detect I/O for Port 2 /GPIO
	VCONN_OCP_TRIP_P2/ GPIO	P3.3	B9	VCONN OCP output indicator for Port 2 / GPIO
	VCONN_OCP_TRIP_P1/GPIO	P3.5	B8	VCONN OCP output indicator for Port 1/ GPIO
	UV_OCP_TRIP_P2/GPIO	P1.5	B7	VBUS undervoltage or OCP output indicator for Port 2/GPIO
	VSEL_2_P2 / GPIO	P2.0	H10	Voltage selection control for VBUS on Port 2 / GPIO
	I2C_SCL_SCB1_EC/ GPIO	P5.1	L6	SCB1 I^2C Clock
	I2C_SDA_SCB1_EC/ GPIO	P5.0	K6	SCB1 I^2C Data
	I2C_INT_EC/GPIO	P2.5	L5	I^2C interrupt line
	I2C_SCL_SCB2_TBT/GPIO	P1.2	E2	SCB2 I^2C Clock/GPIO
	I2C_SDA_SCB2_TBT/GPIO	P1.1	D2	SCB2 I^2C Data /GPIO
	I2C_INT_TBT_P1/GPIO	P1.3	F2	I^2C interrupt line/GPIO
	I2C_INT_TBT_P2/GPIO	P2.1	G2	I^2C interrupt line
	I2C_SCL_SCB3 / VSEL_1_P1 /GPIO	P3.7	L10	SCB3 I^2C Clock/ Voltage selection control for VBUS on Port 1/ GPIO
	I2C_SDA_SCB3 / VSEL_2_P1 / GPIO	P3.6	J10	SCB3 I^2C Data / Voltage selection control for VBUS on Port 1 /GPIO
	I2C_SCL_SCB4/GPIO	P2.3	F10	SCB4 I^2C Clock /GPIO
	I2C_SDA_SCB4/GPIO	P3.2	G10	SCB4 I^2C Data /GPIO
	SWD_IO/AR_RST# /GPIO	P1.6	B2	SWD I/O / AR Reset / GPIO
	SWD_CLK/I2C_CFG_EC/GPIO	P1.0	C2	SWD Clock / I^2C config line / GPIO. I^2C config line is used to select the I^2C address of HPI interface. The state of line decides the 7 bit I^2C address for HPI. I^2C Config Line Floating: 0x08 Pulled up with 1 KW: 0x42 Pulled down with 1 KW: 0x40
Reset	XRES	Analog	H6	Reset input (Active LOW)

Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI *(continued)*

Group Name	Pin Name	Port	Ball Location	Description
Power	VBUS_P1	Power	D1	VBUS Input for Port 1 (4 V to 21.5 V)
	VBUS_P2	Power	L3	VBUS Input for Port 2 (4 V to 21.5 V)
	VSYS	Power	A5	2.75 V to 5.5 V supply for the system
	VDDD	Power	D10	VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V 2. VBUS powered - 3.15 V to 3.6 V
	VCCD	Power	B10	1.8 V regulator output for filter capacitor. This pin cannot drive external load.
	VDDIO	Power	C10	At system-level short the VDDD to VDDIO
	V5V_P1	Power	J2	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1
	V5V_P2	Power	L9	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 2
Ground	GND	Ground	D5	Ground
	GND	Ground	D6	Ground
	GND	Ground	D7	Ground
	GND	Ground	D8	Ground
	GND	Ground	E4	Ground
	GND	Ground	E5	Ground
	GND	Ground	E6	Ground
	GND	Ground	E7	Ground
	GND	Ground	E8	Ground
	GND	Ground	F4	Ground
	GND	Ground	F5	Ground
	GND	Ground	F6	Ground
	GND	Ground	F7	Ground
	GND	Ground	F8	Ground
	GND	Ground	G4	Ground
	GND	Ground	G5	Ground
	GND	Ground	G6	Ground
	GND	Ground	G7	Ground
	GND	Ground	H7	Ground
No Connect	NC	DNU	G8	Not Connect
	NC	DNU	H4	Not Connect
	NC	DNU	H5	Not Connect
	NC	DNU	H8	Not Connect

Figure 8. CCG5 in a Dual Port Notebook Application using CYPD5225-96BZXI

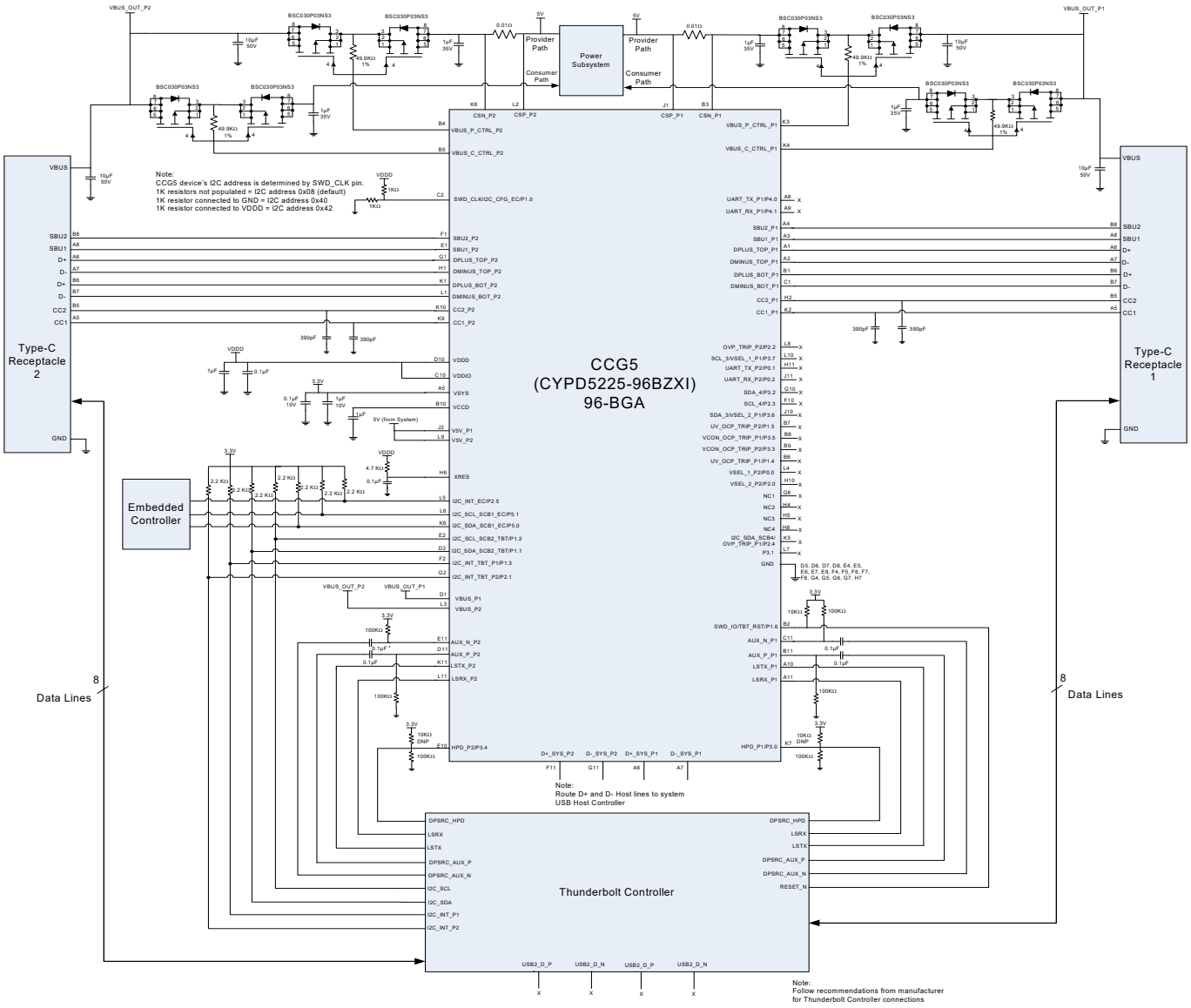


Figure 9 illustrates a Single Port Thunderbolt Notebook DRP application diagram using CYPD5125-40LQXIT.

Figure 9. CCG5 in a Single Port Notebook Application using CYPD5125-40LQXIT

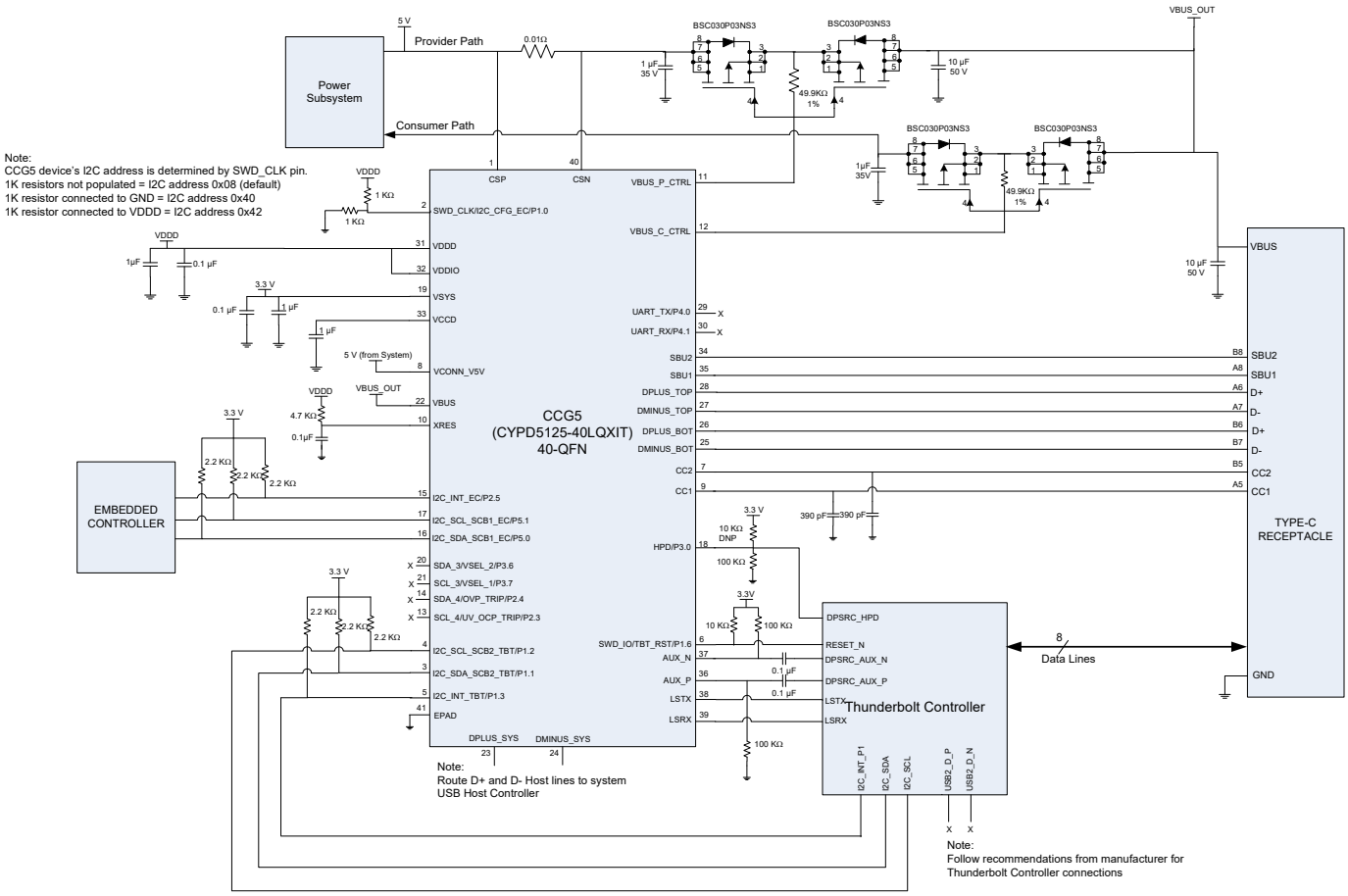


Figure 10 illustrates the Dual Type-C Port Thunderbolt device/dock upstream application diagram using a CCG5 device. The CCG5 device communicates with the power system over I²C, which manages the power provided to the upstream Type-C ports. It also updates the Thunderbolt Controller over I²C based on the alternate mode negotiation to sink Thunderbolt or USB or DisplayPort Data. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the Thunderbolt Controller and Billboard controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the link management. As mentioned in Features, CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

Figure 10. CCG5 in a Dual port Thunderbolt Device/Dock Upstream Port Application using CYPD5235-96BXZI

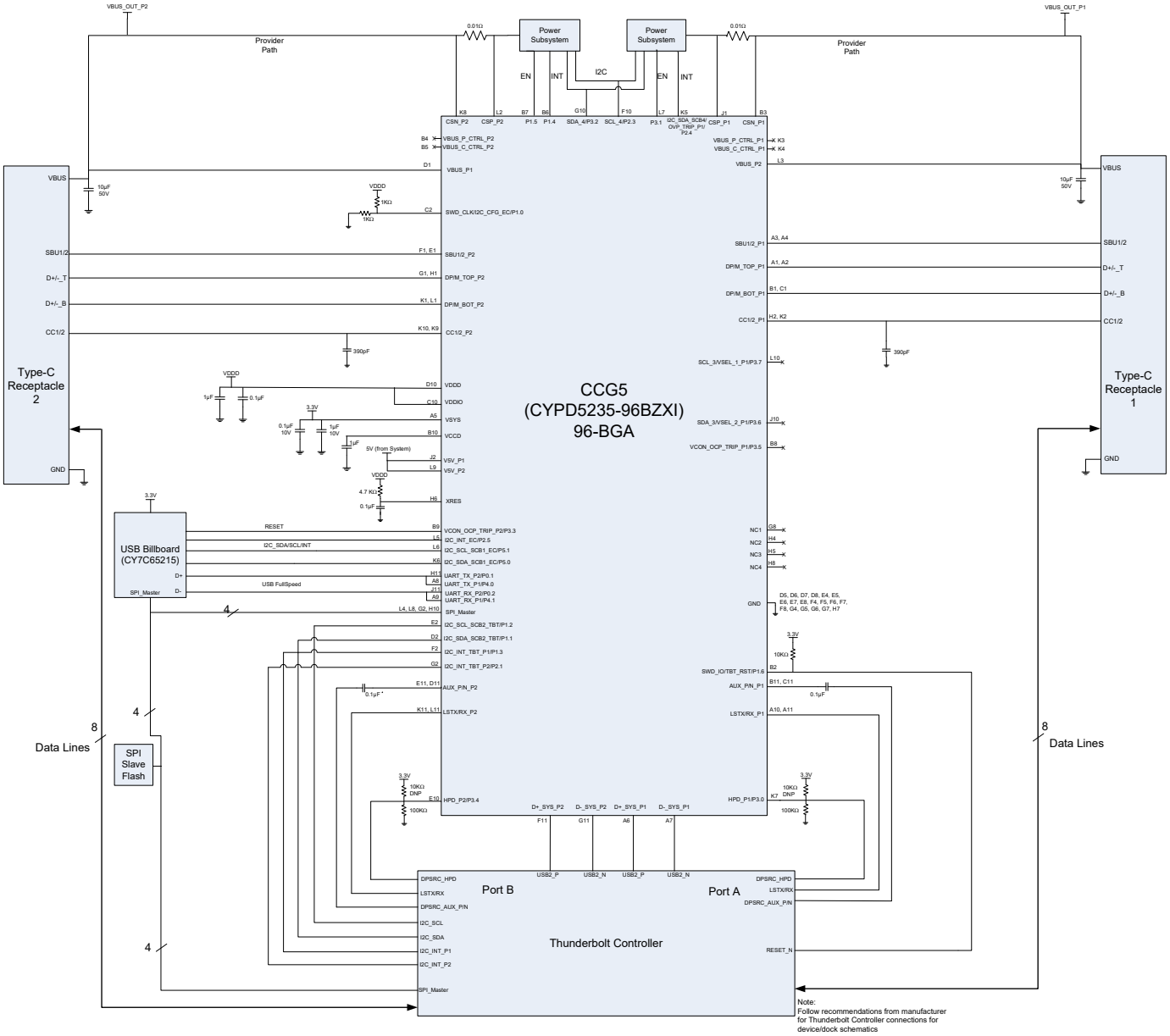
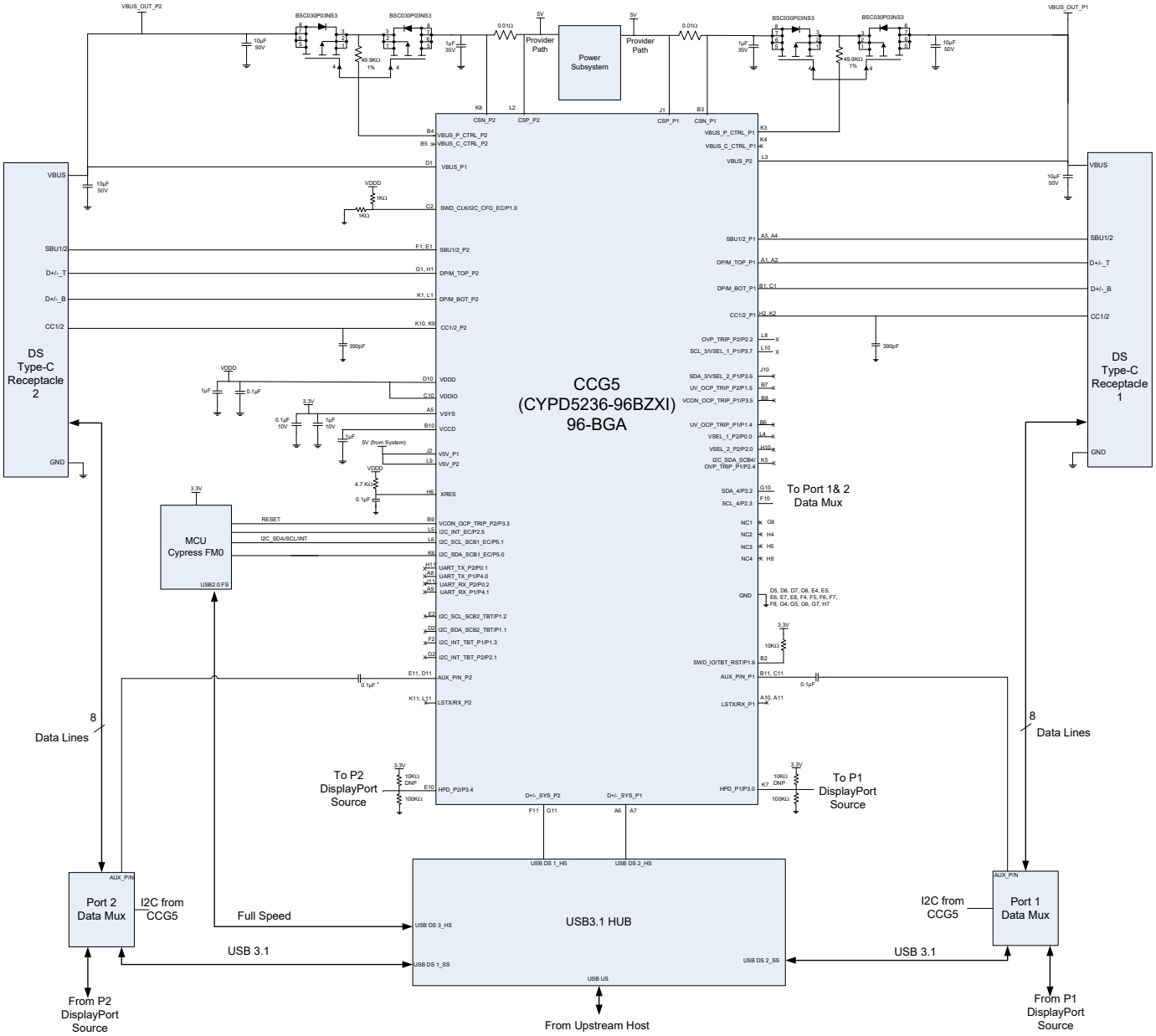


Figure 11 illustrates the Dual Type-C Port dock downstream application diagram using a CCG5 device. The CCG5 negotiates power contract with the connected device on the downstream Type-C port and controls the power system. It also controls the data mux via I^2C based on the alternate mode negotiation to source USB SuperSpeed and/or DisplayPort on the downstream Type-C port. As mentioned above, CCG5 device offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

Figure 11. CCG5 in a Dual port Dock Downstream Port Application using CYPD5236-96BXZI



Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings[3]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–	–	6	V	Absolute max
$V_{5V_P1_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{5V_P2_MAX}$	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS_P1_MAX}$	Max VBUS voltage relative to Vss	–	–	24	V	
$V_{BUS_P2_MAX}$	Max VBUS voltage relative to Vss	–	–	24	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	V_{DDD}	V	
V_{GPIO_ABS}	Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (AUX, LS, SBU1/2 pins)	–0.5	–	V_{DDIO} + 0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	Applicable for all pins except SBU pins
ESD_HBM_SBU[4]	Electrostatic discharge human body model for SBU1, SBU2 pins	1100	–	–	V	Only applicable to SBU pins
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2, contact discharge	8000	–	–	V	Contact Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2, air discharge	15000	–	–	V	Air Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
VCC_PIN_ABS	Max voltage on CC1 and CC2 pins	–	–	24	V	Absolute max
VSBU_PIN_ABS	Max voltage on SBU1 and SBU2 pins	–	–	24	V	
VGPIO_OVT_ABS	OVT GPIO voltage	–0.5	–	6	V	Absolute maximum for OVT pins K6 and L6 of BGA, pins 16 and 17 of QFN

Notes

3. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
4. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

Table 10. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	All V_{DDD}
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	Guaranteed by characterization
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	
SYS.FES#1	$T_{_PWR_RDY}$	Power-up to "Ready to accept I^2C/CC command"	–	5	25	ms	

Table 11. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	$0.7 \times V_{DDIO}$	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	$0.3 \times V_{DDIO}$	V	CMOS input
SID.GIO#39	$V_{IH_VDDIO2.7-}$	LVTTL input, $V_{DDIO} < 2.7$ V	$0.7 \times V_{DDIO}$	–	–	V	–
SID.GIO#40	$V_{IL_VDDIO2.7-}$	LVTTL input, $V_{DDIO} < 2.7$ V	–	–	$0.3 \times V_{DDIO}$	V	–
SID.GIO#41	$V_{IH_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq 2.7$ V	2.0	–	–	V	–
SID.GIO#42	$V_{IL_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq 2.7$ V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	$V_{DDIO} - 0.6$	–	–	V	$I_{OH} = -4$ mA at 3 V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	$V_{DDIO} - 0.5$	–	–	V	$I_{OH} = -1$mA at 1.8 V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 4$ mA at 1.8 V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 10$ mA (IOL_LED) at 3 V V_{DDIO}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDIO}
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL	15	40	–	mV	$V_{DDIO} > 2.7$ V. Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDIO}$	–	–	mV	$V_{DDIO} < 4.5$ V
SID.GIO#44A	$V_{HYSCMOS55}$	Input hysteresis CMOS	200	–	–	mV	$V_{DDIO} > 4.5$ V

Table 12. I/O AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, $C_{load} = 25$ pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, $C_{load} = 25$ pF
SID.GIO#46	T_{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, $C_{load} = 25$ pF
SID.GIO#47	T_{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, $C_{load} = 25$ pF
SID.GIO#48	F_{GPIO_OUT1}	GPIO F_{OUT}; $3.3\ V \leq V_{DDIO} \leq 5.5$ V. Fast Strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#49	F_{GPIO_OUT2}	GPIO F_{OUT}; $1.7\ V \leq V_{DDIO} \leq 3.3$ V. Fast Strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#50	F_{GPIO_OUT3}	GPIO F_{OUT}; $3.3\ V \leq V_{DDIO} \leq 5.5$ V. Slow Strong mode.	–	–	7	MHz	90/10%, 25 pF load

Table 26. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.cc_shvt.1	vSwing	Transmitter Output High Voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter Output Low Voltage		–	0.075	V	–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.cc_shvt.4	zBmcRx	Receiver Input Impedance	10	–		MΩ	Guaranteed by design
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	165.6	–	194.4	µA	–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	303.6	–	356.4	µA	–
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery (upstream facing port)	4.08	–	6.12	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7	V	–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31	V	–
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.30	FS_0p53	Voltage threshold for Fast Swap Detect	0.49	–	0.58	V	–

Analog to Digital Converter

Table 27. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generate from bandgap

Charger Detect

Table 28. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.CHGDET.1	VDAT_REF	Data detect voltage in charger detect mode	250	–	400	mV	–
DC.CHGDET.2	VDM_SRC	Dn voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.3	VDP_SRC	Dp voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.4	IDM_SINK	Dn sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.5	IDP_SINK	Dp sing current in charger detect mode	25	–	175	µA	–
DC.CHGDET.6	IDP_SRC	Data contact detect current source	7	–	13	µA	–
DC.CHGDET.27	RDP_UP	Qualcomm pull-up termination on Dp/Dn	0.9	–	1.575	kΩ	–
DC.CHGDET.32	RDM_UP	Dp/Dn pull-up resistance	0.9	–	1.575	kΩ	–
DC.CHGDET.28	RDP_DWN	Qualcomm pull-down termination on Dp/Dn	14.25	–	24.8	kΩ	–
DC.CHGDET.31	RDM_DWN	Dp/Dn pull-down resistance	14.25	–	24.8	kΩ	–
DC.CHGDET.29	RDAT_LKG	Data line leakage on Dp/Dn	300	–	500	kΩ	–
DC.CHGDET.34	VSETH	Logic Threshold	1.26	–	1.54	V	–

Table 29. V_{BUS} Regulator AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20VREG.1	T_{START}	Total start up time for the regulator supply outputs	–	–	120	µs	Apply V_{BUS} and measure start time on V_{DDD} pin.
SID.AC.20VREG.2	T_{STOP}	Regulator power down time from vreg_en = 0 to regulator disable	–	–	1	µs	Time from assertion of an internal disable signal to for load current on V_{DDD} to decrease from 30 mA to 10 µA.

Table 30. V_{SYS} Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.VDDDSW.1	Res_sw	Resistance from supply input to output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA to 10 mA on V_{DDD}.

Table 31. CSA DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.CSA.21	Out_E_Trim_15_DS	Cumulative output Error for Av = 15, after trim, using Deep sleep (beta-multiplier) reference	–7	–	7	%	–
SID.DC.CSA.22	Out_E_Trim_15_BG	Cumulative output Error for Av = 15, after trim, using bandgap reference	–4.5	–	4.5	%	–
SID.DC.CSA.23	Out_E_Trim_100_DS	Cumulative output Error for Av = 100, after trim, using Deep sleep (beta-multiplier) reference	–24.5	–	24.5	%	–

Table 32. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy in active mode using bandgap reference	–	±3	–	%	–
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy in Deep Sleep mode using Deep Sleep reference	–	±5	–	%	–
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4s	–15	–	15	mV	–

Table 33. PFET Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.PGDO.1	R_{pd}	Resistance when “pull_dn” enabled	–	–	5	kΩ	–

Table 34. PFET Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.PGDO.2	$T_{r_discharge}$	Discharge Rate of output note	–	–	5	V/µs	Guaranteed by design

SBU

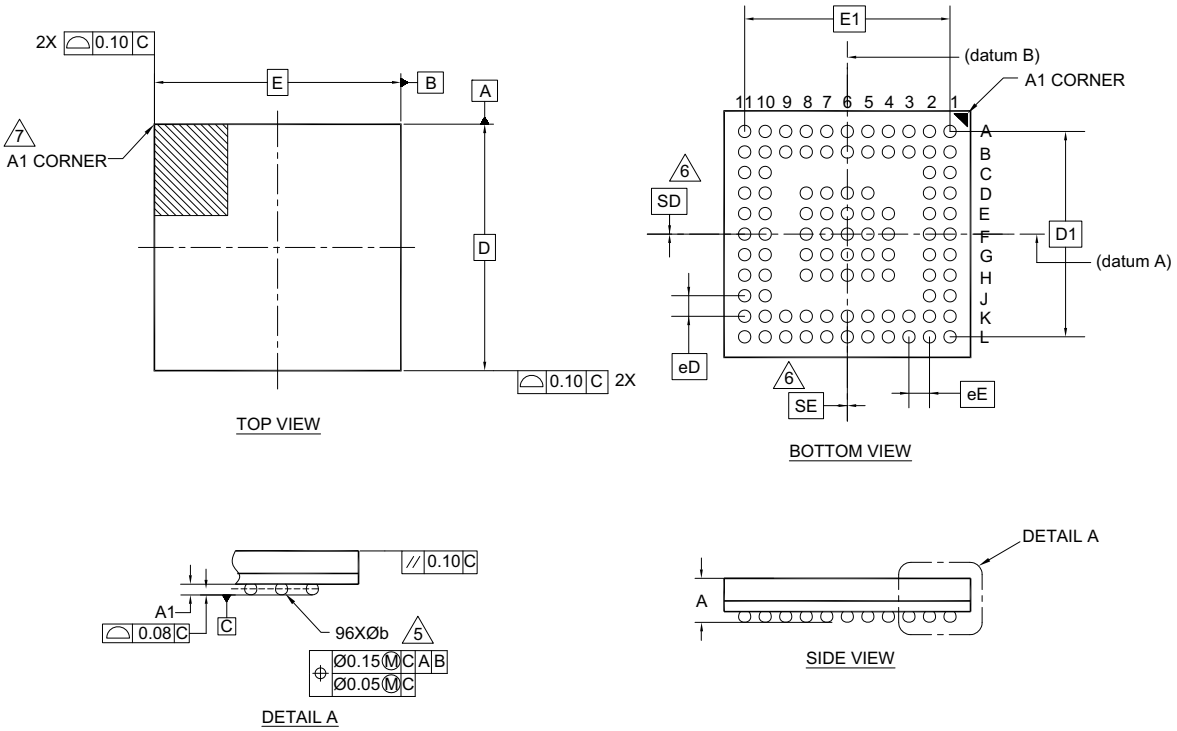
Table 35. SBU Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.20sbu.1	Ron1	On resistances for Aux switch at 3.3 V input	–	4	7	Ω	–
SID.DC.20sbu.2	Ron2	On resistances for Aux switch at 1 V input	–	3	5	Ω	–
SID.DC.20sbu.4	Ileak1	Pin leakage current for SBU1, SBU2	–4.5	–	4.5	µA	–
SID.DC.20sbu.5	Ileak2	Pin leakage current for LSTX, LSRX, AUX_P, AUX_N	–1	–	1	µA	–
SID.DC.20sbu.6	Rpu_aux_1	Pull-up resistance on AUX_P/N	80	–	320	KΩ	–
SID.DC.20sbu.7	Rpu_aux_2	Pull-up resistance on AUX_P/N	0.8	–	1.4	MΩ	–
SID.DC.20sbu.8	Rpd_aux_1	Pull-down resistance on AUX_P/N	80	–	120	KΩ	–
SID.DC.20sbu.9	Rpd_aux_2	Pull-down resistance on AUX_P/N	0.3	–	1.2	MΩ	–
SID.DC.20sbu.10	Rpd_aux_3	Pull-down resistance on AUX_P/N	250	–	611	KΩ	–
SID.DC.20sbu.11	Rpd_aux_4	Pull-down resistance on AUX_P/N	0.3	–	6.11	MΩ	–
SID.DC.20sbu.16	OVP_threshold	Over-voltage protection detection threshold above V_{DDIO}	200	–	1200	mV	–
SID.DC.20sbu.17	lsx_ron_3p3	On resistances of LSTX/LSRX to SBU1/2 switch at 3.3 V input	–	8.5	17	Ω	–
SID.DC.20sbu.18	lsx_ron_1	On resistances of LSTX/LSRX to SBU1/2 switch at 1 V input	–	5.5	11	Ω	–
SID.DC.20sbu.19	aux_ron_flat_fs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V)	–	–	2.5	Ω	Guaranteed by design
SID.DC.20sbu.20	aux_ron_flat_hs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design
SID.DC.20sbu.21	lsx_ron_flat_fs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V)	–	–	5	Ω	Guaranteed by design
SID.DC.20sbu.22	lsx_ron_flat_hs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design

Table 36. SBU Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20sbu.1	Con	Switch ON capacitance	–	–	120	pF	–
SID.AC.20sbu.2	Coff	Switch OFF capacitance - Connector side	–	–	80	pF	–
SID.AC.20sbu.3	Off_isolation	Switch isolation at F = 1 MHz	–50	–		dB	–
SID.AC.20sbu.4	T_{ON}	SBU Switch turn-on time	–	–	200	µs	–
SID.AC.20sbu.5	T_{OFF}	SBU Switch turn-off time	–	–	400	µs	Guaranteed by design
SID.AC.20sbu.6	Off_isolation_tran	Coupling on sbu1,2 terminated to 50 ohm, switch-OFF, Rail-to-rail toggling on LSTX/LSRX	–60	–	60	mV	Guaranteed by design
SID.AC.20sbu.7	X_talk_AC	Cross talk of Switch at F=1 MHz SBU1/2 to SBU2/1	–50	–	–	dB	Guaranteed by design
SID.AC.20sbu.8	X_talk_tran	Check voltage coupling on SBU2(1) when Data is transferred from LSTX (RX) to SBU1 (2)	–70	–	70	mV	Guaranteed by design

Figure 13. 96-Ball BGA (6 × 6 × 1.0 mm), Package Outline, 002-10631



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	96		
∅ b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-225.

002-10631 *A

Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
BOD	Brown out Detect
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG5 pins used to connect to a USB port
XRES	external reset I/O pin

References and Links To Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG5 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG5 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG5 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG5

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG5 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG3: USB Type-C Controller Datasheet