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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f677-e-ml

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# 3.3 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bit of the OSCCON register. See **Section 3.6 "Clock Switching"** for additional information.

# 3.4 External Clock Modes

# 3.4.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see Section 3.7 "Two-Speed Clock Start-up Mode").

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz to 8 MHz	Oscillator Warm-up Delay (Twarm)
Sleep/POR	EC, RC	DC – 20 MHz	2 cycles
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	1 cycle of each
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	125 kHz to 8 MHz	1 μs (approx.)

## TABLE 3-1: OSCILLATOR DELAY EXAMPLES

## 3.4.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC<sup>®</sup> MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

## FIGURE 3-2:

#### EXTERNAL CLOCK (EC) MODE OPERATION



#### 3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

FIGURE 3-7:	TWO-SPEED START-UP	
HFINTOSC /		
OSC1	←Tost	
OSC2		
Program Counter	PC-N (PC	XPC + 1X
System Clock		

# 4.2 Additional Pin Functions

Every PORTA pin on this device family has an interrupton-change option and a weak pull-up option. RA0 also has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

# 4.2.1 ANSEL AND ANSELH REGISTERS

The ANSEL and ANSELH registers are used to disable the input buffers of I/O pins, which allow analog voltages to be applied to those pins without causing excessive current. Setting the ANSx bit of a corresponding pin will cause all digital reads of that pin to return '0' and also permit analog functions of that pin to operate correctly.

The state of the ANSx bit has no effect on the digital output function of its corresponding pin. A pin with the TRISx bit clear and ANSx bit set will operate as a digital output, together with the analog input function of that pin. Pins with the ANSx bit set always read '0', which can cause unexpected behavior when executing read or write operations on the port due to the read-modifywrite sequence of all such operations.

# 4.2.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the RABPU bit of the OPTION register. A weak pull-up is automatically enabled for RA3 when configured as MCLR and disabled when RA3 is an I/O. There is no software control of the MCLR pull-up.

# 4.2.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 4-6. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (RABIF) in the INTCON register (Register 2-6).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- a) Any read or write of PORTA. This will end the mismatch condition, then,
- b) Clear the flag bit RABIF.

A mismatch condition will continue to set flag bit RABIF. Reading PORTA will end the mismatch condition and allow flag bit RABIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOR Reset. After these Resets, the RABIF flag will continue to be set if a mismatch is present.

**Note:** If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RABIF interrupt flag may not get set.









#### **REGISTER 9-3:** ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

| R/W-x  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES9 | ADRES8 | ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 |
| bit 7  |        |        |        |        |        |        | bit 0  |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as	s 'O'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0

**ADRES<9:2>**: ADC Result Register bits Upper eight bits of 10-bit conversion result

#### **REGISTER 9-4:** ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-6	ADRES<1:0>: ADC Result Register bits
	Lower two bits of 10-bit conversion result
bit 5-0	Reserved: Do not use.

#### REGISTER 9-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x	R/W-x						
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-2 Reserved: Do not use.

bit 1-0 ADRES<9:8>: ADC Result Register bits Upper two bits of 10-bit conversion result

# REGISTER 9-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

| R/W-x  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7  |        |        |        |        |        |        | bit 0  |

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-0 ADRES<7:0>: ADC Result Register bits

Lower eight bits of 10-bit conversion result

## 11.3.1 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

# EQUATION 11-1: PWM PERIOD

$$PWM Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet$$
$$(TMR2 \ Prescale \ Value)$$
Note: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

#### Note: The Timer2 postscaler (see Section 7.1 "Timer2 Operation") is not used in the determination of the PWM frequency.

# 11.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1B<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

# EQUATION 11-2: PULSE WIDTH

 $Pulse Width = (CCPR1L:CCP1CON < 5:4>) \bullet$ 

TOSC • (TMR2 Prescale Value)

# EQUATION 11-3: DUTY CYCLE RATIO

$$Duty Cycle Ratio = \frac{(CCPR1L:CCP1CON < 5:4>)}{4(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-3).

# 11.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

## EQUATION 11-4: PWM RESOLUTION

Resolution = 
$$\frac{\log[4(PR2 + 1)]}{\log(2)}$$
 bits

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

## TABLE 11-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

# TABLE 11-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

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# 11.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 11-6). This mode can be used for Half-Bridge applications, as shown in Figure 11-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 11.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations. Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.





# FIGURE 11-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS



# 13.11 SSP I<sup>2</sup>C Operation

The SSP module in  $l^2$ C mode, fully implements all slave functions, except general call support, and provides interrupts on Start and Stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RB6/ SCK/SCL pin, which is the clock (SCL), and the RB4/ AN10/SDI/SDA pin, which is the data (SDA).

The SSP module functions are enabled by setting SSP enable bit SSPEN (SSPCON<5>).

FIGURE 13-7: SSP BLOCK DIAGRAM (I<sup>2</sup>C™ MODE)



The SSP module has six registers for the  $I^2C$  operation, which are listed below.

- SSP Control register (SSPCON)
- SSP Status register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift register (SSPSR) Not directly accessible
- SSP Address register (SSPADD)
- SSP Mask register (SSPMSK)

The SSPCON register allows control of the  $I^2C$  operation. Four mode selection bits (SSPCON<3:0>) allow one of the following  $I^2C$  modes to be selected:

- I<sup>2</sup>C Slave mode (7-bit address)
- I<sup>2</sup>C Slave mode (10-bit address)
- I<sup>2</sup>C Slave mode (7-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I<sup>2</sup>C Slave mode (10-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I<sup>2</sup>C Start and Stop bit interrupts enabled to support Firmware Master mode; Slave is idle

Selection of any  $I^2C$  mode with the SSPEN bit set forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISB bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the  $I^2C$  module.

# 13.12 Slave Mode

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISB<6,4> are set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge  $(\overline{ACK})$ pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this ACK pulse. They include (either or both):

- a) The Buffer Full bit BF of the SSPSTAT register was set before the transfer was received.
- b) The overflow bit SSPOV of the SSPCON register was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 13-3 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. For high and low times of the  $I^2C$  specification, as well as the requirements of the SSP module, see **Section 17.0 "Electrical Specifications"**.

## 14.2.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in EC mode with <u>PWRTE</u> bit erased (PWRT disabled), there will be no time-out at all. Figures 14-4, 14-5 and 14-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see Section 3.7.2 "Two-speed Start-up Sequence" and Section 3.8 "Fail-Safe Clock Monitor").

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Then, bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (see Figure 14-5). This is useful for testing purposes or to synchronize more than one PIC16F631/677/685/ 687/689/690 device operating in parallel.

Table 14-5 shows the Reset conditions for some special registers, while Table 14-4 shows the Reset conditions for all the registers.

#### 14.2.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is  $\overline{\text{BOR}}$  (Brown-out Reset).  $\overline{\text{BOR}}$  is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if  $\overline{\text{BOR}} = 0$ , indicating that a Brown-out has occurred. The  $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see Section 4.2.4 "Ultra Low-Power Wake-up" and Section 14.2.4 "Brown-out Reset (BOR)".

Oscillator Configuration	Powe	er-up	Brown-o	Wake-up from	
	<b>PWRTE</b> = 0	TE = 0PWRTE = 1PWRTE = 0		PWRTE = 1	Sleep
XT, HS, LP	TPWRT + 1024 • Tosc	1024 • Tosc	Tpwrt + 1024 • Tosc	1024 • Tosc	1024 • Tosc
LP, T1OSCIN = 1	TPWRT	—	TPWRT	_	—
RC, EC, INTOSC	TPWRT		TPWRT		_

## TABLE 14-1:TIME-OUT IN VARIOUS SITUATIONS

## TABLE 14-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	Condition	
0	x	1	1	Power-on Reset	
u	0	1	1	Brown-out Reset	
u	u	0	u	WDT Reset	
u	u	0	0	WDT Wake-up	
u	u	u	u	MCLR Reset during normal operation	
u	u	1	0	MCLR Reset during Sleep	

**Legend:** u = unchanged, x = unknown

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## TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PCON	—	—	ULPWUE	SBOREN	-	_	POR	BOR	01qq	0uuu
STATUS	IRP	RP1	RPO	TO	PD	Z	DC	С	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR. Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

TABLE 14-4:	INITIALIZATION CONDITION FOR REGISTER
-------------	---------------------------------------

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset <sup>(1)</sup>	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	XXXX XXXX	uuuu uuuu	uuuu uuuu
INDF	00h/80h/ 100h/180h	XXXX XXXX	XXXX XXXX	սսսս սսսս
TMR0	01h/101h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h/ 102h/182h	0000 0000	0000 0000	PC + 1 <sup>(3)</sup>
STATUS	03h/83h/ 103h/183h	0001 1xxx	000q quuu <sup>(4)</sup>	uuuq quuu <sup>(4)</sup>
FSR	04h/84h/ 104h184h	XXXX XXXX	սսսս սսսս	սսսս սսսս
PORTA	05h/105h	xx xxxx	uu uuuu	uu uuuu
PORTB	06h/106h	xxxx	uuuu	uuuu
PORTC	07h/107h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah/8Ah/ 10Ah/18Ah	0 0000	0 0000	u uuuu
INTCON	0Bh/8Bh/ 10Bh/18Bh	0000 000x	0000 000u	uuuu uuuu <sup>(2)</sup>
PIR1	0Ch	-000 0000	-000 0000	-uuu uuuu <sup>(2)</sup>
PIR2	0Dh	0000	0000	uuuu <b>(2)</b>
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	սսսս սսսս
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	սսսս սսսս	սսսս սսսս
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
SSPBUF	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	14h	0000 0000	0000 0000	սսսս սսսս
CCPR1L	15h	xxxx xxxx	uuuu uuuu	սսսս սսսս
CCPR1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	17h	0000 0000	0000 0000	uuuu uuuu
RCSTA	18h	0000 000x	0000 000x	սսսս սսսս
TXREG	19h	0000 0000	0000 0000	uuuu uuuu
RCREG	1Ah	0000 0000	0000 0000	uuuu uuuu
PWM1CON	1Ch	0000 0000	0000 0000	սսսս սսսս
ECCPAS	1Dh	0000 0000	0000 0000	uuuu uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	սսսս սսսս
ADCON0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h/181h	1111 1111	1111 1111	սսսս սսսս
TRISA	85h/185h	11 1111	11 1111	uu uuuu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 14-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** Accessible only when SSPM < 3:0 > = 1001.

Register	Address	Power-on Reset	MCLR Reset WDT Reset (Continued) Brown-out Reset <sup>(1)</sup>	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
TRISB	86h/186h	1111	1111	uuuu
TRISC	87h/187h	1111 1111	1111 1111	<u>uuuu</u> uuuu
PIE1	8Ch	-000 0000	-000 0000	-uuu uuuu
PIE2	8Dh	0000	0000	uuuu uuuu
PCON	8Eh	010x	0uuq <sup>1,5)</sup>	uuuu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	0 0000	u uuuu	u uuuu
PR2	92h	1111 1111	1111 1111	սսսս սսսս
SSPADD	93h	0000 0000	1111 1111	uuuu uuuu
SSPMSK <sup>(6)</sup>	93h		1111 1111	սսսս սսսս
SSPSTAT	94h	0000 0000	1111 1111	սսսս սսսս
WPUA	95h	11 -111	11 -111	սսսս սսսս
IOCA	96h	00 0000	00 0000	uu uuuu
WDTCON	97h	0 1000	0 1000	u uuuu
TXSTA	98h	0000 0010	0000 0010	սսսս սսսս
SPBRG	99h	0000 0000	0000 0000	սսսս սսսս
SPBRGH	9Ah	0000 0000	0000 0000	սսսս սսսս
BAUDCTL	9Bh	01-0 0-00	01-0 0-00	uu-u u-uu
ADRESL	9Eh	XXXX XXXX	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000	-000	-uuu
EEDAT	10Ch	0000 0000	0000 0000	uuuu uuuu
EEADR	10Dh	0000 0000	0000 0000	<u>uuuu</u> uuuu
EEDATH	10Eh	00 0000	00 0000	uu uuuu
EEADRH	10Fh	0000	0000	uuuu
WPUB	115h	1111	1111	uuuu
IOCB	116h	0000	0000	uuuu
VRCON	118h	0000 0000	0000 0000	uuuu uuuu
CM1CON0	119h	0000 -000	0000 -000	uuuu -uuu
CM2CON0	11Ah	0000 -000	0000 -000	uuuu -uuu
CM2CON1	11Bh	0000	0010	uuuu
ANSEL	11Eh	1111 1111	1111 1111	uuuu uuuu
ANSELH	11 Fh	1111	1111	uuuu
EECON1	18Ch	x x000	u q000	uuuu
EECON2	18Dh			
PSTRCON	19Dh	0 0001	0 0001	u uuuu
SRCON	19EH	0000 00	0000 00	uuuu uu

## TABLE 14-4: INITIALIZATION CONDITION FOR REGISTER (CONTINUED)

 $\label{eq:logend: u = unchanged, x = unknown, - = unimplemented bit, reads as `0', q = value depends on condition.$ 

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 14-5 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** Accessible only when SSPM < 3:0 > = 1001.

# TABLE 14-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

# TABLE 17-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER<br/>AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
30	ТмсL	MCLR Pulse Width (low)	2 5	_		μS μS	VDD = 5V, -40°C to +85°C VDD = 5V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V
32	Tost	Oscillation Start-up Timer Period <sup>(1, 2)</sup>	_	1024	_	Tosc	(Note 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	Tioz	I/O High-impedance from MCLR Low or Watchdog Timer Reset	_	_	2.0	μS	
35	VBOR	Brown-out Reset Voltage	2.0	_	2.2	V	(Note 4)
36*	VHYST	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	_	_	μS	$VDD \leq VBOR$

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to the OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.
  - 2: By design.
  - 3: Period of the slower clock.
  - **4:** To ensure these voltage tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

Param	Device	Min	True	Max	Unite	Condition		
No.	Characteristics	win.		Units	Vdd	Note		
D001	Vdd	2.1	_	5.5	V	—	Fosc $\leq$ 8 MHz: HFINTOSC, EC	
		2.1	—	5.5	V	—	Fosc ≤ 4 MHz	
D010	Supply Current (IDD)	_	_	47		2.1	E	
		_	_	69	μA	3.0	-FOSC = 32  kHz	
		_	_	108		5.0		
D011		_	_	357		2.1	E (184)	
		_		533	μA	3.0	-Fosc = 1 MHz	
		_	_	729		5.0		
D012		_	_	535	^	2.1		
		_		875	μΑ	3.0	Fosc = 4 MHz	
		_	_	1.32	mA	5.0		
D013		_	_	336		2.1		
		_	—	477	μA	3.0	-Fosc = 1 MHz	
		_	—	777		5.0		
D014		_	_	505		2.1		
		_		724	μΑ	3.0	Fosc = 4 MHz	
		_	_	1.30	mA	5.0		
D015		_		51		2.1		
		_	_	92	μΛ	3.0	Fosc = 31 kHz	
		_		117	mA	5.0		
D016		_		665		2.1		
		_	_	970	μΛ	3.0		
		_		1.56	mA	5.0		
D017		_		936	μA	2.1		
		_		1.34	m۸	3.0	THOSC = 8 MHZ	
		_	_	2.27		5.0		
D018		_		605		2.1		
		_		903	μΑ	3.0	-Fosc = 4 MHz	
		_	—	1.43	mA	5.0		
D019		_	—	6.61	m۸	4.5	Fosc = 20 MHz	
		_	—	7.81		5.0	HS Oscillator	

# TABLE 17-19: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC16F685/687/689/690-H (High Temp.)

















#### FIGURE 18-20: WDT PERIOD vs. TEMPERATURE OVER VDD (5.0V)







FIGURE 18-31: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE



**COMPARATOR RESPONSE TIME (RISING EDGE)** 

FIGURE 18-32:







FIGURE 18-33: COMPARATOR RESPONSE TIME (FALLING EDGE)





## FIGURE 18-45: TYPICAL VP6 REFERENCE VOLTAGE OVER TEMPERATURE (5V)

# APPENDIX A: DATA SHEET REVISION HISTORY

## Revision A (March 2005)

This is a new data sheet.

## Revision B (May 2006)

Added 631/677 part numbers; Added pin summary tables after pin diagrams; Incorporated Golden Chapters.

# **Revision C (July 2006)**

Revised Section 4.2.1, ANSEL and ANSELH Registers; Register 4-3, ANSEL Analog Select; Added Register 4-4, ANSELH Analog Select High; Section 11.3.2, Revised CCP1<1:0> to DC1B<1:0>; Section 11.3.7, Number 4 - Revised CCP1 to DC1B; Figure 11-5, Revised CCP1 to DC1B; Table 11-4, Revised P1M to P1M<1:0>; Section 12.3.1, Revised Paragraph 3; Revised Note 2; Revised Figure 12-6 Title.

# **Revision D (February 2007)**

Removed Preliminary status; Changed PICmicro to PIC; Replaced Dev. Tool Section; Replaced Package Drawings.

# **Revision E (March 2008)**

Add Char Data charts; Updated EUSART Golden Chapter; Updated the Electrical Specification section; Updated Package Drawings as needed.

# **Revision F (April 2015)**

Added Section 17.8: High Temperature Operation in the Electrical Specifications section.

# APPENDIX B: MIGRATING FROM OTHER PIC<sup>®</sup> DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC16F6XX Family of devices.

## B.1 PIC16F676 to PIC16F685

#### TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F685
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	4096
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2
ECCP+	N	Y
Ultra Low-Power Wake-up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	31 kHz-8 MHz
Clock Switching	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.