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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f677-i-ss

TABLE 1-5: PINOUT DESCRIPTION – PIC16F690

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT/ ULPWU	RA0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN0	AN	—	A/D Channel 0 input.
	C1IN+	AN	—	Comparator C1 positive input.
	ICSPDAT	TTL	CMOS	ICSP™ Data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/AN1/C12IN0-/V$_{REF}$/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN1	AN	—	A/D Channel 1 input.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	V$_{REF}$	AN	—	External Voltage Reference for A/D.
	ICSPCLK	ST	—	ICSP™ clock.
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN2	AN	—	A/D Channel 2 input.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
RA3/$\overline{MCLR}$/V$_{PP}$	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	V$_{PP}$	HV	—	Programming voltage.
RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN3	AN	—	A/D Channel 3 input.
	$\overline{T1G}$	ST	—	Timer1 gate input.
	OSC2	—	XTAL	Crystal/Resonator.
	CLKOUT	—	CMOS	F$_{OSC}$/4 output.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	T1CKI	ST	—	Timer1 clock input.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	External clock input/RC oscillator connection.
RB4/AN10/SDI/SDA	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	SDI	ST	—	SPI data input.
	SDA	ST	OD	I^{2}C™ data input/output.
RB5/AN11/RX/DT	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.

Legend: AN = Analog input or output   CMOS=CMOS compatible input or outputOD= Open Drain
TTL = TTL compatible input   ST= Schmitt Trigger input with CMOS levels
HV = High Voltage   XTAL= Crystal

2.2.2.1   STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (GPR and SFR)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 15.0 "Instruction Set Summary"**

> **Note 1:** The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1:   STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC[1]	C[1]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`00` = Bank 0 (00h-7Fh)
`01` = Bank 1 (80h-FFh)
`10` = Bank 2 (100h-17Fh)
`11` = Bank 3 (180h-1FFh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)[1]
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit[1] (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)[1]
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.5   PIE2 Register

The PIE2 register contains the interrupt enable bits, as shown in Register 2-5.

> **Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-5:   PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
OSFIE	C2IE	C1IE	EEIE	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **OSFIE:** Oscillator Fail Interrupt Enable bit

    1 = Enables oscillator fail interrupt
    0 = Disables oscillator fail interrupt

bit 6   **C2IE:** Comparator C2 Interrupt Enable bit

    1 = Enables Comparator C2 interrupt
    0 = Disables Comparator C2 interrupt

bit 5   **C1IE:** Comparator C1 Interrupt Enable bit

    1 = Enables Comparator C1 interrupt
    0 = Disables Comparator C1 interrupt

bit 4   **EEIE:** EE Write Operation Interrupt Enable bit

    1 = Enables write operation interrupt
    0 = Disables write operation interrupt

bit 3-0   **Unimplemented:** Read as '0'

3.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.
.

> **Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
>
> **2:** Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
>
> **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
>
> • AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
>
> • AN849, "*Basic PIC® Oscillator Design*" (DS00849)
>
> • AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
>
> • AN949, "*Making Your Oscillator Work*" (DS00949)

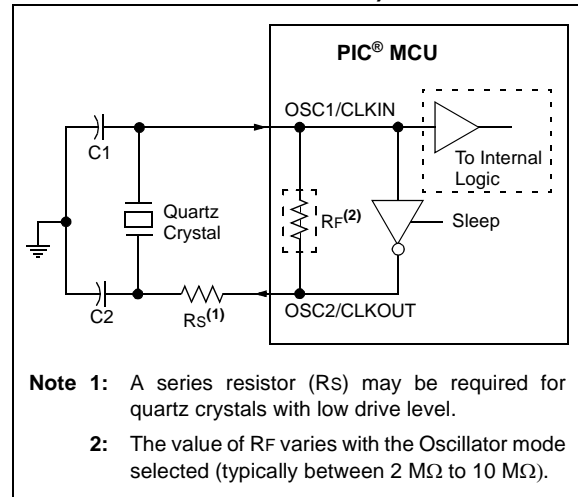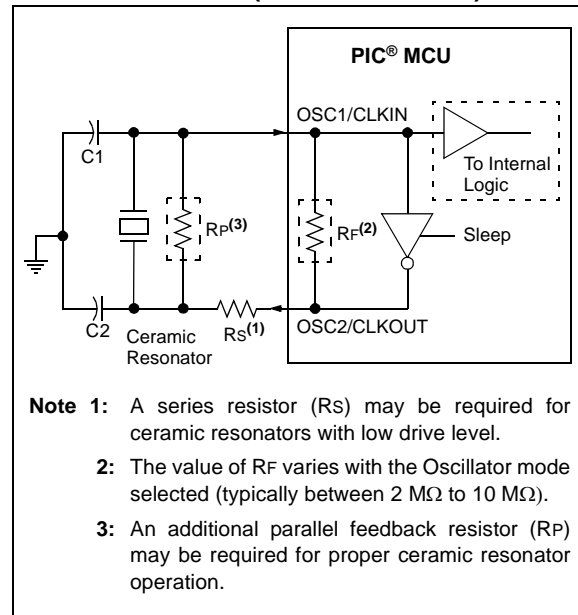**FIGURE 3-3:** **QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)**

> **Note 1:** A series resistor (R_S) may be required for quartz crystals with low drive level.
>
> **2:** The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

FIGURE 3-4: **CERAMIC RESONATOR OPERATION (XT OR HS MODE)**

> **Note 1:** A series resistor (R_S) may be required for ceramic resonators with low drive level.
>
> **2:** The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
>
> **3:** An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

3.8 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word register (CONFIG). The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, RC and RCIO).

FIGURE 3-8:   FSCM BLOCK DIAGRAM
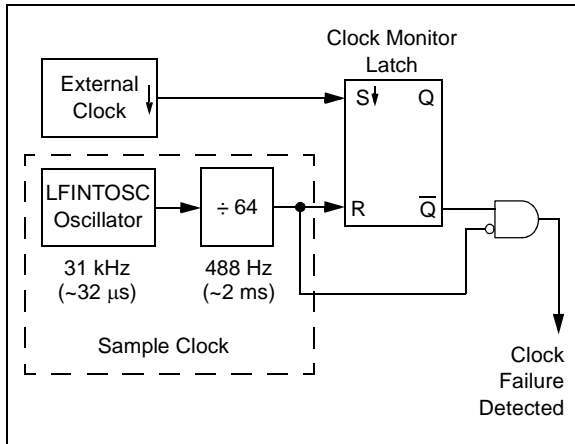
3.8.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 3-8. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

3.8.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

3.8.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a `SLEEP` instruction or toggling the SCS bit of the OSCCON register. When the SCS bit is toggled, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

3.8.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

> **Note:** Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify the oscillator start-up and that the system clock switchover has successfully completed.

REGISTER 4-3: **ANSEL: ANALOG SELECT REGISTER**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0   **ANS<7:0>**: Analog Select bits
                Analog select between analog or digital function on pins AN<7:0>, respectively.
                1 = Analog input. Pin is assigned as analog input[1].
                0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 4-4: **ANSELH: ANALOG SELECT HIGH REGISTER[2]**

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANS11	ANS10	ANS9	ANS8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4   **Unimplemented:** Read as '0'

bit 3-0   **ANS<11:8>**: Analog Select bits
                Analog select between analog or digital function on pins AN<7:0>, respectively.
                1 = Analog input. Pin is assigned as analog input[1].
                0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

    2: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

PIC16F631/677/685/687/689/690

REGISTER 4-5: WPUA: PORTA REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented**: Read as '0'

bit 5-4   **WPUA<5:4>:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

bit 3   **Unimplemented**: Read as '0'

bit 2-0   **WPUA<2:0>:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global RABPU bit of the OPTION register must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).
3: The RA3 pull-up is enabled when configured as MCLR and disabled as an I/O in the Configuration Word.
4: WPUA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

REGISTER 4-6: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented**: Read as '0'

bit 5-0   **IOCA<5:0>:** Interrupt-on-change PORTA Control bit
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.
2: IOCA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

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PIC16F631/677/685/687/689/690

4.2.5.2   RA1/AN1/C12IN0-/VREF/ICSPCLK

Figure 4-2 shows the diagram for this pin. The RA1/AN1/C12IN0-/VREF/ICSPCLK pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- an analog input to Comparator C1 or C2
- a voltage reference input for the ADC
- In-Circuit Serial Programming clock
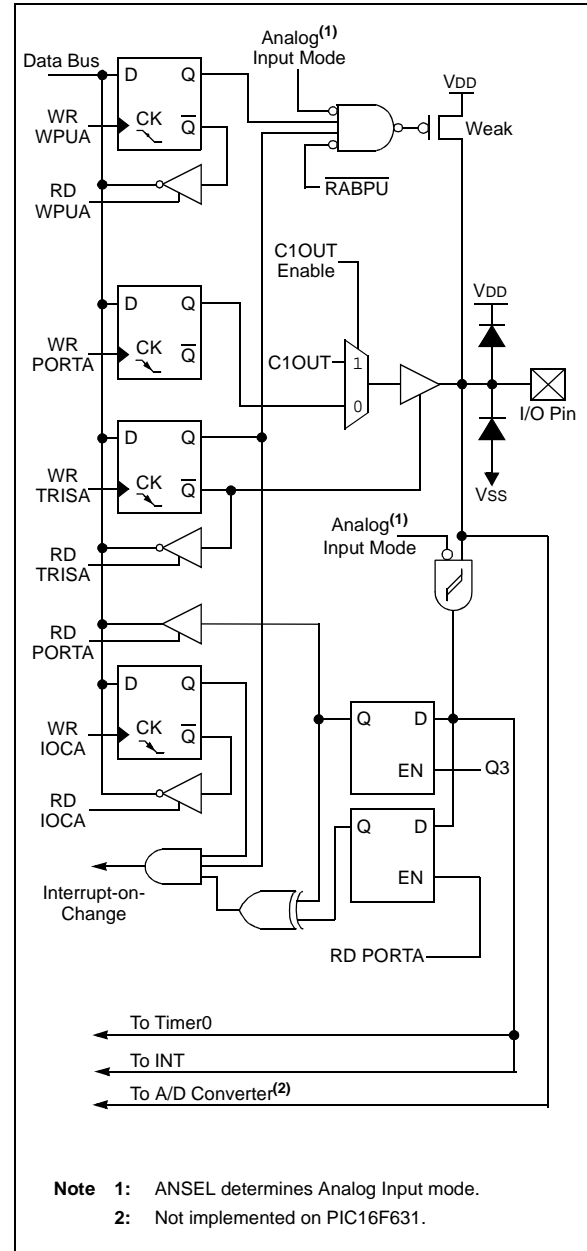
FIGURE 4-2:   BLOCK DIAGRAM OF RA1

Note 1: ANSEL determines Analog Input mode.
2: Not implemented on PIC16F631.
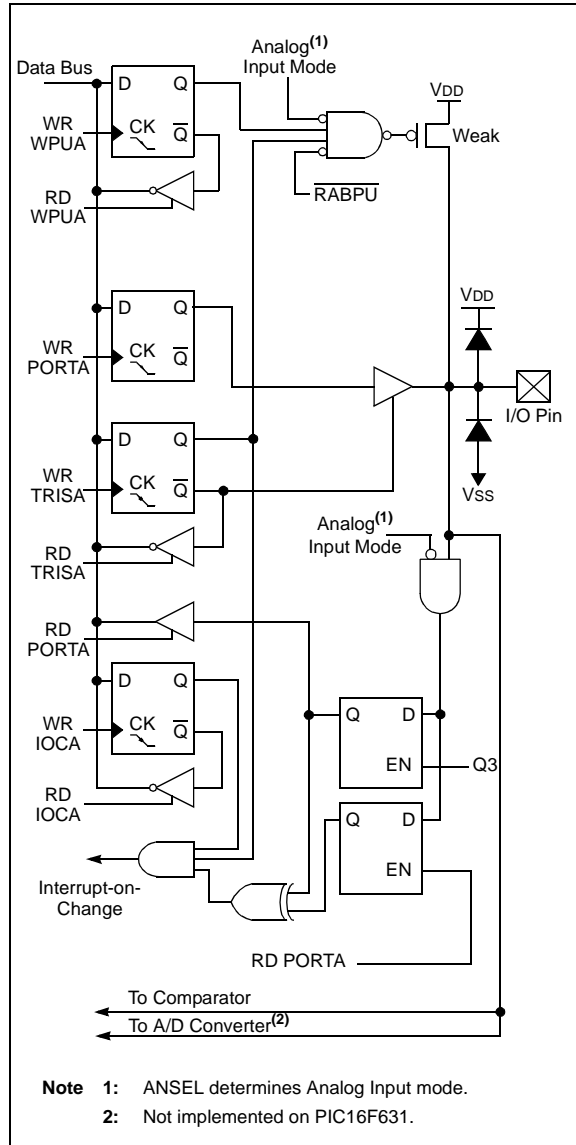
4.2.5.3   RA2/AN2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2/AN2/T0CKI/INT/C1OUT pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- the clock input for Timer0
- an external edge triggered interrupt
- a digital output from Comparator C1

FIGURE 4-3:   BLOCK DIAGRAM OF RA2

Note 1: ANSEL determines Analog Input mode.
2: Not implemented on PIC16F631.

4.5.1 RC0/AN4/C2IN+

The RC0 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- an analog input to Comparator C2

4.5.2 RC1/AN5/C12IN1-

The RC1 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input to Comparator C1 or C2

4.5.3 RC2/AN6/C12IN2-/P1D

The RC2/AN6/P1D[1] is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- a PWM output
- an analog input to Comparator C1 or C2

> **Note 1:** P1D is available on PIC16F685/
> PIC16F690 only.

4.5.4 RC3/AN7/C12IN3-/P1C

The RC3/AN7/P1C[1] is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- a PWM output
- a PWM output
- an analog input to Comparator C1 or C2

> **Note 1:** P1C is available on PIC16F685/
> PIC16F690 only.

FIGURE 4-11: BLOCK DIAGRAM OF RC0 AND RC1

> **Note 1:** ANSEL determines Analog Input mode.
> **2:** Not implemented on PIC16F631.

FIGURE 4-12: BLOCK DIAGRAM OF RC2 AND RC3

> Available on PIC16F685/PIC16F690 only.
> **Note 1:** ANSEL determines Analog Input mode.
> **2:** Not implemented on PIC16F631.

6.12   Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1:   T1CON: TIMER 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV[1]	TMR1GE[2]	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **T1GINV:** Timer1 Gate Invert bit[1]

1 = Timer1 gate is active-high (Timer1 counts when Timer1 gate signal is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6   **TMR1GE:** Timer1 Gate Enable bit[2]

<u>If TMR1ON = 0:</u>
This bit is ignored
<u>If TMR1ON = 1:</u>
1 = Timer1 counting is controlled by the Timer1 Gate function
0 = Timer1 is always counting

bit 5-4   **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3   **T1OSCEN:** LP Oscillator Enable Control bit

<u>If INTOSC without CLKOUT oscillator is active:</u>
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
<u>Else:</u>
This bit is ignored

bit 2   **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit

<u>TMR1CS = 1:</u>
1 = Do not synchronize external clock input
0 = Synchronize external clock input
<u>TMR1CS = 0:</u>
This bit is ignored. Timer1 uses the internal clock

bit 1   **TMR1CS:** Timer1 Clock Source Select bit

1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (F$_{OSC}$/4)

bit 0   **TMR1ON:** Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1

Note 1:   T1GINV bit inverts the Timer1 gate logic, regardless of source.
        2:   TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or C2OUT, as selected by the T1GSS bit of the CM2CON1 register, as a Timer1 gate source.

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

Note:	The ADC module applies to PIC16F677/ PIC16F685/PIC16F687/PIC16F689/ PIC16F690 devices only.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

FIGURE 9-1:   ADC BLOCK DIAGRAM

Note 1:   P1C and P1D available on PIC16F685/PIC16F690 only.
     2:   SS, SDO, SDA, RX and DT available on PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.
     3:   ADC module applies to the PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 devices only.
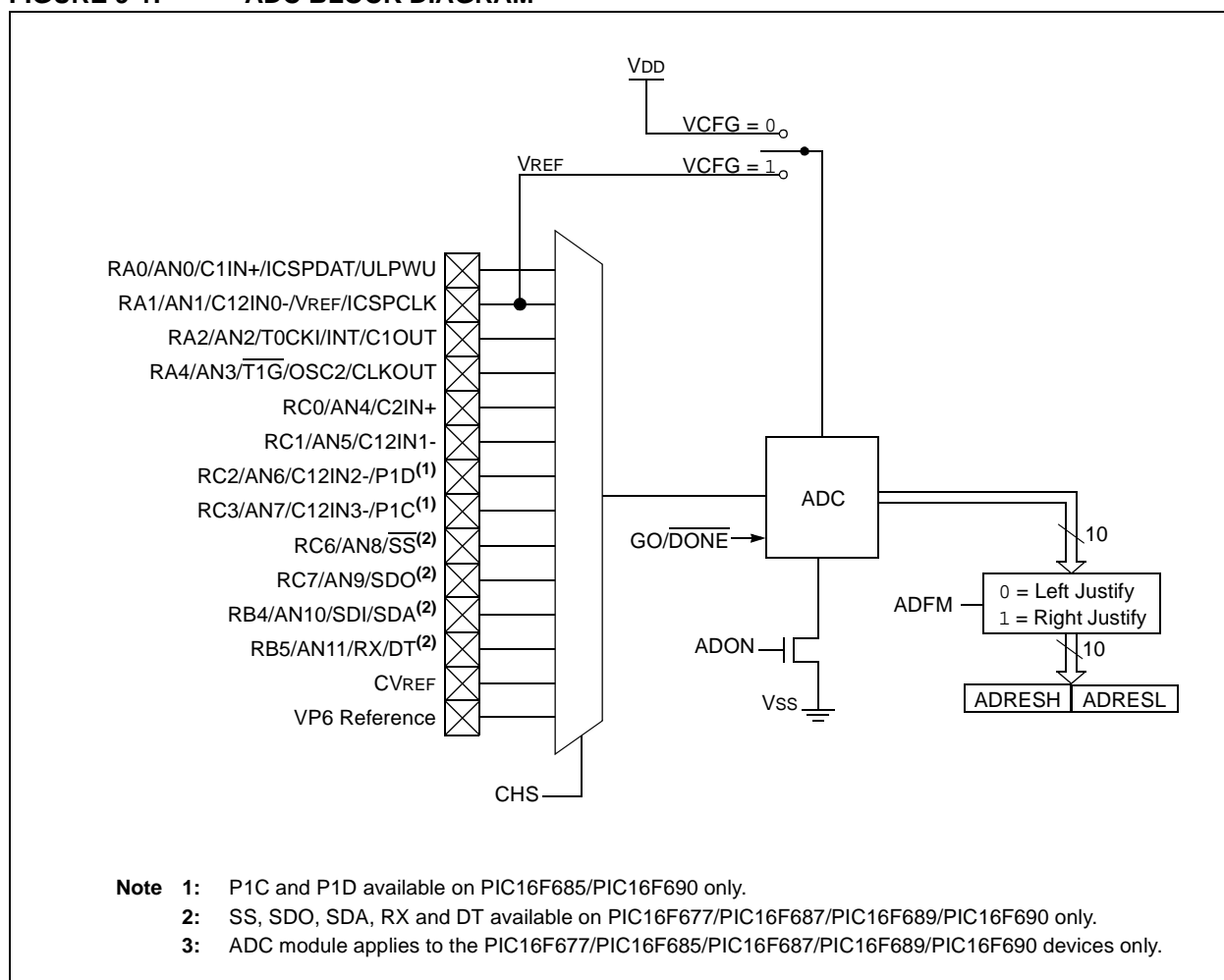
TABLE 9-1: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES (V_{DD} $\geq$ 3.0V, V_{REF} $\geq$ 2.5V)

ADC Clock Period (T$_{AD}$)		Device Frequency (F$_{OSC}$)			
ADC Clock Source	ADCS<2:0>	20 MHz	8 MHz	4 MHz	1 MHz
F$_{OSC}$/2	000	100 ns[2]	250 ns[2]	500 ns[2]	2.0 μs
F$_{OSC}$/4	100	200 ns[2]	500 ns[2]	1.0 μs[2]	4.0 μs
F$_{OSC}$/8	001	400 ns[2]	1.0 μs[2]	2.0 μs	8.0 μs[3]
F$_{OSC}$/16	101	800 ns[2]	2.0 μs	4.0 μs	16.0 μs[3]
F$_{OSC}$/32	010	1.6 μs	4.0 μs	8.0 μs[3]	32.0 μs[3]
F$_{OSC}$/64	110	3.2 μs	8.0 μs[3]	16.0 μs[3]	64.0 μs[3]
F$_{RC}$	x11	2-6 μs[1,4]	2-6 μs[1,4]	2-6 μs[1,4]	2-6 μs[1,4]

Legend: Shaded cells are outside of recommended range.

Note 1: The F$_{RC}$ source has a typical T$_{AD}$ time of 4 μs for V$_{DD}$ > 3.0V.

2: These values violate the minimum required T$_{AD}$ time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the F$_{RC}$ clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION T$_{AD}$ CYCLES
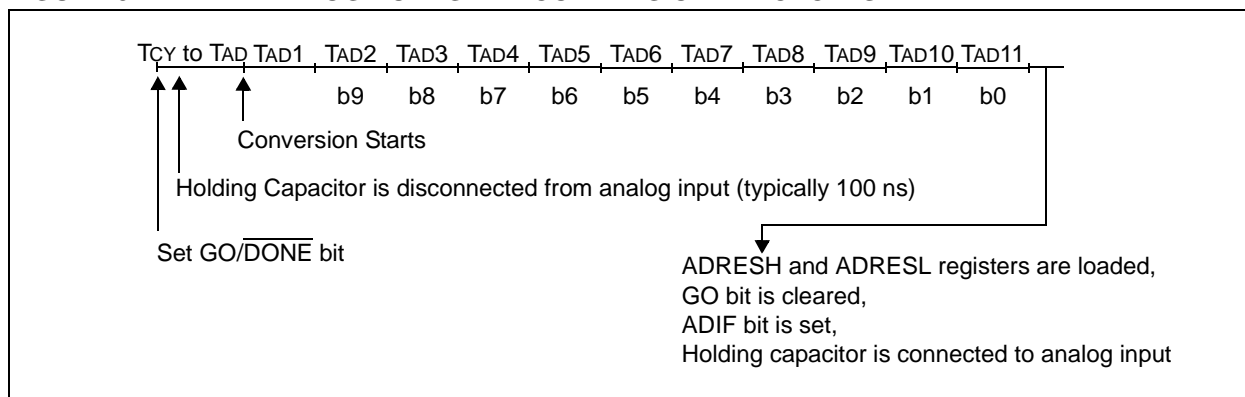
9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

> **Note:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

Please see **Section 9.1.5 "Interrupts"** for more information.

REGISTER 9-2:   ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2
001 = Fosc/8
010 = Fosc/32
x11 = Frc (clock derived from a dedicated internal oscillator = 500 kHz max)
100 = Fosc/4
101 = Fosc/16
110 = Fosc/64

bit 3-0   **Unimplemented:** Read as '0'

PIC16F631/677/685/687/689/690

11.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 11-6). This mode can be used for Half-Bridge applications, as shown in Figure 11-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 11.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

FIGURE 11-8: **EXAMPLE OF HALF-BRIDGE PWM OUTPUT**

td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.
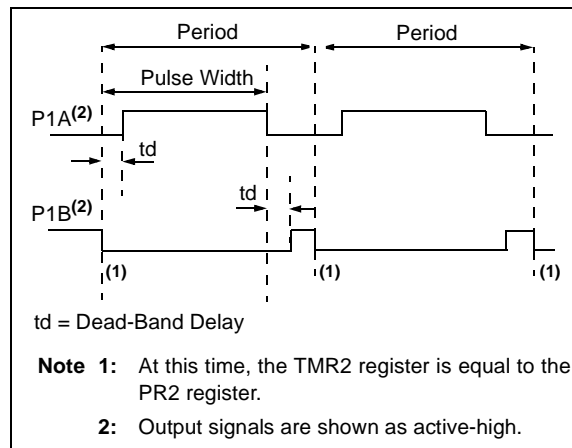
FIGURE 11-9: **EXAMPLE OF HALF-BRIDGE APPLICATIONS**
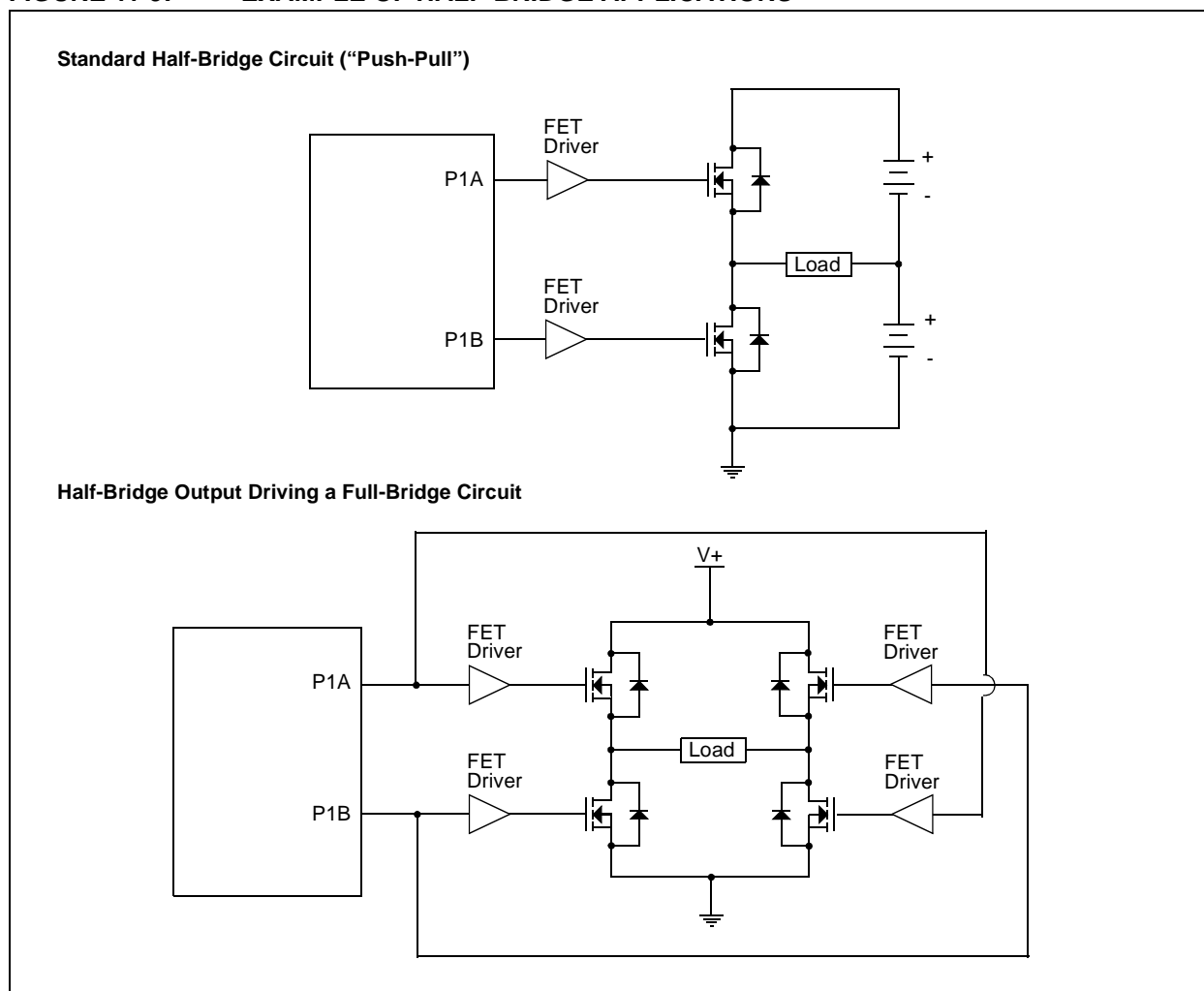
12.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a V$_{OH}$ mark state which represents a '1' data bit, and a V$_{OL}$ space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 12-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

12.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 12-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

12.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note 1: When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the EUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded.

2: The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

12.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one T$_{CY}$ immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

12.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

PIC16F631/677/685/687/689/690

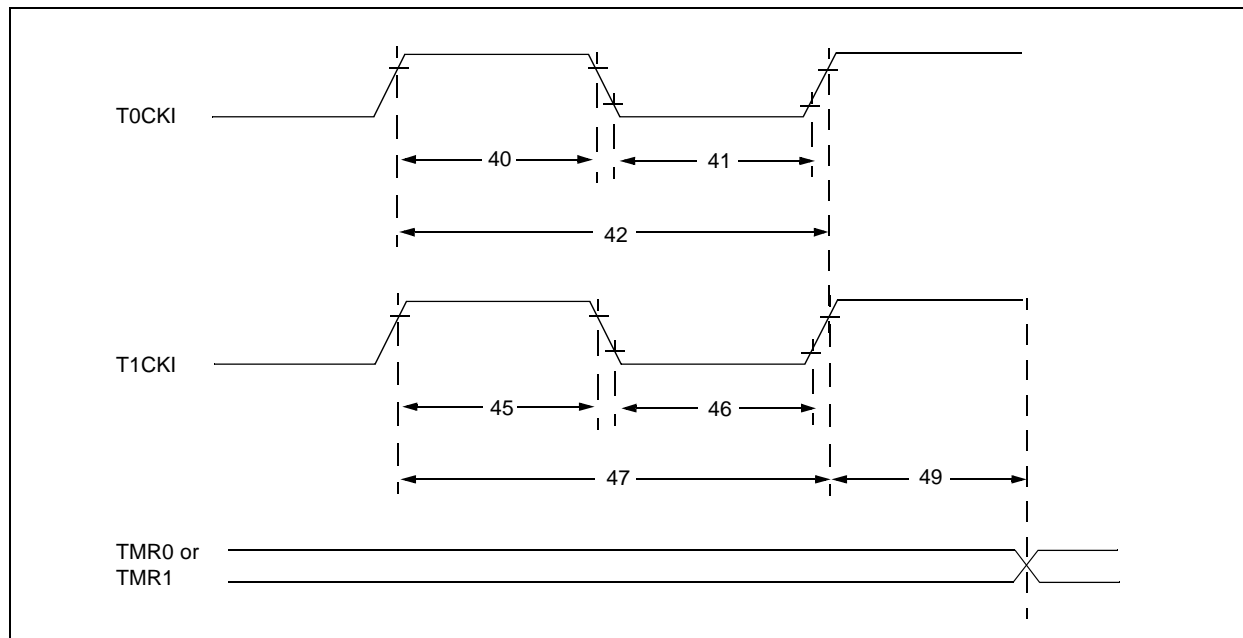**FIGURE 17-8:** TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

TABLE 17-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature   -40°C ≤ TA ≤ +125°C

Param No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 17-19: **DC CHARACTERISTICS FOR I_{DD} SPECIFICATIONS FOR PIC16F685/687/689/690-H (High Temp.)**

Param No.	Device Characteristics	Min.	Typ.	Max.	Units	Condition	
						V_{DD}	Note
D001	V_{DD}	2.1	—	5.5	V	—	F_{OSC} ≤ 8 MHz: HFINTOSC, EC
		2.1	—	5.5	V	—	F_{OSC} ≤ 4 MHz
D010	Supply Current (I_{DD})	—	—	47	μA	2.1	Fosc = 32 kHz LP Oscillator
		—	—	69		3.0	
		—	—	108		5.0	
D011		—	—	357	μA	2.1	Fosc = 1 MHz XT Oscillator
		—	—	533		3.0	
		—	—	729		5.0	
D012		—	—	535	μA	2.1	Fosc = 4 MHz XT Oscillator
		—	—	875		3.0	
		—	—	1.32	mA	5.0	
D013		—	—	336	μA	2.1	Fosc = 1 MHz EC Oscillator
		—	—	477		3.0	
		—	—	777		5.0	
D014		—	—	505	μA	2.1	Fosc = 4 MHz EC Oscillator
		—	—	724		3.0	
		—	—	1.30	mA	5.0	
D015		—	—	51	μA	2.1	Fosc = 31 kHz LFINTOSC
		—	—	92		3.0	
		—	—	117	mA	5.0	
D016		—	—	665	μA	2.1	Fosc = 4 MHz HFINTOSC
		—	—	970		3.0	
		—	—	1.56	mA	5.0	
D017		—	—	936	μA	2.1	Fosc = 8 MHz HFINTOSC
		—	—	1.34	mA	3.0	
		—	—	2.27		5.0	
D018		—	—	605	μA	2.1	Fosc = 4 MHz EXTRC
		—	—	903		3.0	
		—	—	1.43	mA	5.0	
D019		—	—	6.61	mA	4.5	Fosc = 20 MHz HS Oscillator
		—	—	7.81		5.0	

PIC16F631/677/685/687/689/690

FIGURE 18-16: BOR I_PD vs. V_DD OVER TEMPERATURE
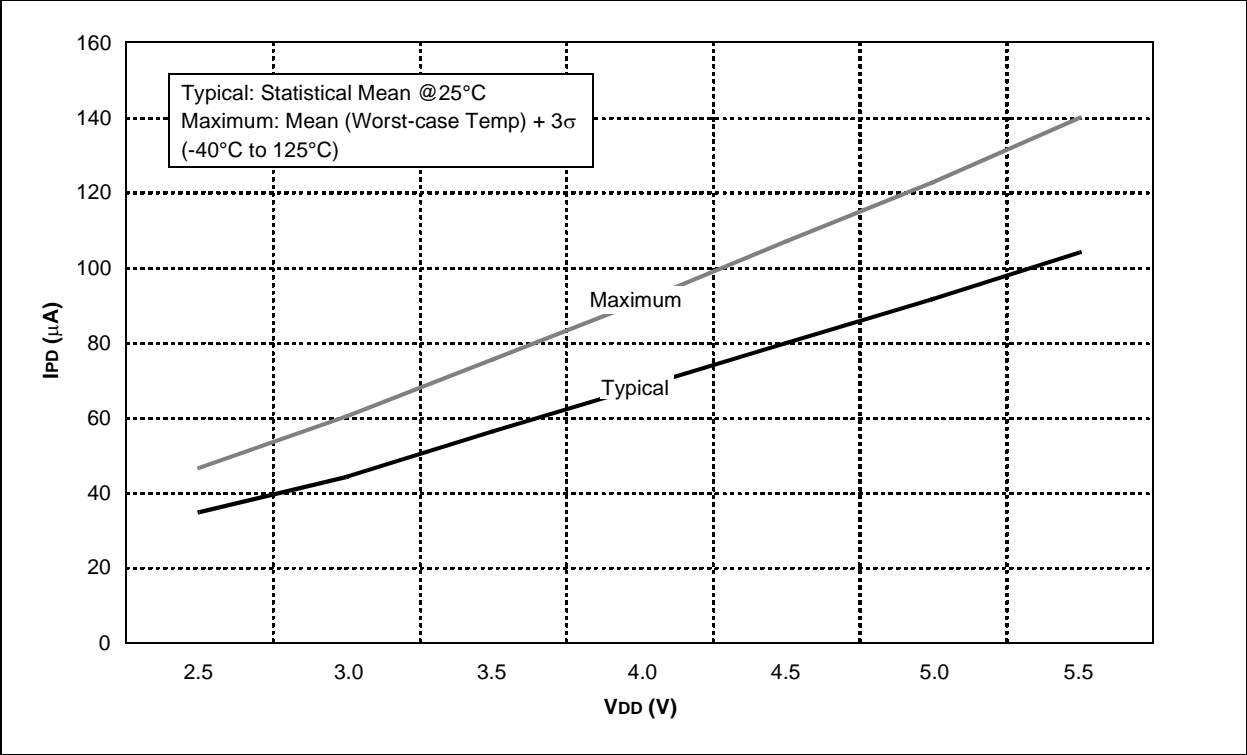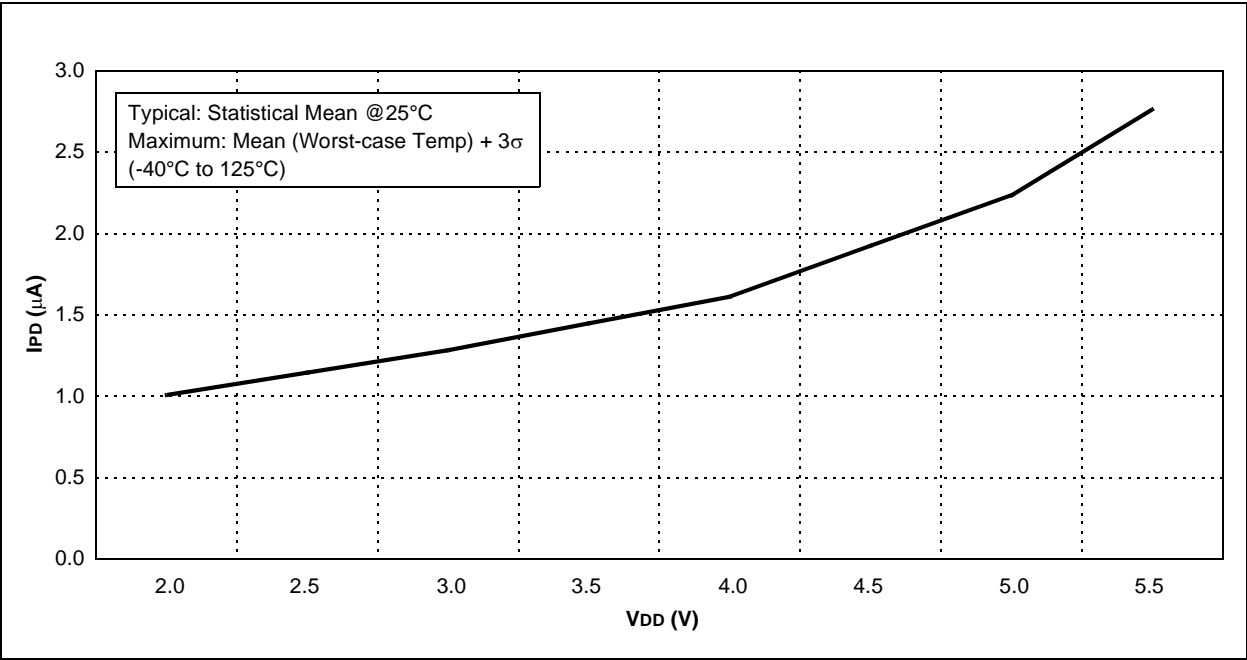

FIGURE 18-17: TYPICAL WDT I_PD vs. V_DD OVER TEMPERATURE

PIC16F631/677/685/687/689/690

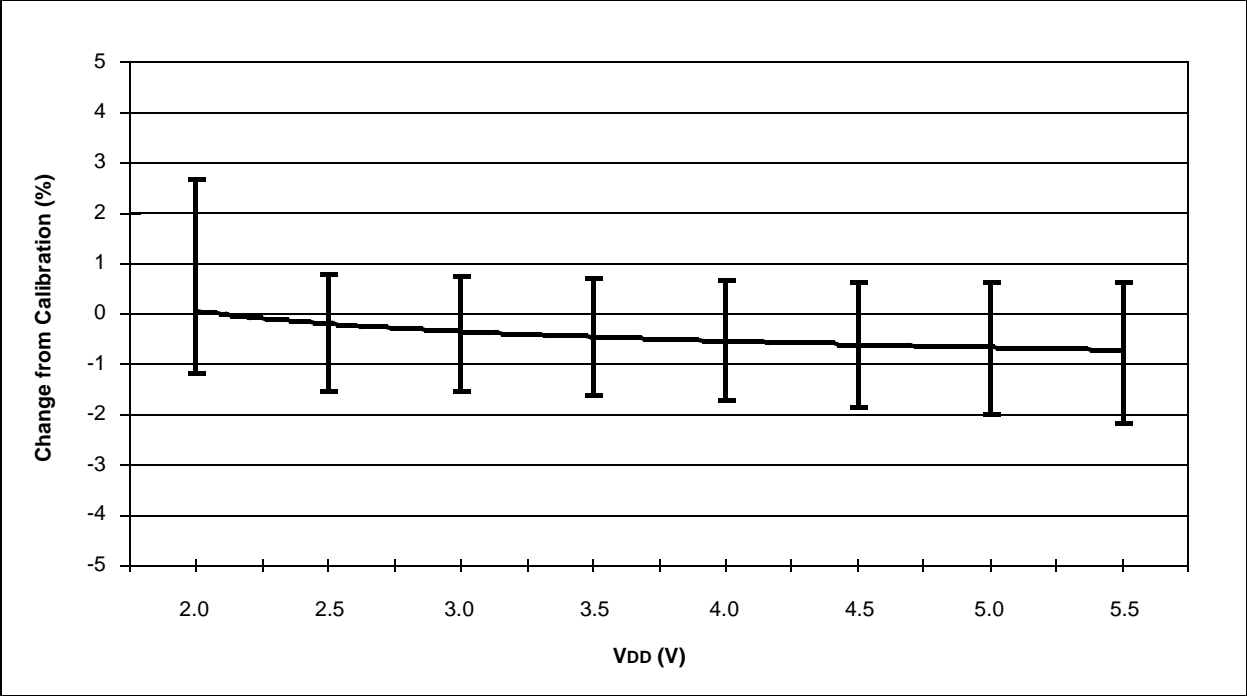**FIGURE 18-40:** **TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE V$_{DD}$ (85°C)**

FIGURE 18-41: **TYPICAL HFINTOSC FREQUENCY CHANGE vs. V$_{DD}$ (125°C)**