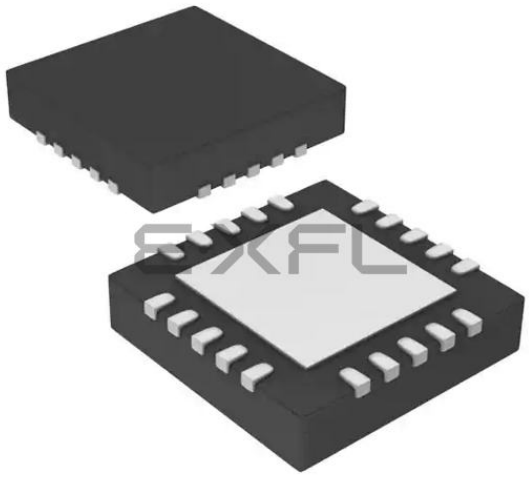

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f685t-i-ml

2.2 Data Memory Organization

The data memory (see Figures 2-6 through 2-8) is partitioned into four banks which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. The General Purpose Registers, implemented as static RAM, are located in the last 96 locations of each Bank. Register locations F0h-FFh in Bank 1, 170h-17Fh in Bank 2 and 1F0h-1FFh in Bank 3 point to addresses 70h-7Fh in Bank 0. The actual number of General Purpose Resisters (GPR) in each Bank depends on the device. Details are shown in Figures 2-4 through 2-8. All other RAM is unimplemented and returns '0' when read. RP<1:0> of the STATUS register are the bank select bits:

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC16F687 and 256 x 8 in the PIC16F685/PIC16F689/PIC16F690. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Tables 2-1 through 2-4). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Registers related to the operation of peripheral features are described in the section of that peripheral feature.

TABLE 2-2: PIC16F631/677/685/687/689/690 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	43,200
81h	OPTION_REG	$\overline{\text{RABPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	36,200
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	43,200
83h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	35,200
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	43,200
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	57,200
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	68,201
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	74,200
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	43,200
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF(1)	0000 000x	37,200
8Ch	PIE1	—	ADIE(4)	RCIE(2)	TXIE(2)	SSPIE(5)	CCP1IE(3)	TMR2IE(3)	TMR1IE	-000 0000	38,201
8Dh	PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----	39,201
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	--01 --qq	42,201
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	46,201
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	50,201
91h	—	Unimplemented								—	—
92h	PR2(3)	Timer2 Period Register								1111 1111	89,201
93h	SSPADD(5, 7)	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	184,201
93h	SSPMSK(5, 7)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111	187,201
94h	SSPSTAT(5)	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	0000 0000	176,201
95h	WPUA(6)	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	60,201
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	60,201
97h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	208,201
98h	TXSTA(2)	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	157,201
99h	SPBRG(2)	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	160,201
9Ah	SPBRGH(2)	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	160,201
9Bh	BAUDCTL(2)	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	159,201
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL(4)	A/D Result Register Low Byte								xxxx xxxx	113,201
9Fh	ADCON1(4)	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	112,201

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: $\overline{\text{MCLR}}$ and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.

2: PIC16F687/PIC16F689/PIC16F690 only.

3: PIC16F685/PIC16F690 only.

4: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

5: PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.

6: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

7: Accessible only when SSPCON register bits SSPM<3:0> = 1001.

4.0 I/O PORTS

There are as many as eighteen general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING PORTA

```
BCF   STATUS,RP0;Bank 0
BCF   STATUS,RP1;
CLRF  PORTA    ;Init PORTA
BSF   STATUS,RP1;Bank 2
CLRF  ANSEL    ;digital I/O
BSF   STATUS,RP0;Bank 1
BCF   STATUS,RP1;
MOVLW 0Ch      ;Set RA<3:2> as inputs
MOVWF TRISA    ;and set RA<5:4,1:0>
               ;as outputs
BCF   STATUS,RP0;Bank 0
```

REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Pin bit
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.
2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

REGISTER 4-3: ANSEL: ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ANS<7:0>**: Analog Select bits
Analog select between analog or digital function on pins AN<7:0>, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 4-4: ANSELH: ANALOG SELECT HIGH REGISTER(2)

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANS11	ANS10	ANS9	ANS8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ANS<11:8>**: Analog Select bits
Analog select between analog or digital function on pins AN<7:0>, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

4.4.3.2 RB5/AN11/RX/DT(1, 2)

Figure 4-8 shows the diagram for this pin. The RB5/AN11/RX/DT pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- an asynchronous serial input
- a synchronous serial data I/O

Note 1:	RX and DT are available on PIC16F687/PIC16F689/PIC16F690 only.
2:	AN11 is not implemented on PIC16F631.

FIGURE 4-8: BLOCK DIAGRAM OF RB5

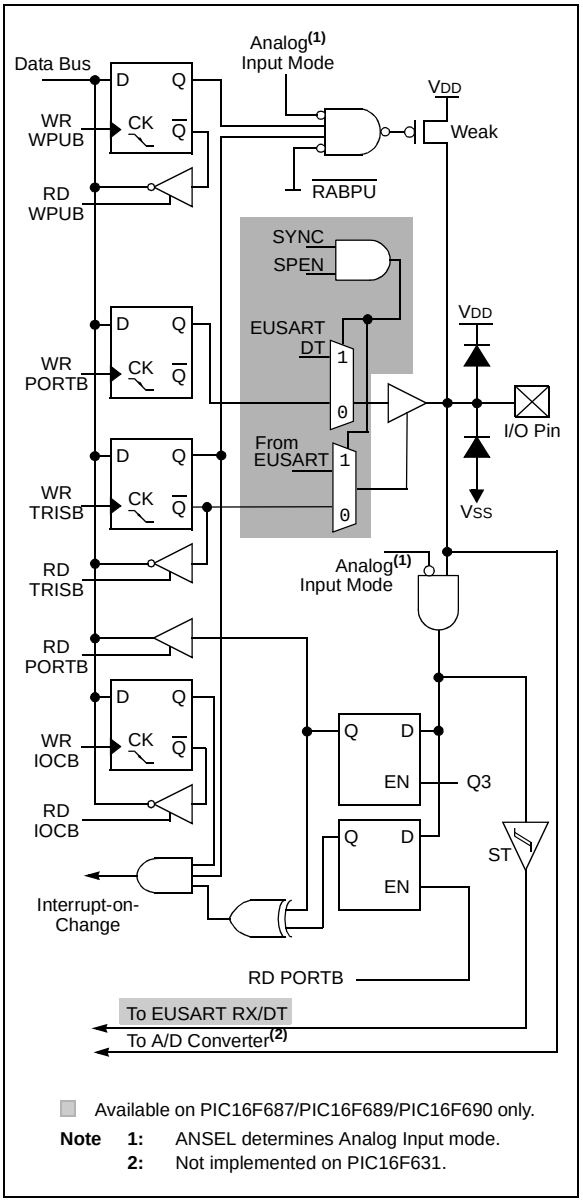
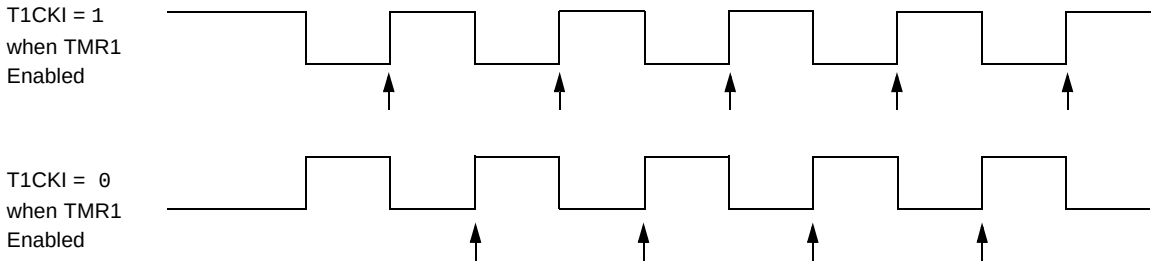


FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

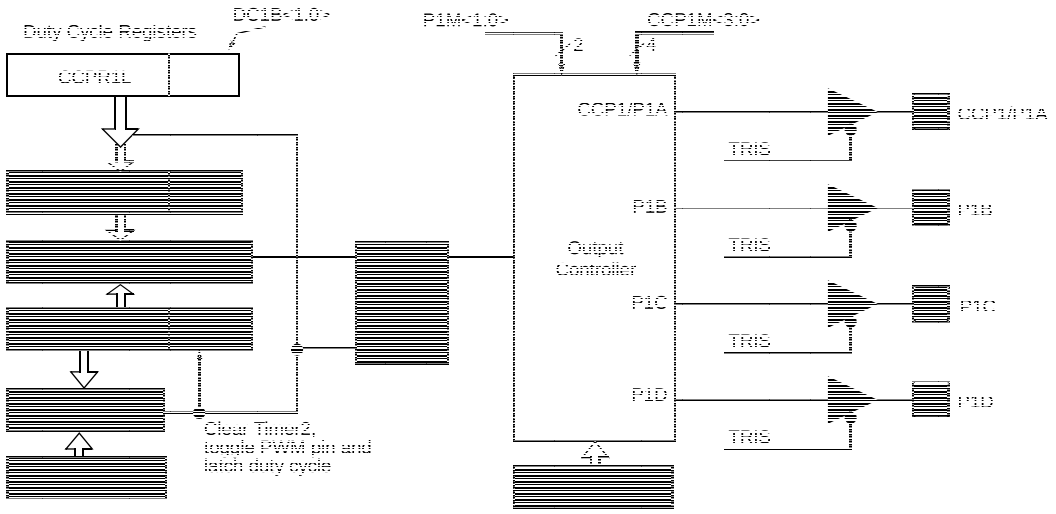
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
EECON1	EEPGD(1)	—	—	—	WRERR	WREN	WR	RD	x--- x000	0--- q000
EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
EEADR	EEADR7(2)	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
EEADRH(1)	—	—	—	—	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---- 0000	---- 0000
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEDATH(1)	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000	--00 0000
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 0000	0000 0000
PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----	0000 ----
PIR2	OSFIF	C2IF	C1IF	EEIF	—	—	—	—	0000 ----	0000 ----

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by data EEPROM module.

Note 1: PIC16F685/PIC16F689/PIC16F690 only.

2: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

FIGURE 11-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler to create the 10-bit time base.

Note 1: The TRIS register value for each PWM output must be configured appropriately.

2: Clearing the CCP1CON register will relinquish ECCP control of all PWM output pins.

3: Any pin not used by an Enhanced PWM mode is available for alternate pin functions

TABLE 11-4: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	P1M<1:0>	CCP1/P1A	P1B	P1C	P1D
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: Pulse Steering enables outputs in Single mode.

REGISTER 11-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
- 1 = A shutdown event has occurred; ECCP outputs are in shutdown state
- 0 = ECCP outputs are operating

bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
- 000 =Auto-Shutdown is disabled
- 001 =Comparator C1 output high
- 010 =Comparator C2 output high(1)
- 011 =Either Comparators output is high
- 100 =VIL on INT pin
- 101 =VIL on INT pin or Comparator C1 output high
- 110 =VIL on INT pin or Comparator C2 output high
- 111 =VIL on INT pin or either Comparators output is high

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
- 00 = Drive pins P1A and P1C to '0'
- 01 = Drive pins P1A and P1C to '1'
- 1x = Pins P1A and P1C tri-state

bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
- 00 = Drive pins P1B and P1D to '0'
- 01 = Drive pins P1B and P1D to '1'
- 1x = Pins P1B and P1D tri-state

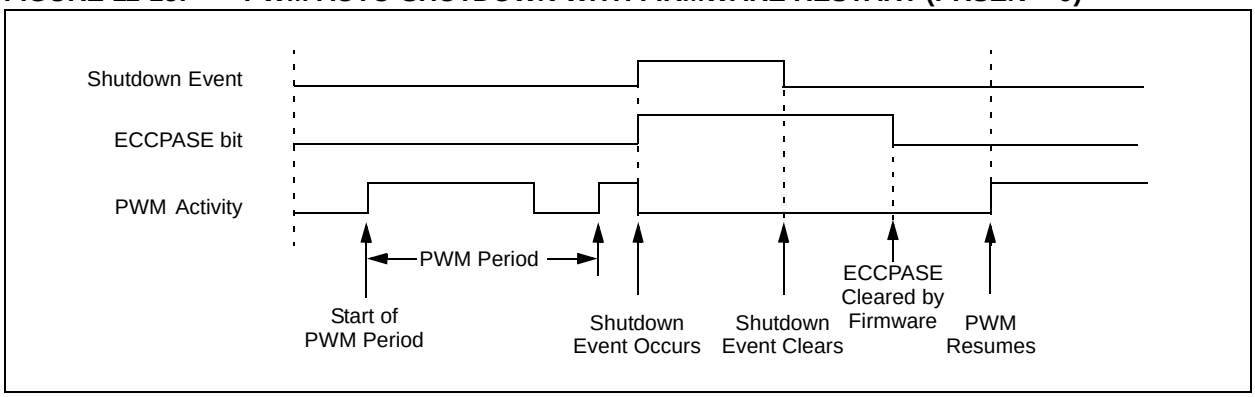
Note 1: If C2SYNC is enabled, the shutdown will be delayed by Timer1.

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.

FIGURE 11-15: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)



11.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 11-16: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)

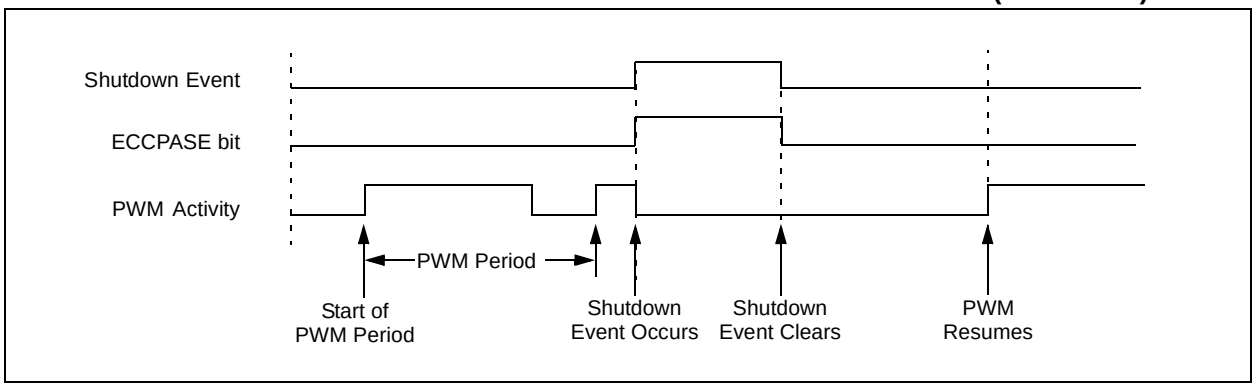
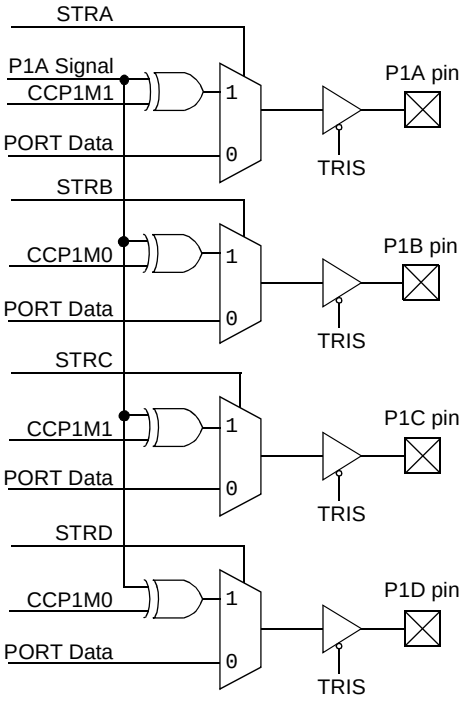


FIGURE 11-19: SIMPLIFIED STEERING BLOCK DIAGRAM



Note 1: Port outputs are configured as shown when the CCP1CON register bits P1M<1:0> = 00 and CCP1M<3:2> = 11.

2: Single PWM output requires setting at least one of the STRx bits.

12.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 12.4.1.5 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

12.4.2.4 Synchronous Slave Reception Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Set the CREN bit to enable reception.
5. The RCIF bit will be set when reception is complete. An interrupt will be generated if the RCIE bit was set.
6. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
7. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
8. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
RCREG	EUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	0000 0000
TRISB	TRISB7	TRISB6	TRISB5	TRISB4					1111 ----	1111 ----
TXREG	EUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010

Legend: x = unknown, – = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

13.12.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no Acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF of the SSPSTAT register is set, or bit SSPOV of the SSPCON register is set. This is an error condition due to the user's firmware.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF of the PIR1 register must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

FIGURE 13-8: I²C™ WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

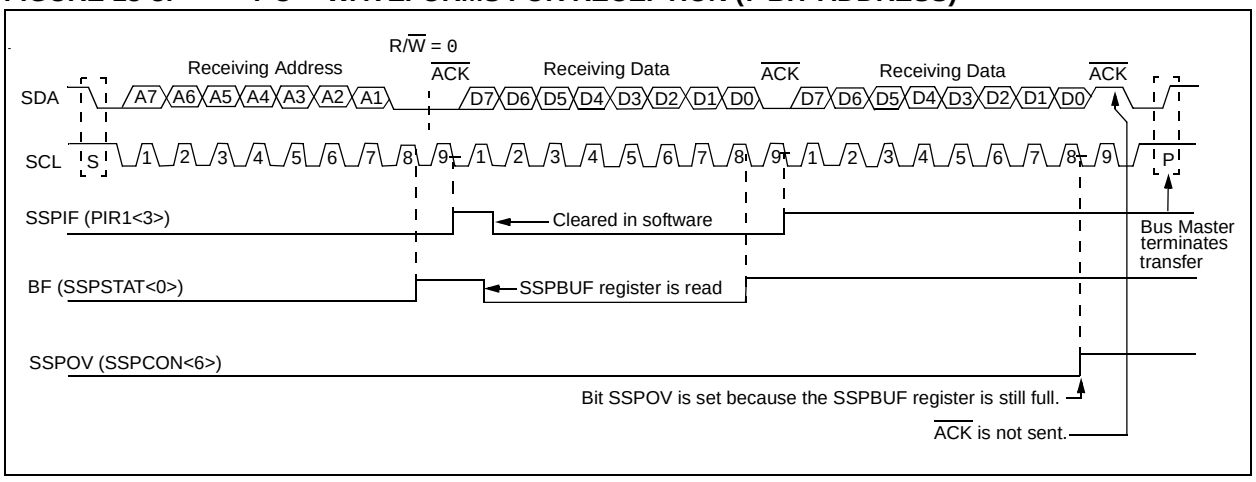
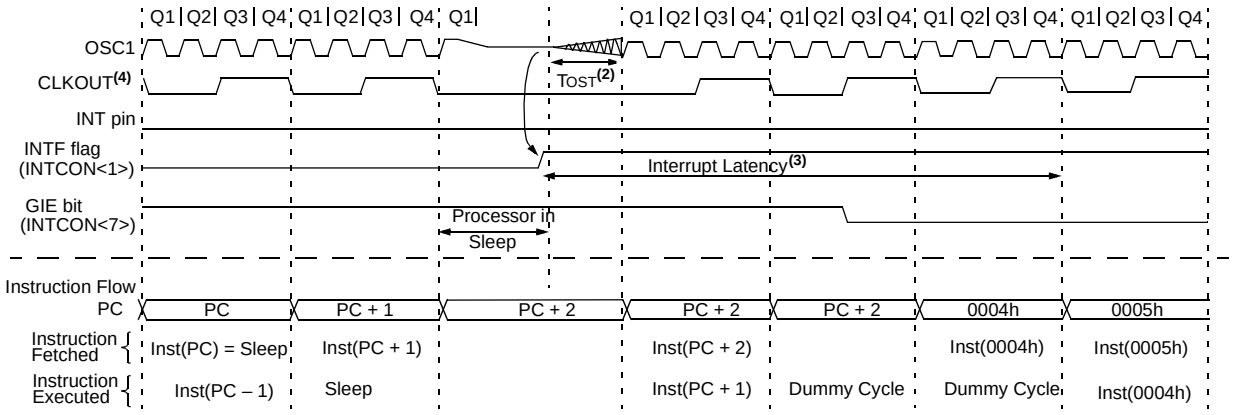


FIGURE 14-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC and RC Oscillator modes.

3: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

14.7 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is switched from on to off. See the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information.

14.8 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant seven bits of the ID locations are used.

14.9 In-Circuit Serial Programming

The PIC16F631/677/685/687/689/690 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0/AN0/C1IN+/ICSPDAT/ULPWU and RA1/AN1/C12IN-/VREF/ICSPCLK pins low, while raising the $\overline{\text{MCLR}}$ (VPP) pin from VIL to VIHH. See the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204).

A typical In-Circuit Serial Programming connection is shown in Figure 14-11.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

CALL	Call Subroutine
Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a 2-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

17.2 DC Characteristics: PIC16F631/677/685/687/689/690-I (Industrial) PIC16F631/677/685/687/689/690-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)(1, 2)**	—	13	19	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	22	30	µA	3.0	
		—	33	60	µA	5.0	
D011*		—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	220	380	µA	3.0	
		—	380	550	µA	5.0	
D012		—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	420	650	µA	3.0	
		—	0.8	1.1	mA	5.0	
D013*		—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	215	360	µA	3.0	
		—	360	520	µA	5.0	
D014		—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	375	550	µA	3.0	
		—	0.65	1.0	mA	5.0	
D015		—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
		—	16	40	µA	3.0	
		—	31	65	µA	5.0	
D016*		—	340	450	µA	2.0	FOSC = 4 MHz HFINTOSC mode
		—	500	700	µA	3.0	
		—	0.8	1.2	mA	5.0	
D017		—	410	650	µA	2.0	FOSC = 8 MHz HFINTOSC mode
		—	700	950	µA	3.0	
		—	1.30	1.65	mA	5.0	
D018		—	230	400	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	400	680	µA	3.0	
		—	0.63	1.1	mA	5.0	
D019		—	3.8	5.0	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	4.0	5.45	mA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

5: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

FIGURE 18-38: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

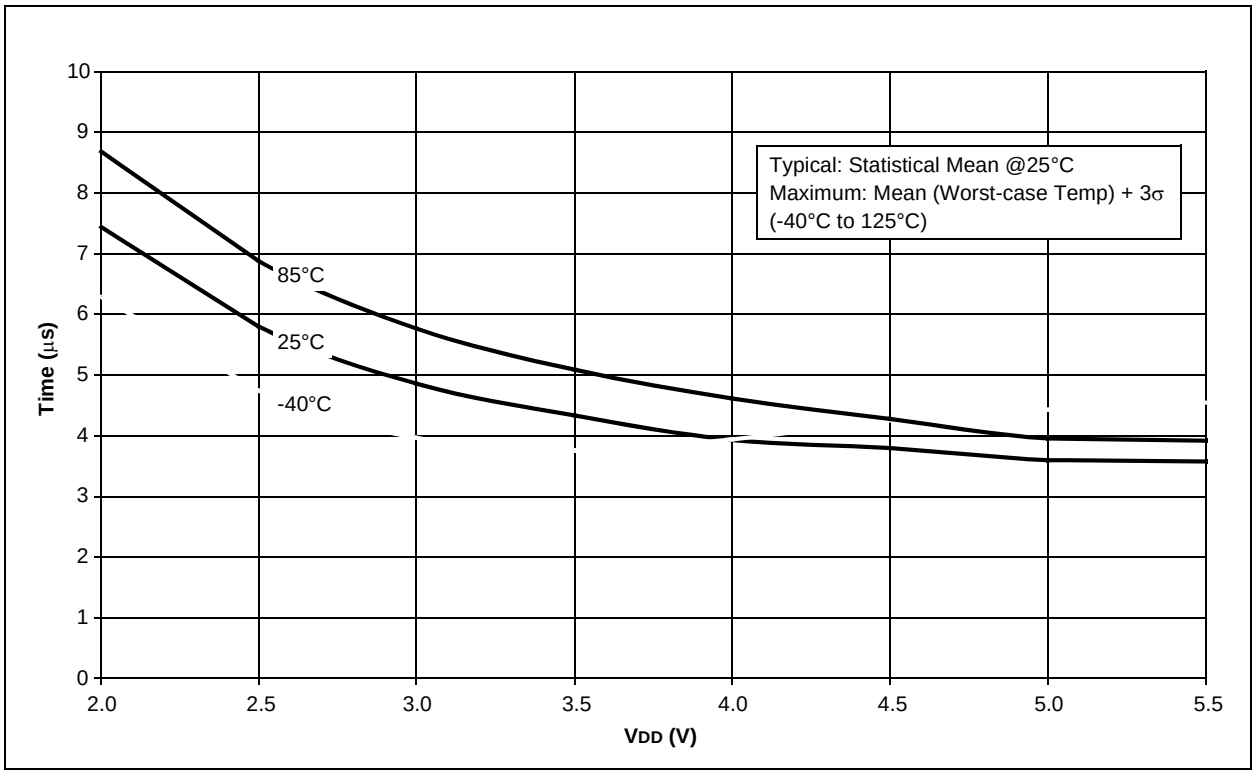


FIGURE 18-39: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

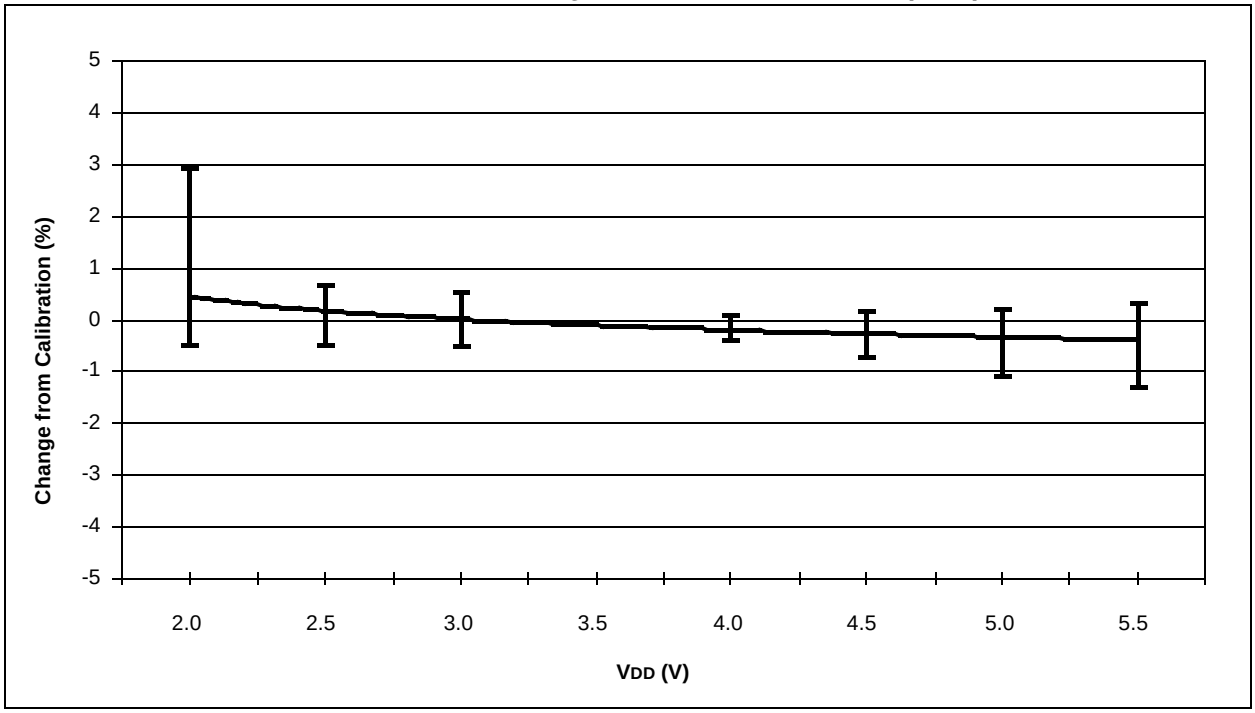


FIGURE 18-42: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)

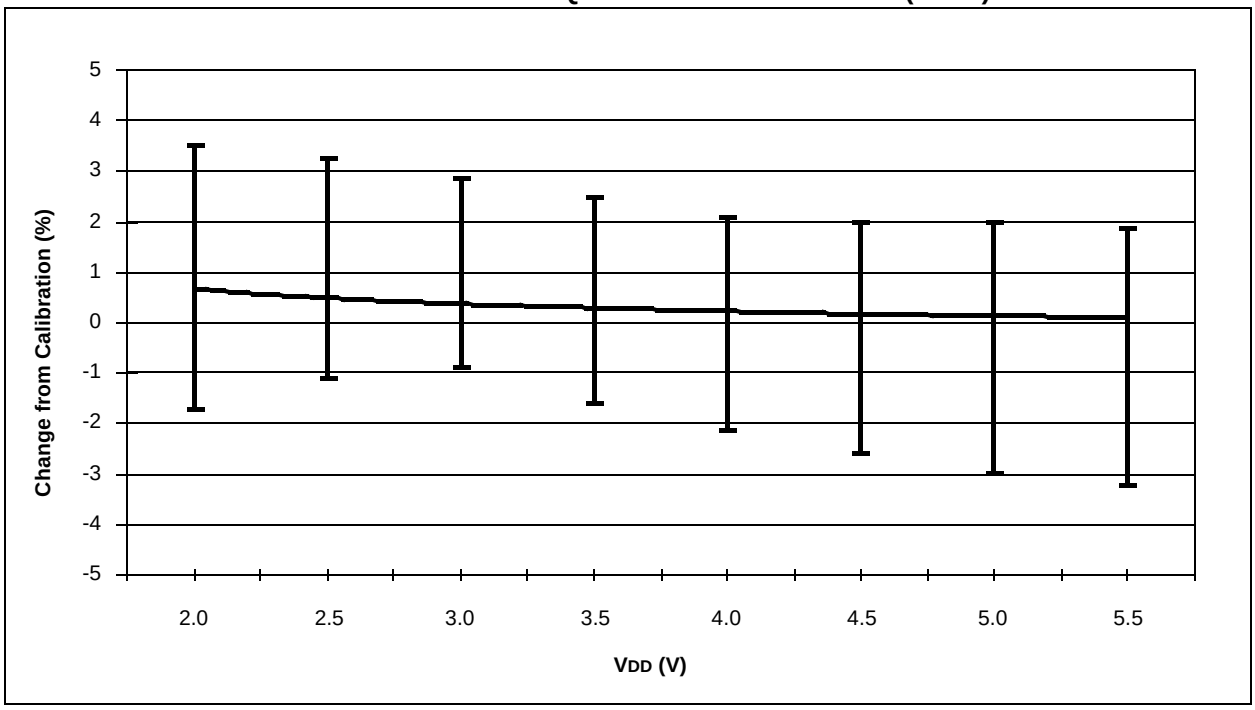


FIGURE 18-43: TYPICAL VP6 REFERENCE VOLTAGE vs. VDD (25°C)

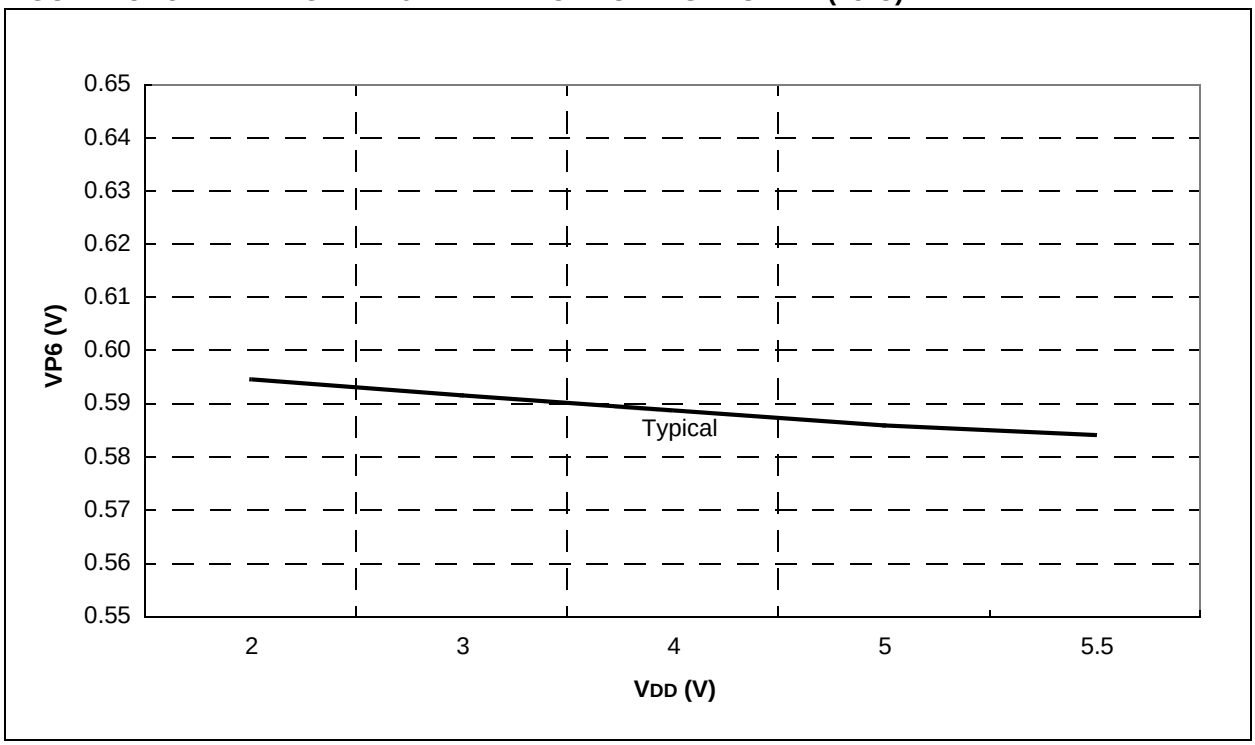


FIGURE 18-52: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (5V, 125°C)

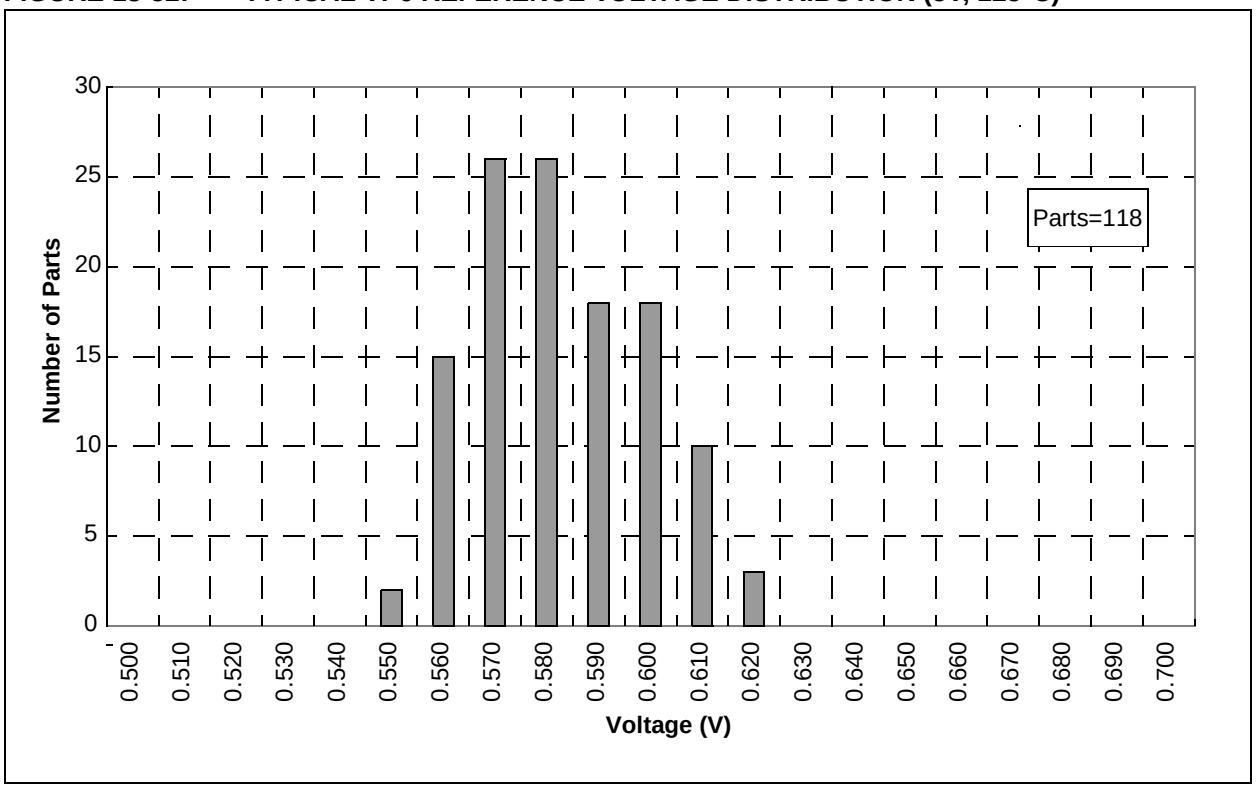
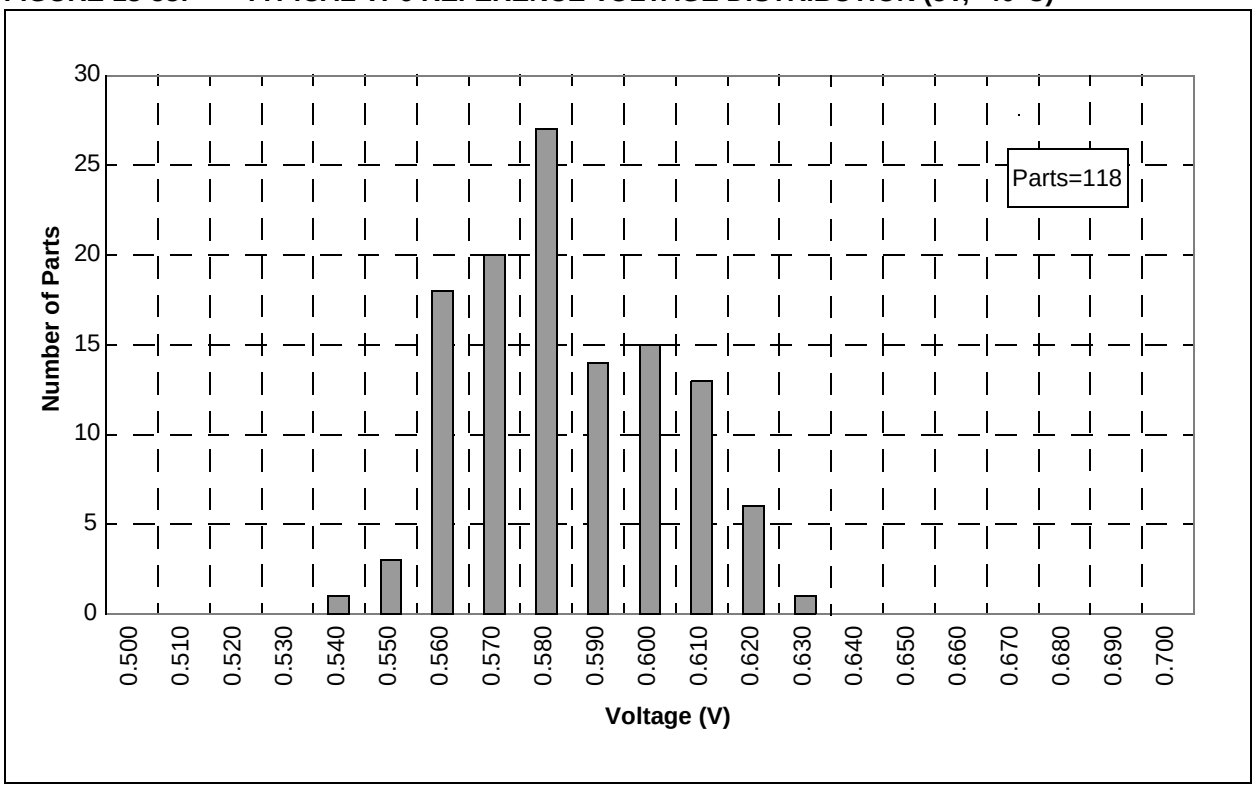


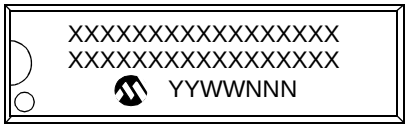
FIGURE 18-53: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (5V, -40°C)



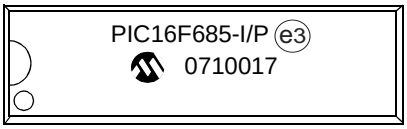
19.0 PACKAGING INFORMATION

19.1 Package Marking Information

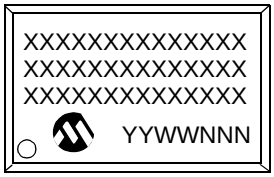
20-Lead PDIP



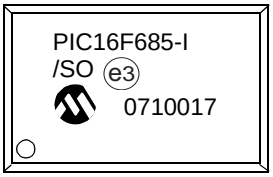
Example



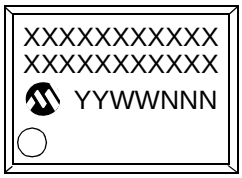
20-Lead SOIC (7.50 mm)



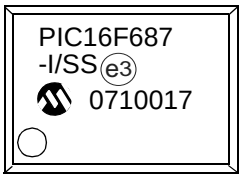
Example



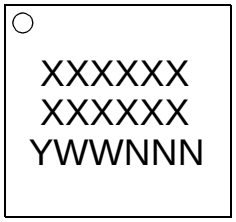
20-Lead SSOP



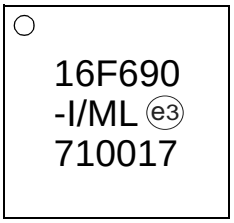
Example



20-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.