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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f685t-i-ss

PIC16F631/677/685/687/689/690

TABLE 1-5: PINOUT DESCRIPTION – PIC16F690

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN0	AN	—	A/D Channel 0 input.
	C1IN+	AN	—	Comparator C1 positive input.
	ICSPDAT	TTL	CMOS	ICSP™ Data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/AN1/C12IN0-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN1	AN	—	A/D Channel 1 input.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF	AN	—	External Voltage Reference for A/D.
	ICSPCLK	ST	—	ICSP™ clock.
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN2	AN	—	A/D Channel 2 input.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
RA3/MCLR/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	MCLR	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/AN3/T1G/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN3	AN	—	A/D Channel 3 input.
	T1G	ST	—	Timer1 gate input.
	OSC2	—	XTAL	Crystal/Resonator.
	CLKOUT	—	CMOS	Fosc/4 output.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	T1CKI	ST	—	Timer1 clock input.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	External clock input/RC oscillator connection.
RB4/AN10/SDI/SDA	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	SDI	ST	—	SPI data input.
	SDA	ST	OD	I ² C™ data input/output.
RB5/AN11/RX/DT	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.

Legend: AN = Analog input or output CMOS=CMOS compatible input or output OD= Open Drain
TTL = TTL compatible input ST= Schmitt Trigger input with CMOS levels
HV = High Voltage XTAL= Crystal

PIC16F631/677/685/687/689/690

TABLE 2-2: PIC16F631/677/685/687/689/690 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	43,200
81h	OPTION_REG	RABPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	36,200
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	43,200
83h	STATUS	IRP	RP1	RP0	T0	PD	Z	DC	C	0001 1xxx	35,200
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	43,200
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	57,200
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	68,201
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	74,200
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				---	0 0000	43,200
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF ⁽¹⁾	0000 000x	37,200
8Ch	PIE1	—	ADIE ⁽⁴⁾	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE ⁽⁵⁾	CCP1IE ⁽³⁾	TMR2IE ⁽³⁾	TMR1IE	-000 0000	38,201
8Dh	PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----	39,201
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	POR	BOR	--01 --q q	42,201
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	46,201
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	50,201
91h	—	Unimplemented								—	—
92h	PR2 ⁽³⁾	Timer2 Period Register								1111 1111	89,201
93h	SSPADD ^(5, 7)	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	184,201
93h	SSPMSK ^(5, 7)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111	187,201
94h	SSPSTAT ⁽⁵⁾	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	176,201
95h	WPUA ⁽⁶⁾	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	60,201
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	60,201
97h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	208,201
98h	TXSTA ⁽²⁾	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	157,201
99h	SPBRG ⁽²⁾	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	160,201
9Ah	SPBRGH ⁽²⁾	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	160,201
9Bh	BAUDCTL ⁽²⁾	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	159,201
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL ⁽⁴⁾	A/D Result Register Low Byte								xxxx xxxx	113,201
9Fh	ADCON1 ⁽⁴⁾	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	112,201

- Legend:** — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
- Note** 1: MCLR and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.
- 2: PIC16F687/PIC16F689/PIC16F690 only.
- 3: PIC16F685/PIC16F690 only.
- 4: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.
- 5: PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.
- 6: RA3 pull-up is enabled when pin is configured as MCLR in Configuration Word.
- 7: Accessible only when SSPCON register bits SSPM<3:0> = 1001.

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FIGURE 3-9: FSCM TIMING DIAGRAM

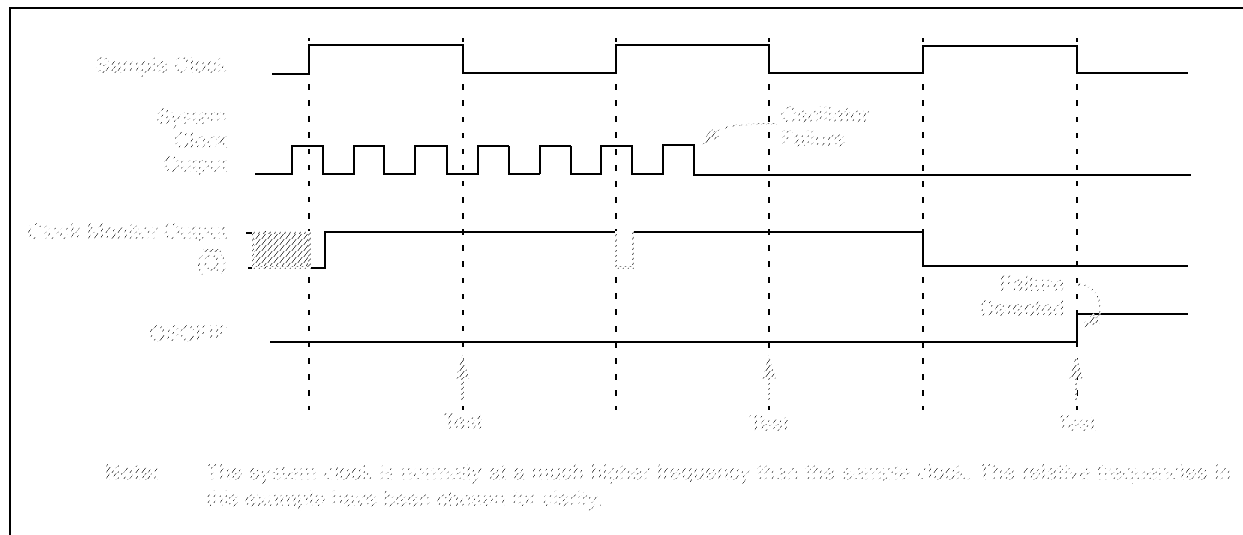


TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 14-1) for operation of all register bits.

PIC16F631/677/685/687/689/690

4.2.5 PIN DESCRIPTIONS AND DIAGRAMS

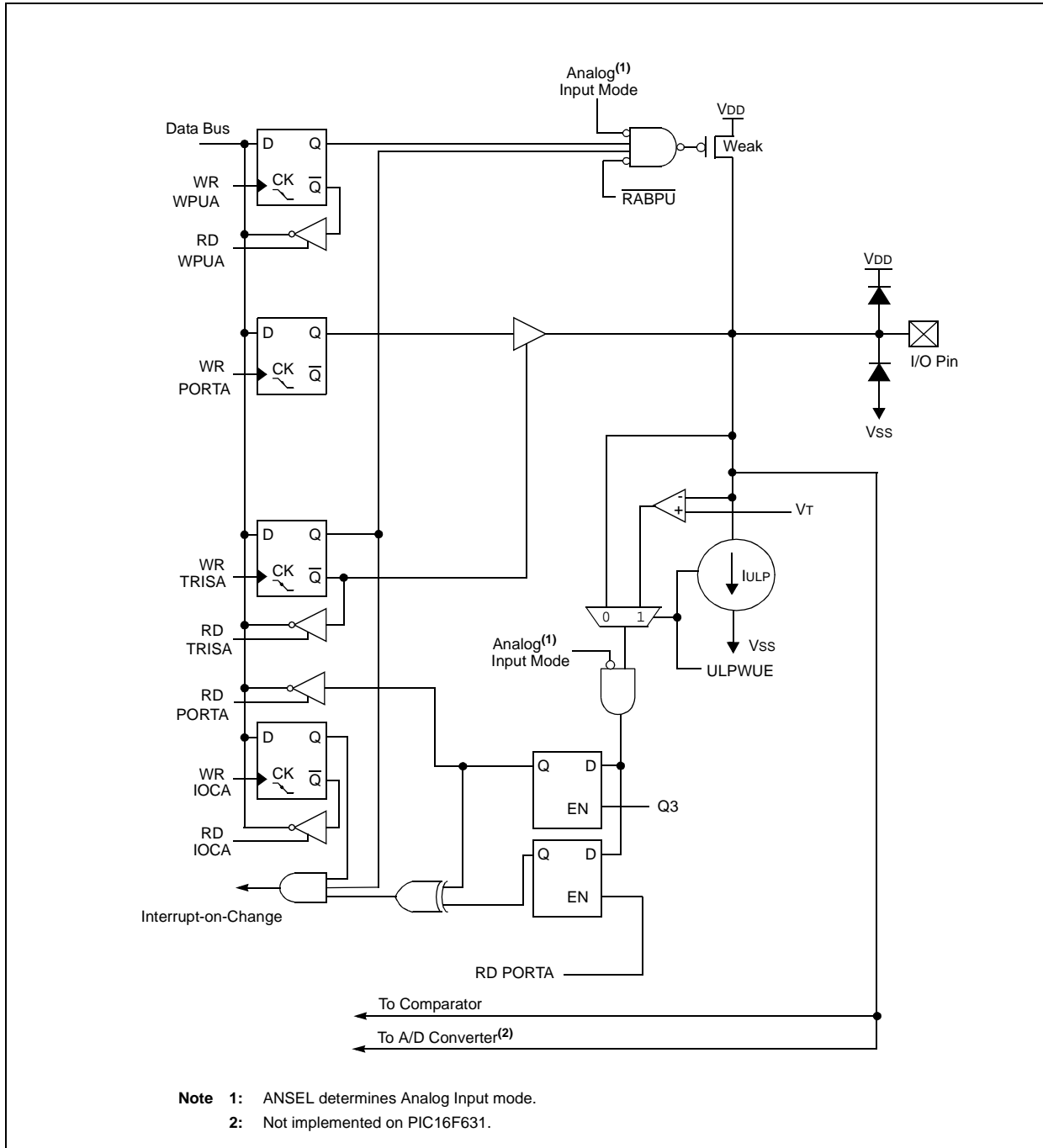
Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D Converter (ADC), refer to the appropriate section in this data sheet.

4.2.5.1 RA0/AN0/C1IN+/ICSPDAT/ULPWU

Figure 4-2 shows the diagram for this pin. The RA0/AN0/C1IN+/ICSPDAT/ULPWU pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- an analog input to Comparator C1
- In-Circuit Serial Programming™ data
- an analog input for the Ultra Low-Power Wake-up

FIGURE 4-1: BLOCK DIAGRAM OF RA0



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4.4.3.3 RB6/SCK/SCL

Figure 4-9 shows the diagram for this pin. The RB6/SCK/SCL⁽¹⁾ pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI clock
- an I²C™ clock

Note 1: SCK and SCL are available on PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.

FIGURE 4-9: BLOCK DIAGRAM OF RB6

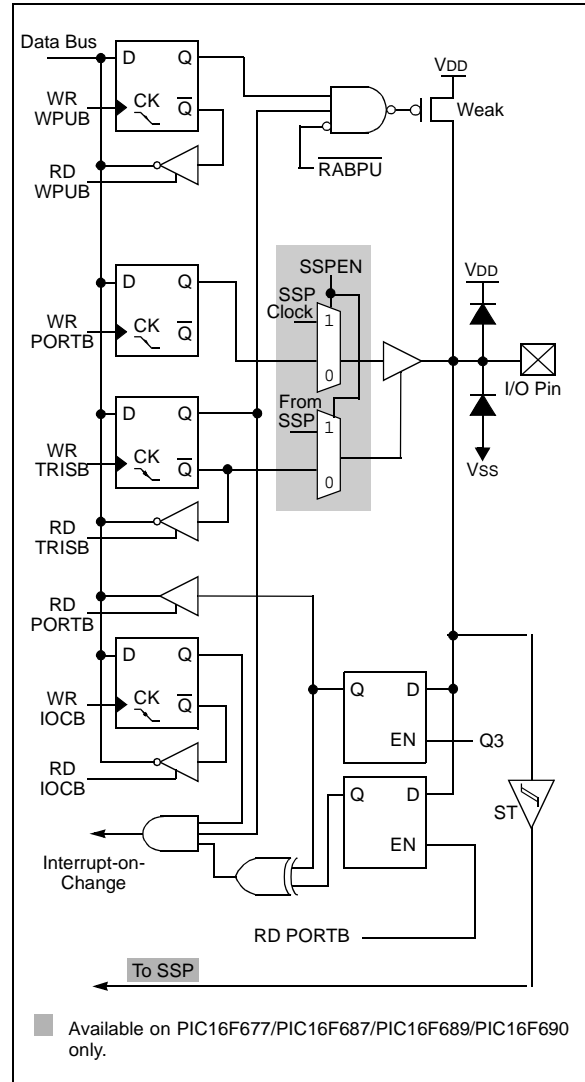


Figure 4-10 shows the diagram for this pin. The RB7/TX/CK⁽¹⁾ pin is configurable to function as one of the following:

- Note 1:** TX and CK are available on PIC16F687/
PIC16F689/PIC16F690 only.

The diagram illustrates the internal logic of the PIC16F687/688/690, specifically the I/O Pin driver and its connection to the Data Bus and various control signals. The circuit includes several registers and logic blocks:

- Data Bus:** Connected to the D input of the first D flip-flop.
- WR WPUB, RD WPUB:** Control signals for the first D flip-flop.
- WR PORTB, WR TRISB, RD TRISB, RD PORTB:** Control signals for the second, third, and fourth D flip-flops.
- WR IOCB, RD IOCB:** Control signals for the fifth D flip-flop.
- Interrupt-on-Change:** A logic block that generates an interrupt signal based on changes in the I/O Pin state.
- I/O Pin Driver:** A logic block that drives the I/O Pin based on the output of the fifth D flip-flop and the Interrupt-on-Change signal.
- I/O Pin:** The external pin connected to VDD and VSS, with a pull-up resistor (Weak) and a pull-down resistor (VSS).

The diagram shows the internal logic of the I/O Pin driver, including the RABPU, SPEN, TXEN, SYNC, EUSART, and the I/O Pin driver. The I/O Pin driver is connected to VDD and VSS, and the I/O Pin is connected to VDD and VSS.

Available on PIC16F687/PIC16F689/PIC16F690 only.



12.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.
--

12.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

12.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

12.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

12.5 EUSART Operation During Sleep

The EUSART WILL remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

12.5.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see **Section 12.4.2.4 “Synchronous Slave Reception Set-up:”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE Global Interrupt Enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

12.5.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (see **Section 12.4.2.2 “Synchronous Slave Transmission Set-up:”**).
 - The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
9. If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE Global Interrupt Enable bit is also set then the Interrupt Service Routine at address 0004h will be called.

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FIGURE 13-12: CLOCK SYNCHRONIZATION TIMING

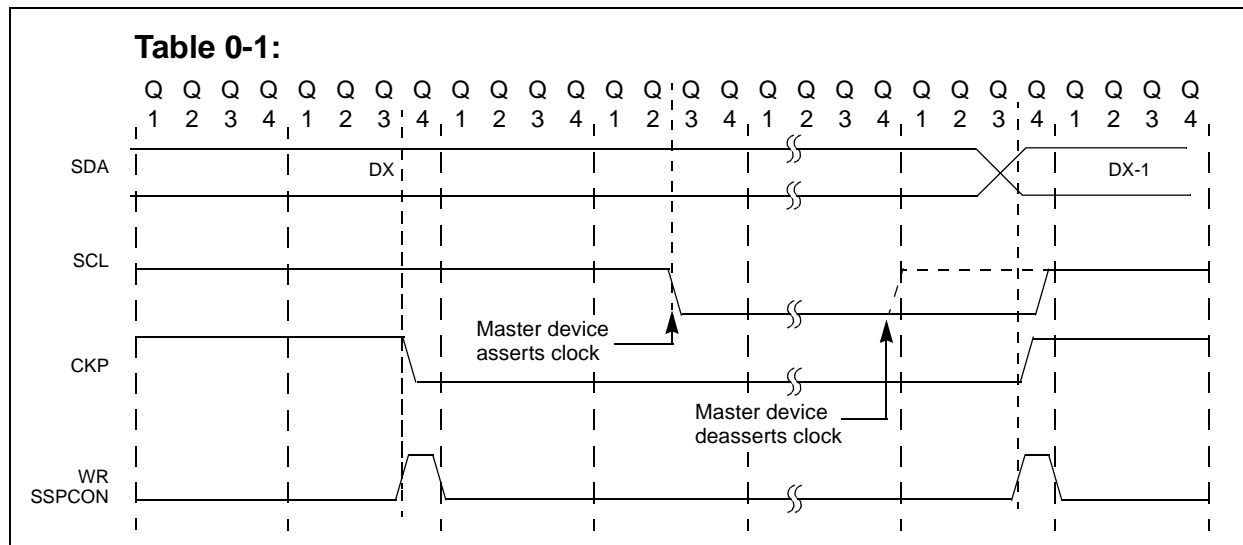


TABLE 13-4: REGISTERS ASSOCIATED WITH I²C™ OPERATION⁽¹⁾

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh/8Bh/ 10Bh/18Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
0Ch	PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	—000 0000	—000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
93h	SSPMSK ⁽²⁾	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111	1111 1111
94h	SSPSTAT	SMP ⁽³⁾	CKE ⁽³⁾	D/A	P	S	R/W	UA	BF	0000 0000	0000 0000
8Ch	PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IF	TMR1IF	—000 0000	—000 0000

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the SSP module.

Note 1: PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.

Note 2: SSPMSK register (Register 13-3) can be accessed by reading or writing to SSPADD register with bits SSPM<3:0> = 1001. See Registers 13-2 and 13-3 for more details.

Note 3: Maintain these bits clear.

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14.2.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. A maximum rise time for VDD is required. See **Section 17.0 “Electrical Specifications”** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see **Section 14.2.4 “Brown-out Reset (BOR)”**).

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach VSS for a minimum of 100 μ s.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, “Power-up Trouble Shooting” (DS00607).

14.2.2 $\overline{\text{MCLR}}$

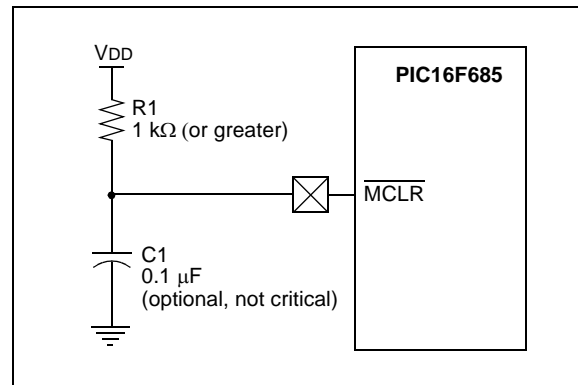
PIC16F631/677/685/687/689/690 has a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

The behavior of the ESD protection on the $\overline{\text{MCLR}}$ pin has been altered from early devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{\text{MCLR}}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{\text{MCLR}}$ pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 14-2, is suggested.

An internal $\overline{\text{MCLR}}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When $\overline{\text{MCLRE}} = 0$, the Reset signal to the chip is generated internally. When the $\overline{\text{MCLRE}} = 1$, the RA3/ $\overline{\text{MCLR}}$ pin becomes an external Reset input. In this mode, the RA3/ $\overline{\text{MCLR}}$ pin has a weak pull-up to VDD. However, for robustness in noisy environments, the circuit shown in Figure 14-2 is still recommended.

FIGURE 14-2: RECOMMENDED $\overline{\text{MCLR}}$ CIRCUIT



14.2.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 “Internal Clock Modes”**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, $\overline{\text{PWRTE}}$, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip and vary due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 17.0 “Electrical Specifications”**).

14.6 Power-Down Mode (Sleep)

The Power-Down mode is entered by executing a `SLEEP` instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- \overline{PD} bit in the STATUS register is cleared.
- \overline{TO} bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at V_{DD} or V_{SS} , with no external circuitry drawing current from the I/O pin and the comparators and CV_{REF} should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The $T0CKI$ input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The \overline{MCLR} pin must be at a logic high level.

Note: It should be noted that a Reset generated by a WDT time-out does not drive \overline{MCLR} pin low.

14.6.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on \overline{MCLR} pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from RA2/INT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The \overline{TO} and \overline{PD} bits in the STATUS register can be used to determine the cause of device Reset. The \overline{PD} bit, which is set on power-up, is cleared when Sleep is invoked. \overline{TO} bit is cleared if WDT Wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is FRC).
4. EEPROM write operation completion.
5. Comparator output changes state.
6. Interrupt-on-change.
7. External Interrupt from INT pin.
8. EUSART Break detect, I^2C slave.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the `SLEEP` instruction is being executed, the next instruction ($PC + 1$) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. The `SLEEP` instruction is completely executed.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

14.6.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the \overline{TO} bit will not be set and the \overline{PD} bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from Sleep. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the \overline{TO} bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the WDT is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

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FIGURE 17-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

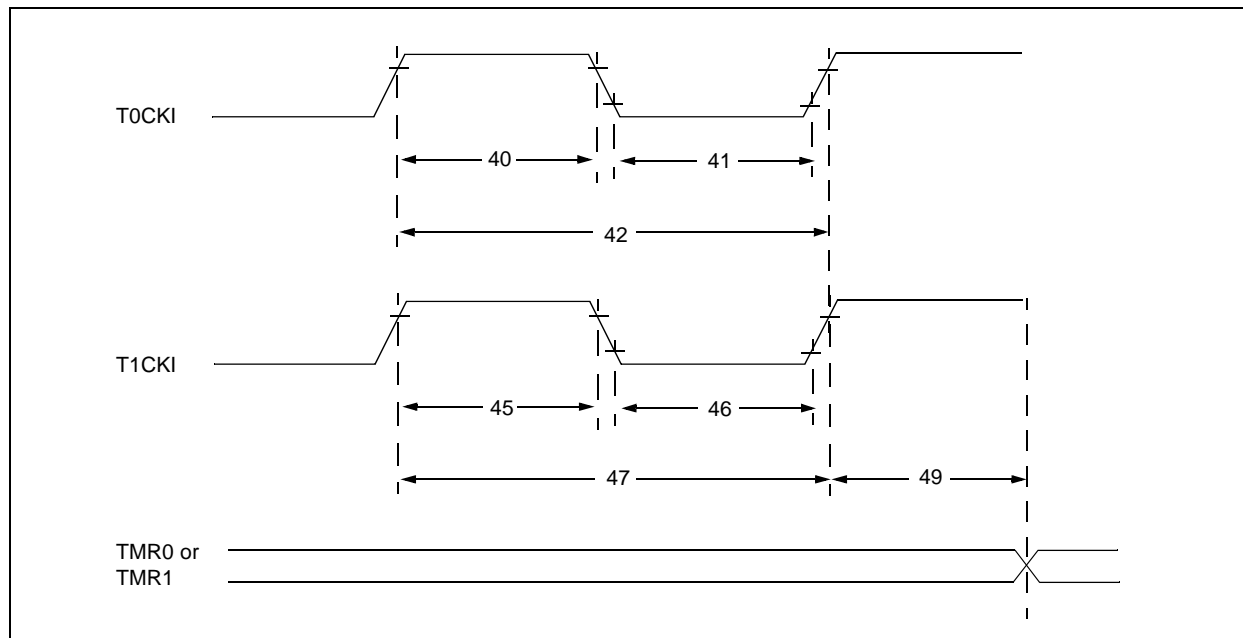


TABLE 17-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$								
Param No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	Ft1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		$2 T_{OSC}$	—	$7 T_{OSC}$	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 17-19: A/D CONVERSION TIMING (SLEEP MODE)

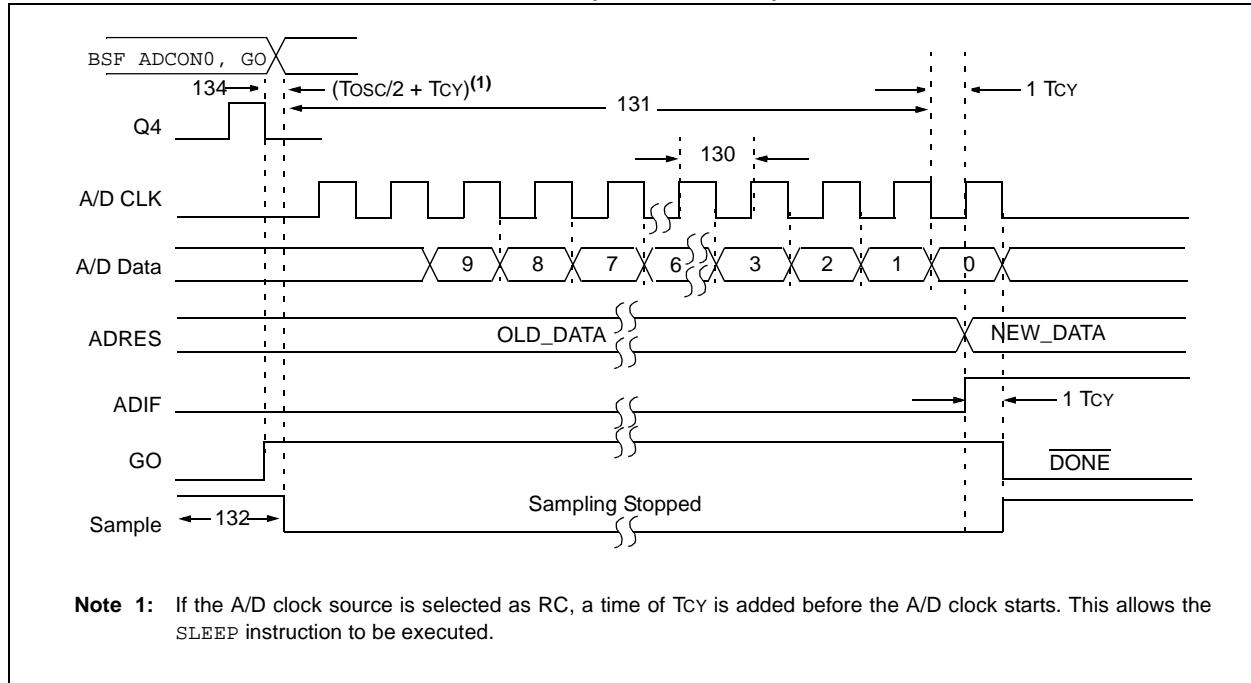


TABLE 1: A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
130*	TAD	A/D Internal RC Oscillator Period	3.0*	6.0	9.0*	μs	ADCS<1:0> = 11 (RC mode) At $V_{DD} = 2.5\text{V}$ At $V_{DD} = 5.0\text{V}$
			2.0*	4.0	6.0*	μs	
131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	
132*	TACQ	Acquisition Time	(2)	11.5	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSB (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
			5*	—	—	μs	
134	TGO	Q4 to A/D Clock Start	—	$T_{OSC}/2 + T_{CY}$	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the <code>SLEEP</code> instruction to be executed.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Table 9-1 for minimum conditions.

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TABLE 17-18: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES ($V_{DD} \geq 3.0V$, $V_{REF} \geq 2.5V$)

ADC Clock Period (T_{AD})		Device Frequency (F_{osc})			
ADC Clock Source	ADCS<2:0>	20 MHz	8 MHz	4 MHz	1 MHz
$F_{osc}/2$	000	100 ns	250 ns	500 ns	2.0 μs
$F_{osc}/4$	100	200 ns	500 ns	1.0 μs	4.0 μs
$F_{osc}/8$	001	400 ns	1.0 μs	2.0 μs	8.0 μs
$F_{osc}/16$	101	800 ns	2.0 μs	4.0 μs	16.0 μs
$F_{osc}/32$	010	1.6 μs	4.0 μs	8.0 μs	32.0 μs
$F_{osc}/64$	110	3.2 μs	8.0 μs	16.0 μs	64.0 μs
Frc	x11	2-6 μs	2-6 μs	2-6 μs	2-6 μs

Legend: Shaded cells should not be used for conversions at temperatures above +125°C.

Note 1: T_{AD} must be between 1.6 μs and 4.0 μs .

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FIGURE 18-38: MINIMUM HFINTOSC START-UP TIMES vs. V_{DD} OVER TEMPERATURE

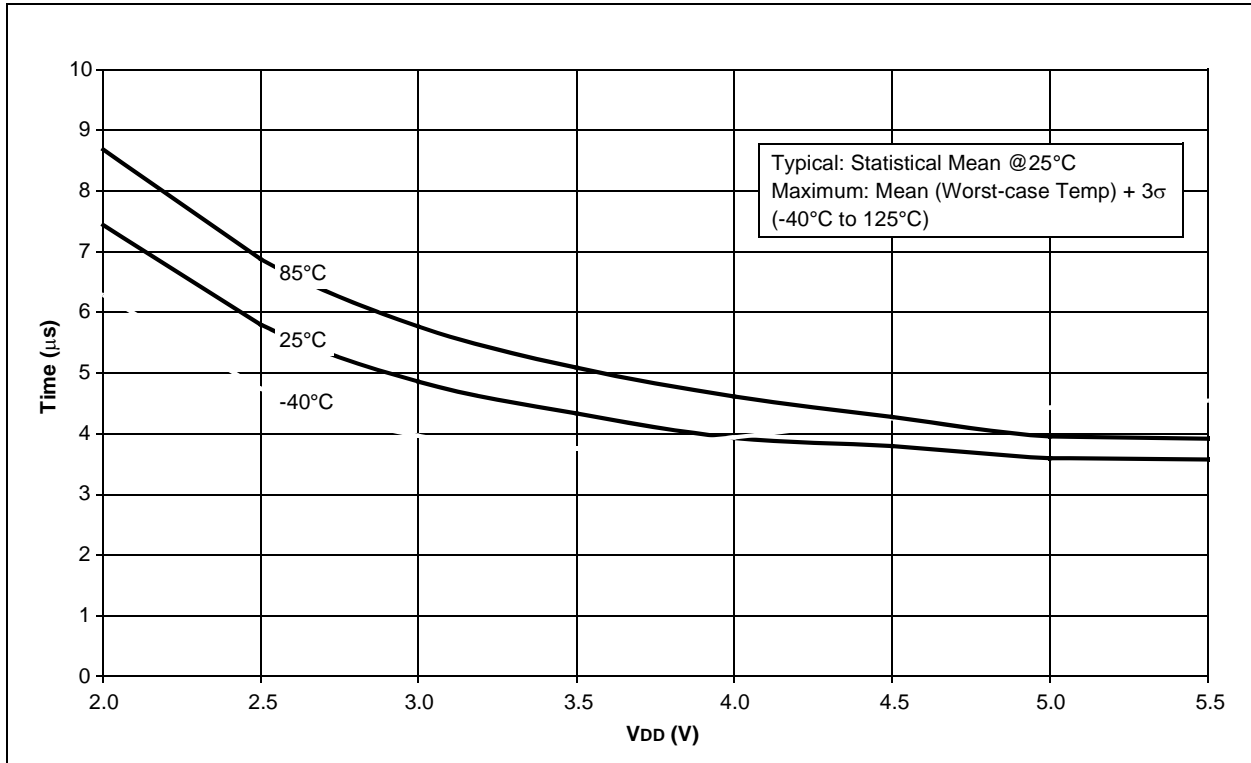
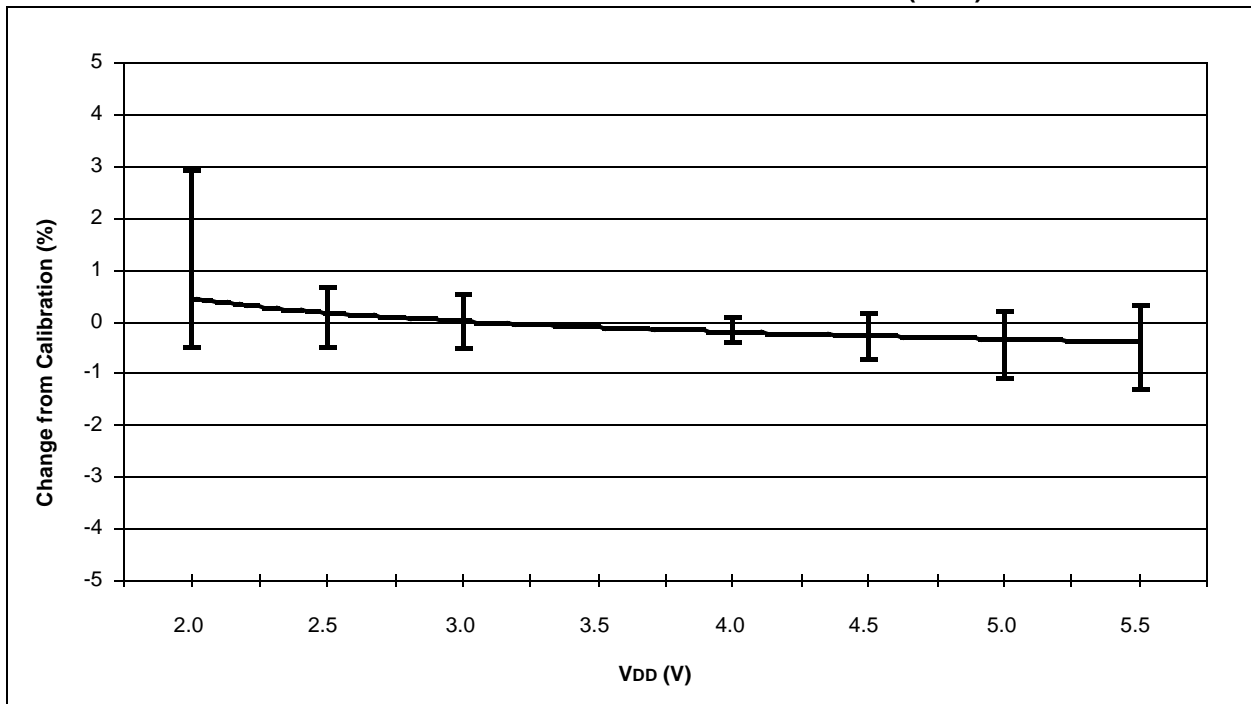


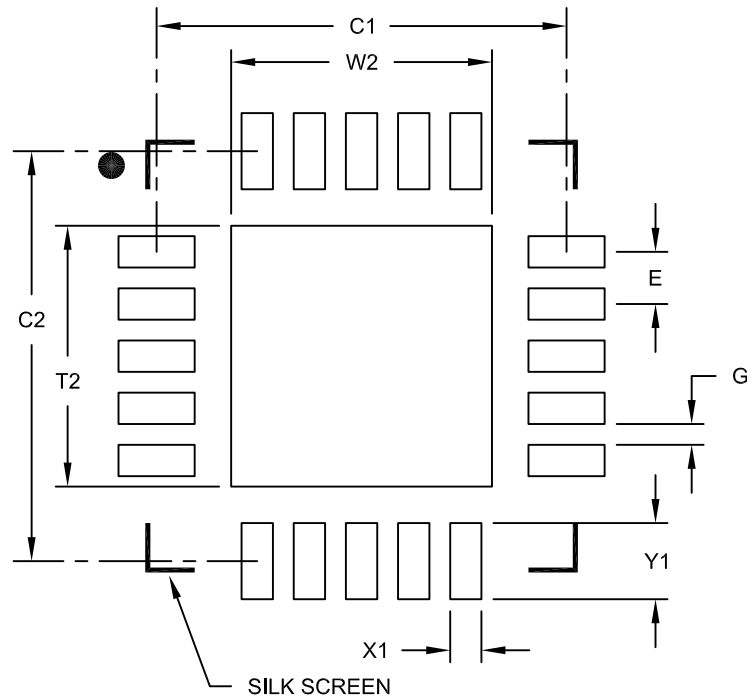
FIGURE 18-39: TYPICAL HFINTOSC FREQUENCY CHANGE vs. V_{DD} (25°C)



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20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (March 2005)

This is a new data sheet.

Revision B (May 2006)

Added 631/677 part numbers; Added pin summary tables after pin diagrams; Incorporated Golden Chapters.

Revision C (July 2006)

Revised Section 4.2.1, ANSEL and ANSELH Registers; Register 4-3, ANSEL Analog Select; Added Register 4-4, ANSELH Analog Select High; Section 11.3.2, Revised CCP1<1:0> to DC1B<1:0>; Section 11.3.7, Number 4 - Revised CCP1 to DC1B; Figure 11-5, Revised CCP1 to DC1B; Table 11-4, Revised P1M to P1M<1:0>; Section 12.3.1, Revised Paragraph 3; Revised Note 2; Revised Figure 12-6 Title.

Revision D (February 2007)

Removed Preliminary status; Changed PICmicro to PIC; Replaced Dev. Tool Section; Replaced Package Drawings.

Revision E (March 2008)

Add Char Data charts; Updated EUSART Golden Chapter; Updated the Electrical Specification section; Updated Package Drawings as needed.

Revision F (April 2015)

Added Section 17.8: High Temperature Operation in the Electrical Specifications section.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC16F6XX Family of devices.

B.1 PIC16F676 to PIC16F685

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F685
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	4096
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2
ECCP+	N	Y
Ultra Low-Power Wake-up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	31 kHz-8 MHz
Clock Switching	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

PIC16F631/677/685/687/689/690

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
<div>Device: PIC16F631⁽¹⁾, PIC16F677⁽¹⁾, PIC16F685⁽¹⁾, PIC16F687⁽¹⁾, PIC16F689⁽¹⁾, PIC16F690⁽¹⁾; VDD range 2.0V to 5.5V</div> <div>Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)</div> <div>Package: ML = QFN (Quad Flat, no lead) P = PDIP SO = SOIC SS = SSOP</div> <div>Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise)</div>			

Examples:

- a) PIC16F685 - I/ML 301 = Industrial temp., QFN package, QTP pattern #301.
- b) PIC16F689 - I/SO = Industrial temp., SOIC package.
- c) PIC16F690T - E/SS = Extended temp., SSOP package.

Note 1: T = in tape and reel SSOP, SOIC and QFN packages only.