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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f689-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic16f689-i-ml</a>

# PIC16F631/677/685/687/689/690

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# PIC16F631/677/685/687/689/690

**TABLE 1-4: PINOUT DESCRIPTION – PIC16F687/PIC16F689 (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RB6/SCK/SCL	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	SCK	ST	CMOS	SPI clock.
	SCL	ST	OD	I <sup>2</sup> C™ clock.
RB7/TX/CK	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	TX	—	CMOS	EUSART asynchronous output.
	CK	ST	CMOS	EUSART synchronous clock.
RC0/AN4/C2IN+	RC0	ST	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	C2IN+	AN	—	Comparator C2 positive input.
RC1/AN5/C12IN1-	RC1	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
RC2/AN6/C12IN2-	RC2	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
RC3/AN7/C12IN3-	RC3	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
RC4/C2OUT	RC4	ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
RC5	RC5	ST	CMOS	General purpose I/O.
RC6/AN8/ $\overline{SS}$	RC6	ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	$\overline{SS}$	ST	—	Slave Select input.
RC7/AN9/SDO	RC7	ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	SDO	—	CMOS	SPI data output.
Vss	Vss	Power	—	Ground reference.
VDD	VDD	Power	—	Positive supply.

**Legend:** AN = Analog input or output      CMOS=CMOS compatible input or output      OD= Open Drain  
TTL = TTL compatible input      ST= Schmitt Trigger input with CMOS levels  
HV = High Voltage      XTAL= Crystal

# PIC16F631/677/685/687/689/690

**FIGURE 2-7: PIC16F687/PIC16F689 SPECIAL FUNCTION REGISTERS**

File Address	File Address	File Address	File Address
Indirect addr. <sup>(1)</sup> 00h	Indirect addr. <sup>(1)</sup> 80h	Indirect addr. <sup>(1)</sup> 100h	Indirect addr. <sup>(1)</sup> 180h
TMR0 01h	OPTION_REG 81h	TMR0 101h	OPTION_REG 181h
PCL 02h	PCL 82h	PCL 102h	PCL 182h
STATUS 03h	STATUS 83h	STATUS 103h	STATUS 183h
FSR 04h	FSR 84h	FSR 104h	FSR 184h
PORTA 05h	TRISA 85h	PORTA 105h	TRISA 185h
PORTB 06h	TRISB 86h	PORTB 106h	TRISB 186h
PORTC 07h	TRISC 87h	PORTC 107h	TRISC 187h
08h	88h	108h	188h
09h	89h	109h	189h
PCLATH 0Ah	PCLATH 8Ah	PCLATH 10Ah	PCLATH 18Ah
INTCON 0Bh	INTCON 8Bh	INTCON 10Bh	INTCON 18Bh
PIR1 0Ch	PIE1 8Ch	EEDAT 10Ch	EECON1 18Ch
PIR2 0Dh	PIE2 8Dh	EEADR 10Dh	EECON2 <sup>(1)</sup> 18Dh
TMR1L 0Eh	PCON 8Eh	EEDATH <sup>(3)</sup> 10Eh	18Eh
TMR1H 0Fh	OSCCON 8Fh	EEADRH <sup>(3)</sup> 10Fh	18Fh
T1CON 10h	OSCTUNE 90h	110h	190h
11h	91h	111h	191h
12h	92h	112h	192h
SSPBUF 13h	SSPADD <sup>(2)</sup> 93h	113h	193h
SSPCON 14h	SSPSTAT 94h	114h	194h
15h	WPUA 95h	WPUB 115h	195h
16h	IOCA 96h	IOCB 116h	196h
17h	WDTCON 97h	117h	197h
RCSTA 18h	TXSTA 98h	VRCON 118h	198h
TXREG 19h	SPBRG 99h	CM1CON0 119h	199h
RCREG 1Ah	SPBRGH 9Ah	CM2CON0 11Ah	19Ah
1Bh	BAUDCTL 9Bh	CM2CON1 11Bh	19Bh
1Ch	9Ch	11Ch	19Ch
1Dh	9Dh	11Dh	19Dh
ADRESH 1Eh	ADRESL 9Eh	ANSEL 11Eh	SRCON 19Eh
ADCON0 1Fh	ADCON1 9Fh	ANSELH 11Fh	19Fh
20h	A0h	120h	1A0h
General Purpose Register 32 Bytes	General Purpose Register 80 Bytes (PIC16F689 only)		
48 Bytes (PIC16F689 only)			
accesses 70h-7Fh	accesses 70h-7Fh	170h	accesses 70h-7Fh
7Fh	FFh	17Fh	1FFh
Bank 0	Bank 1	Bank 2	Bank 3

☐ Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.  
**2:** Address 93h also accesses the SSP Mask (SSPMSK) register under certain conditions. See Registers 13-2 and 13-3 for more details.  
**3:** PIC16F689 only.

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## 4.0 I/O PORTS

There are as many as eighteen general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

### 4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write

operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

**Note:** The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

#### EXAMPLE 4-1: INITIALIZING PORTA

```
BCF    STATUS,RP0;Bank 0
BCF    STATUS,RP1;
CLRF   PORTA    ;Init PORTA
BSF    STATUS,RP1;Bank 2
CLRF   ANSEL    ;digital I/O
BSF    STATUS,RP0;Bank 1
BCF    STATUS,RP1;
MOVLW  0Ch      ;Set RA<3:2> as inputs
MOVWF  TRISA    ;and set RA<5:4,1:0>
                    ;as outputs
BCF    STATUS,RP0;Bank 0
```

#### REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

##### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>:** PORTA I/O Pin bit

1 = Port pin is > VIH

0 = Port pin is < VIL

#### REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

##### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit

1 = PORTA pin configured as an input (tri-stated)

0 = PORTA pin configured as an output

**Note 1:** TRISA<3> always reads '1'.

**Note 2:** TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

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**REGISTER 7-1: T2CON: TIMER 2 CONTROL REGISTER<sup>(1)</sup>**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits

0000 =1:1 Postscaler

0001 =1:2 Postscaler

0010 =1:3 Postscaler

0011 =1:4 Postscaler

0100 =1:5 Postscaler

0101 =1:6 Postscaler

0110 =1:7 Postscaler

0111 =1:8 Postscaler

1000 =1:9 Postscaler

1001 =1:10 Postscaler

1010 =1:11 Postscaler

1011 =1:12 Postscaler

1100 =1:13 Postscaler

1101 =1:14 Postscaler

1110 =1:15 Postscaler

1111 =1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 =Prescaler is 1

01 =Prescaler is 4

1x =Prescaler is 16

**Note 1:** PIC16F685/PIC16F690 only.

**TABLE 7-1: SUMMARY OF ASSOCIATED TIMER2<sup>(1)</sup> REGISTERS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
PR2	Timer2 Module Period Register								1111 1111	1111 1111
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for Timer2 module.

**Note 1:** PIC16F685/PIC16F690 only.

## 8.10.5 FIXED VOLTAGE REFERENCE

The Fixed Voltage Reference is independent of  $V_{DD}$ , with a nominal output voltage of 0.6V. This reference can be enabled by setting the VP6EN bit of the VRCON register to '1'. This reference is always enabled when the HFINTOSC oscillator is active.

## 8.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the Fixed Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See the electrical specifications section for the minimum delay requirement.

## 8.10.7 VOLTAGE REFERENCE SELECTION

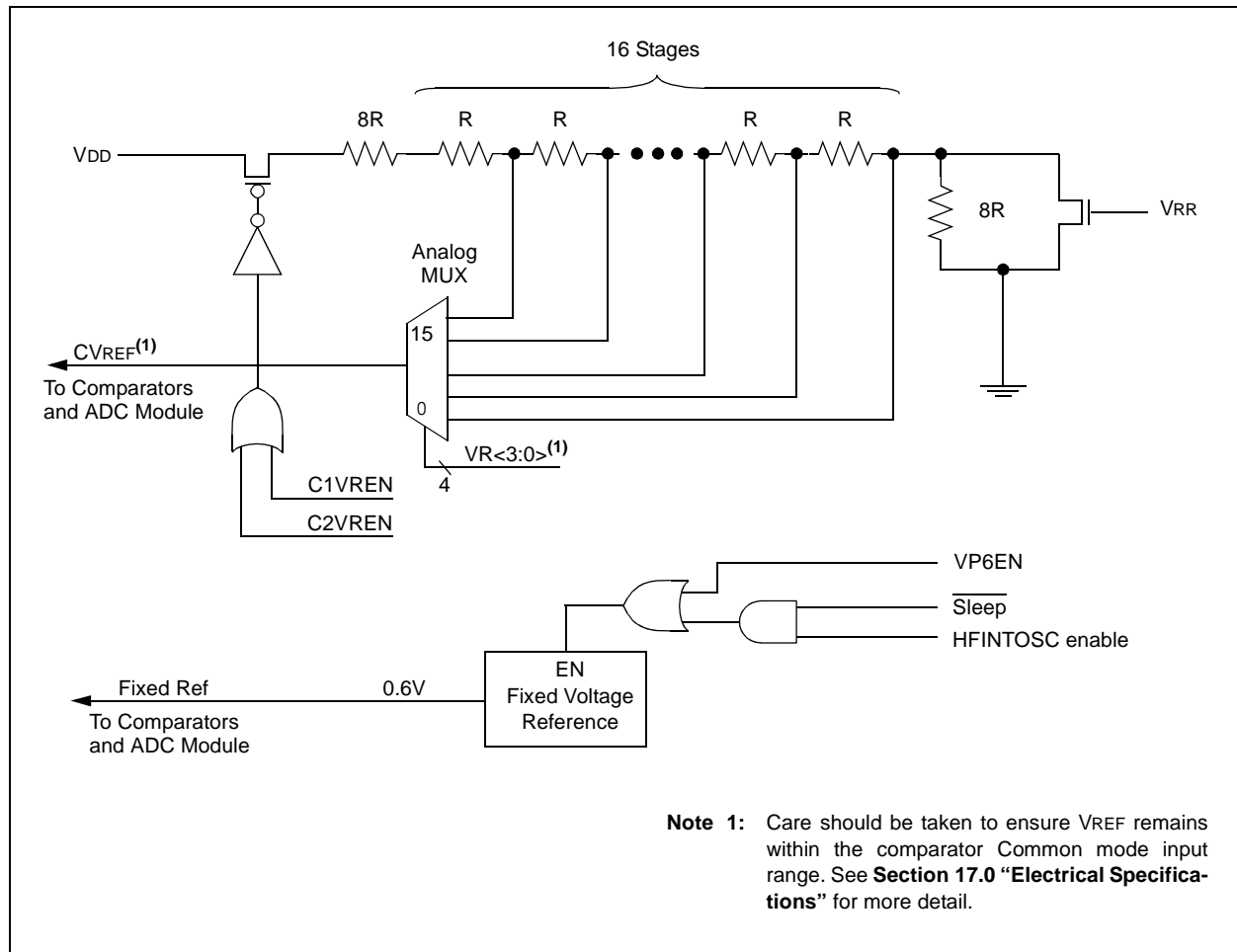
Multiplexers on the output of the Voltage Reference module enable selection of either the CVREF or Fixed Voltage Reference for use by the comparators.

Setting the C1VREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C1. Clearing the C1VREN bit selects the fixed voltage for use by C1.

Setting the C2VREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C2. Clearing the C2VREN bit selects the fixed voltage for use by C2.

When both the C1VREN and C2VREN bits are cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.

**FIGURE 8-8: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



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**TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ANSELH	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	uuuu ----
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for ADC module.



## 10.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

Data EEPROM memory is readable and writable and the Flash program memory (PIC16F685/PIC16F689/PIC16F690 only) is readable during normal operation (full VDD range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers (SFRs). There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDAT
- EEDATH (PIC16F685/PIC16F689/PIC16F690 only)
- EEADR
- EEADRH (PIC16F685/PIC16F689/PIC16F690 only)

When interfacing the data memory block, EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEDAT location being accessed. These devices, except for the PIC16F631, have 256 bytes of data EEPROM with an address range from 0h to 0FFh. The PIC16F631 has 128 bytes of data EEPROM with an address range from 0h to 07Fh.

When accessing the program memory block of the PIC16F685/PIC16F689/PIC16F690 devices, the EEDAT and EEDATH registers form a 2-byte word that holds the 14-bit data for read/write, and the EEADR and EEADRH registers form a 2-byte word that holds the 12-bit address of the EEPROM location being read. These devices (PIC16F685/PIC16F689/PIC16F690) have 4K words of program EEPROM with an address range from 0h to 0FFFh. The program memory allows one-word reads.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the data EEPROM memory and read the program memory. When code-protected, the device programmer can no longer access data or program memory.

## 10.1 EEADR and EEADRH Registers

The EEADR and EEADRH registers can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 4K words of program EEPROM.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADR register. When selecting a data address value, only the LSB of the address is written to the EEADR register.

### 10.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD (PIC16F685/PIC16F689/PIC16F690) determines if the access will be a program or data memory access. When clear, as it is when reset, any subsequent operations will operate on the data memory. When set, any subsequent operations will operate on the program memory. Program memory can only be read.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to data EEPROM. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location.

Interrupt flag bit EEIF of the PIR2 register is set when write is complete. It must be cleared in the software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

# PIC16F631/677/685/687/689/690

**TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
EECON1	EEPGD <sup>(1)</sup>	—	—	—	WRERR	WREN	WR	RD	x--- x000	0--- q000
EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
EEADR	EEADR7 <sup>(2)</sup>	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
EEADRH <sup>(1)</sup>	—	—	—	—	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---- 0000	---- 0000
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEDATH <sup>(1)</sup>	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000	--00 0000
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 0000	0000 0000
PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----	0000 ----
PIR2	OSFIF	C2IF	C1IF	EEIF	—	—	—	—	0000 ----	0000 ----

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition.  
Shaded cells are not used by data EEPROM module.

**Note** 1: PIC16F685/PIC16F689/PIC16F690 only.  
2: PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

## 11.4.2 FULL-BRIDGE MODE

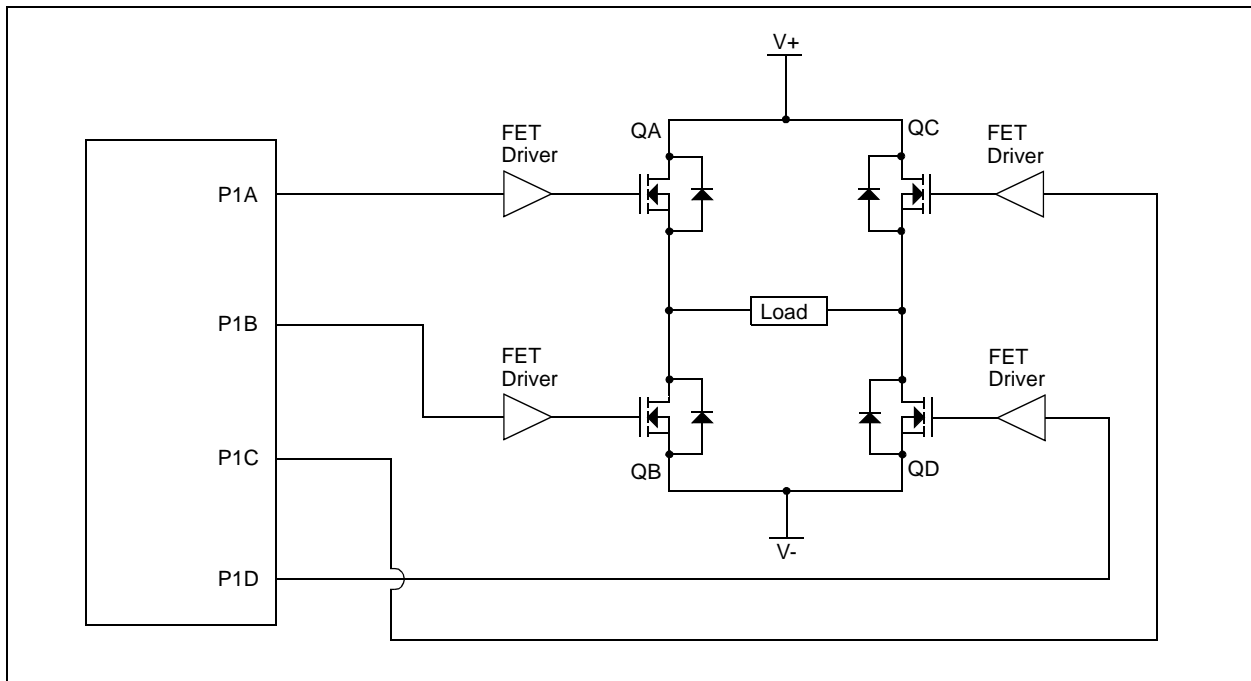
In Full-Bridge mode, all four pins are used as outputs. An example of Full-Bridge application is shown in Figure 11-10.

In the Forward mode, pin CCP1/P1A is driven to its active state, pin P1D is modulated, while P1B and P1C will be driven to their inactive state as shown in Figure 11-11.

In the Reverse mode, P1C is driven to its active state, pin P1B is modulated, while P1A and P1D will be driven to their inactive state as shown Figure 11-11.

P1A, P1B, P1C and P1D outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the P1A, P1B, P1C and P1D pins as outputs.

**FIGURE 11-10: EXAMPLE OF FULL-BRIDGE APPLICATION**



## 12.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

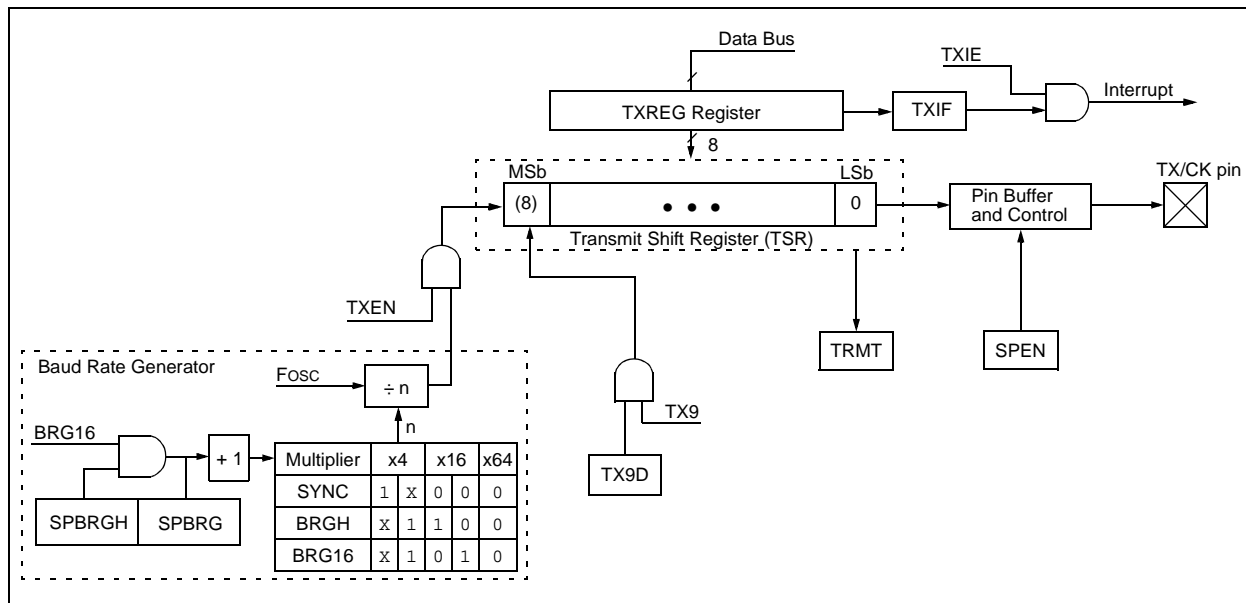
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 12-1 and Figure 12-2.

**FIGURE 12-1: EUSART TRANSMIT BLOCK DIAGRAM**



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**TABLE 12-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
RCREG	EUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	0000 0000
TRISB	TRISB7	TRISB6	TRISB5	TRISB4					1111 ----	1111 ----
TXREG	EUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	SENDER	BRGH	TRMT	TX9D	0000 0010	0000 0010

**Legend:** x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

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**TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODES**

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz			Fosc = 8.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	1221	1.73	255	1200	0.00	239	1200	0.00	143	1202	0.16	103
2400	2404	0.16	129	2400	0.00	119	2400	0.00	71	2404	0.16	51
9600	9470	-1.36	32	9600	0.00	29	9600	0.00	17	9615	0.16	12
10417	10417	0.00	29	10286	-1.26	27	10165	-2.42	16	10417	0.00	11
19.2k	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8	—	—	—
57.6k	—	—	—	57.60k	0.00	7	57.60k	0.00	2	—	—	—
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300	0.16	207	300	0.00	191	300	0.16	103	300	0.16	51
1200	1202	0.16	51	1200	0.00	47	1202	0.16	25	1202	0.16	12
2400	2404	0.16	25	2400	0.00	23	2404	0.16	12	—	—	—
9600	—	—	—	9600	0.00	5	—	—	—	—	—	—
10417	10417	0.00	5	—	—	—	10417	0.00	2	—	—	—
19.2k	—	—	—	19.20k	0.00	2	—	—	—	—	—	—
57.6k	—	—	—	57.60k	0.00	0	—	—	—	—	—	—
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz			Fosc = 8.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	—	—	—	—	—	—	—	—	—
2400	—	—	—	—	—	—	—	—	—	2404	0.16	207
9600	9615	0.16	129	9600	0.00	119	9600	0.00	71	9615	0.16	51
10417	10417	0.00	119	10378	-0.37	110	10473	0.53	65	10417	0.00	47
19.2k	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35	19231	0.16	25
57.6k	56.82k	-1.36	21	57.60k	0.00	19	57.60k	0.00	11	55556	-3.55	8
115.2k	113.64k	-1.36	10	115.2k	0.00	9	115.2k	0.00	5	—	—	—

## 14.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit (PCON<4>) enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 14-2 for the Configuration Word definition.

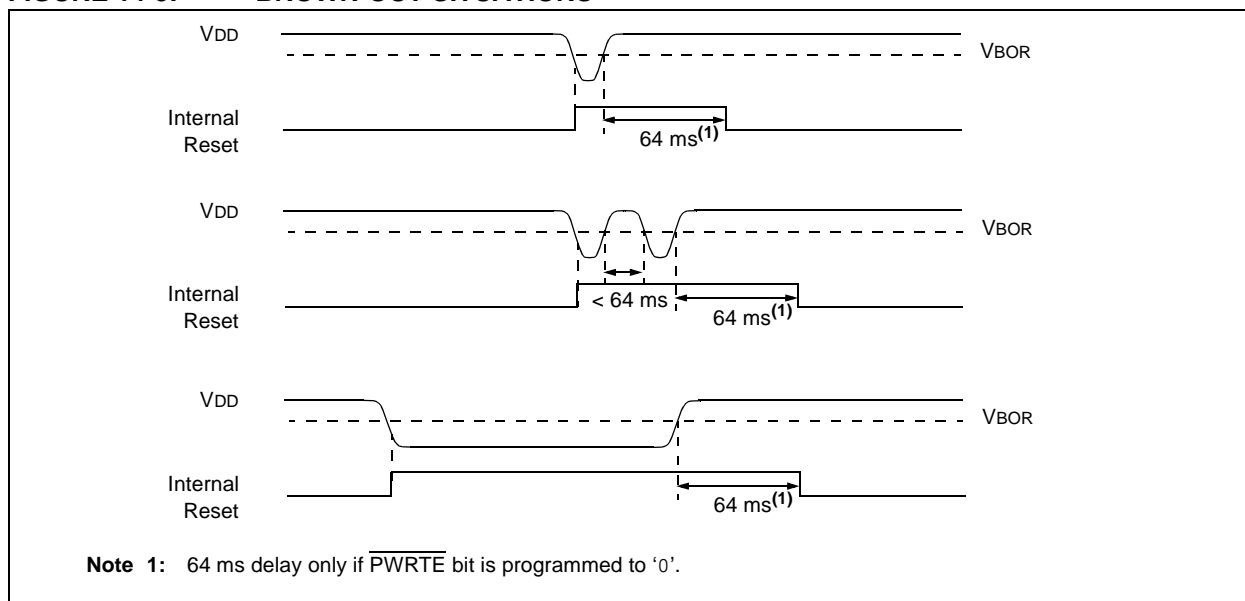
If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 17.0 “Electrical Specifications”**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 14-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

**Note:** The Power-up Timer is enabled by the  $\overline{\text{PWRTE}}$  bit in the Configuration Word register.

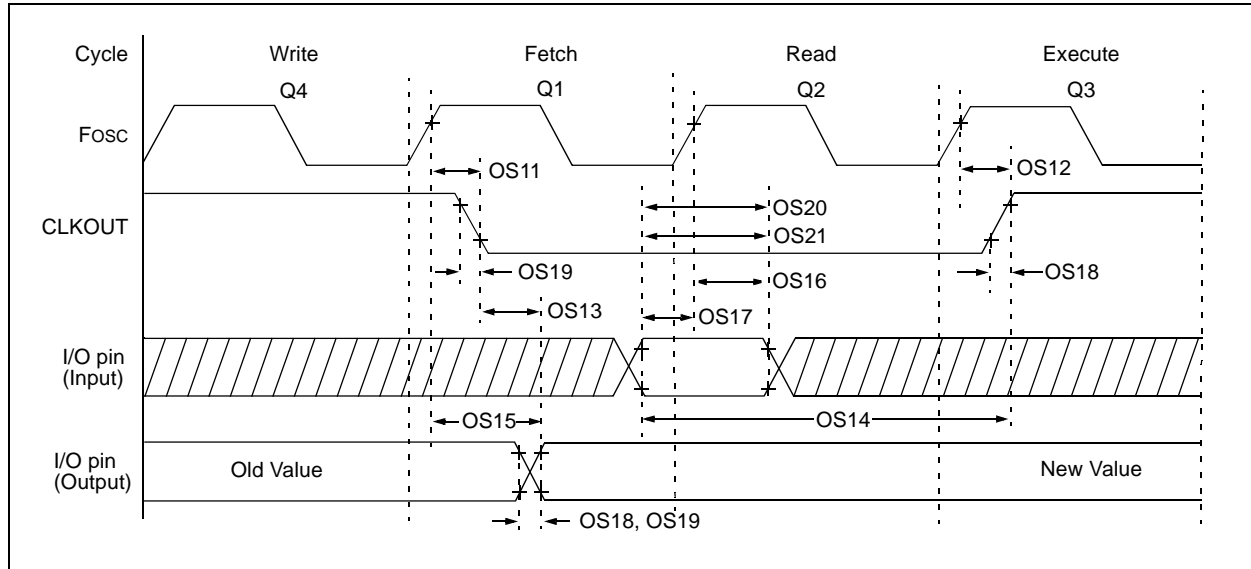
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

**FIGURE 14-3: BROWN-OUT SITUATIONS**



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**FIGURE 17-5: CLKOUT AND I/O TIMING**



**TABLE 17-3: CLKOUT AND I/O TIMING PARAMETERS**

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ <sup>(1)</sup>	—	—	70	ns	V <sub>DD</sub> = 5.0V
OS12	TosH2ckH	Fosc↑ to CLKOUT↑ <sup>(1)</sup>	—	—	72	ns	V <sub>DD</sub> = 5.0V
OS13	TckL2ioV	CLKOUT↓ to port out valid <sup>(1)</sup>	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT↑ <sup>(1)</sup>	Tosc + 200 ns	—	—	ns	
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to port out valid	—	50	70*	ns	V <sub>DD</sub> = 5.0V
OS16	TosH2ioI	Fosc↑ (Q2 cycle) to port input invalid (I/O in hold time)	50	—	—	ns	V <sub>DD</sub> = 5.0V
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time <sup>(2)</sup>	—	15 40	72 32	ns	V <sub>DD</sub> = 2.0V V <sub>DD</sub> = 5.0V
OS19	TioF	Port output fall time <sup>(2)</sup>	—	28 15	55 30	ns	V <sub>DD</sub> = 2.0V V <sub>DD</sub> = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TRAP	PORTA interrupt-on-change new input level time	T <sub>CY</sub>	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated.

**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x T<sub>osc</sub>.

**2:** Includes OSC2 in CLKOUT mode.



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**TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 5	— —	— —	$\mu\text{s}$ $\mu\text{s}$	$V_{DD} = 5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 5\text{V}$
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	$V_{DD} = 5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 5\text{V}$
32	TOST	Oscillation Start-up Timer Period <sup>(1, 2)</sup>	—	1024	—	TOSC	(Note 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	$\mu\text{s}$	
35	VBOR	Brown-out Reset Voltage	2.0	—	2.2	V	(Note 4)
36*	VHYS	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	$\mu\text{s}$	$V_{DD} \leq V_{BOR}$

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (T<sub>CY</sub>) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to the OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

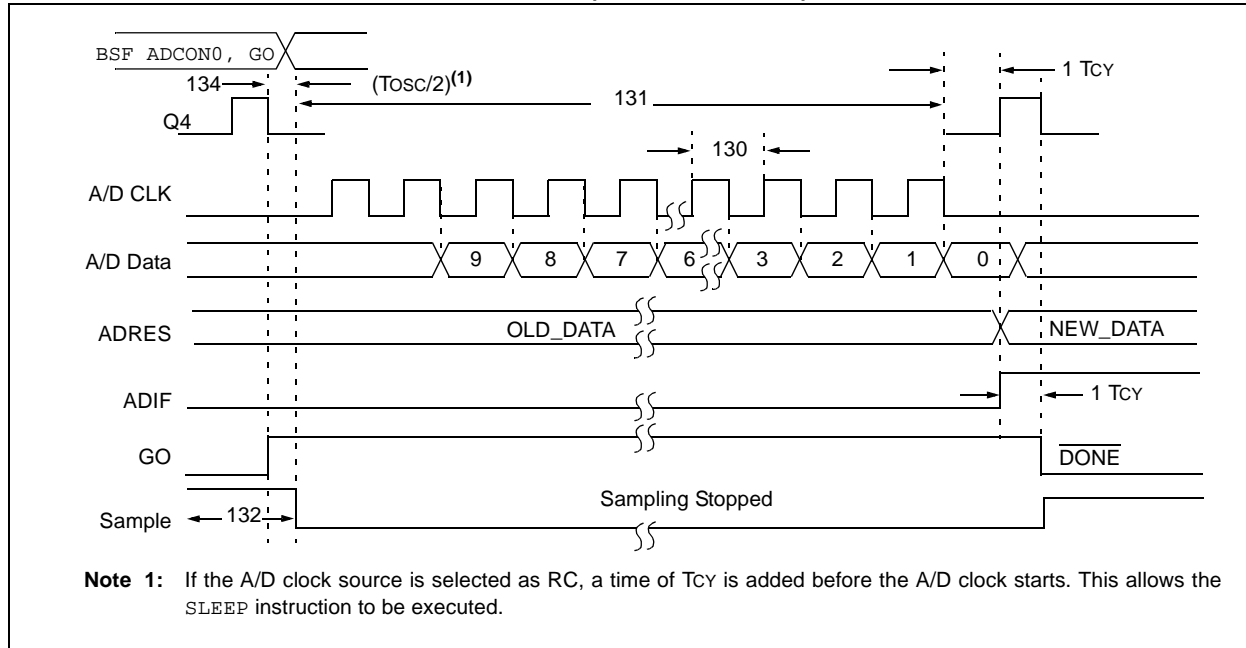
**2:** By design.

**3:** Period of the slower clock.

**4:** To ensure these voltage tolerances, V<sub>DD</sub> and V<sub>SS</sub> must be capacitively decoupled as close to the device as possible. 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  values in parallel are recommended.

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**FIGURE 17-18: A/D CONVERSION TIMING (NORMAL MODE)**



**TABLE 17-16: A/D CONVERSION REQUIREMENTS**

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
130*	TAD	A/D Clock Period	1.5	—	—	$\mu\text{s}$	TOSC-based, $V_{REF} \geq 2.5\text{V}$
		A/D Internal RC Oscillator Period	3.0*	—	—	$\mu\text{s}$	TOSC-based, $V_{REF}$ full range
			3.0*	6.0	9.0*	$\mu\text{s}$	$\text{ADCS}\langle 1:0 \rangle = 11$ (RC mode)
			2.0*	4.0	6.0*	$\mu\text{s}$	At $V_{DD} = 2.5\text{V}$
							At $V_{DD} = 5.0\text{V}$
131	TCNV	Conversion Time (not including Acquisition Time) <sup>(1)</sup>	—	11	—	TAD	Set GO bit to new data in A/D Result register
132*	TACQ	Acquisition Time	(2)	11.5	—	$\mu\text{s}$	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSB (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
			5*	—	—	$\mu\text{s}$	
134	TGO	Q4 to A/D Clock Start	—	$T_{OSC}/2$	—	—	If the A/D clock source is selected as RC, a time of $T_{CY}$ is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

\* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRESH and ADRESL registers may be read on the following  $T_{CY}$  cycle.

**2:** See Table 9-1 for minimum conditions.

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FIGURE 18-12: MAXIMUM  $I_{DD}$  vs.  $F_{osc}$  OVER  $V_{DD}$  (HFINTOSC MODE)

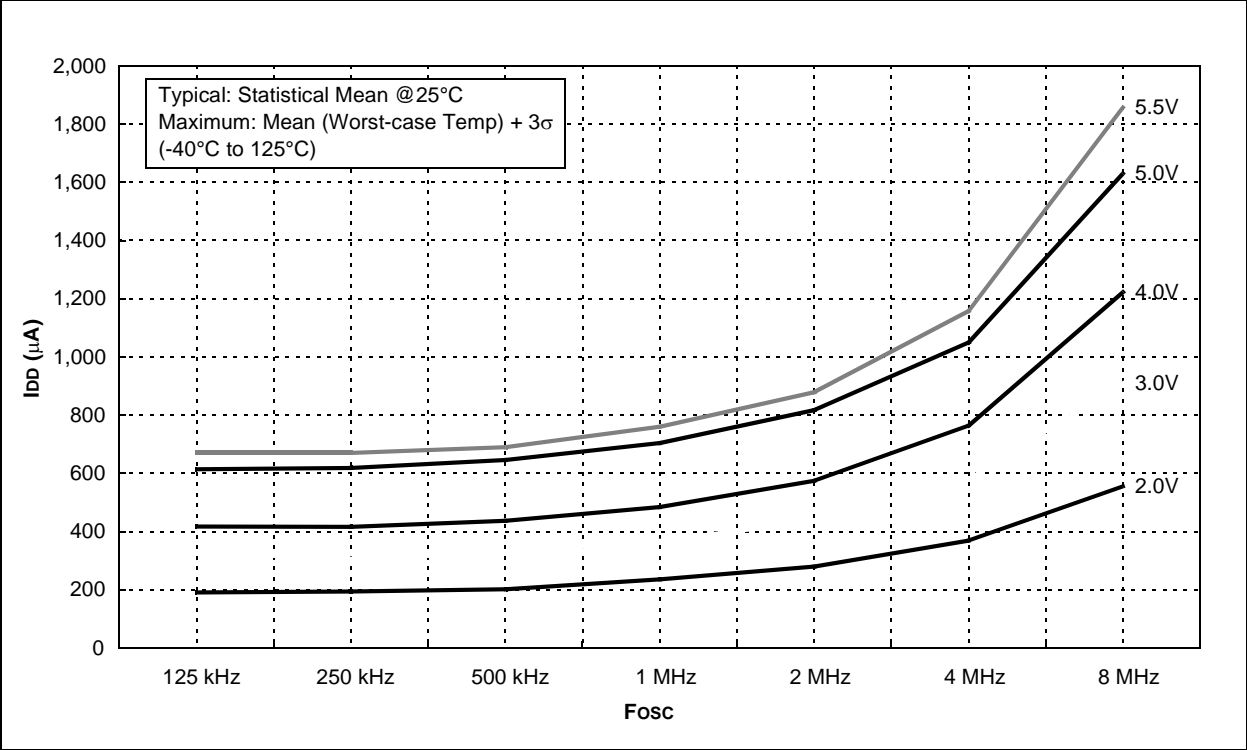
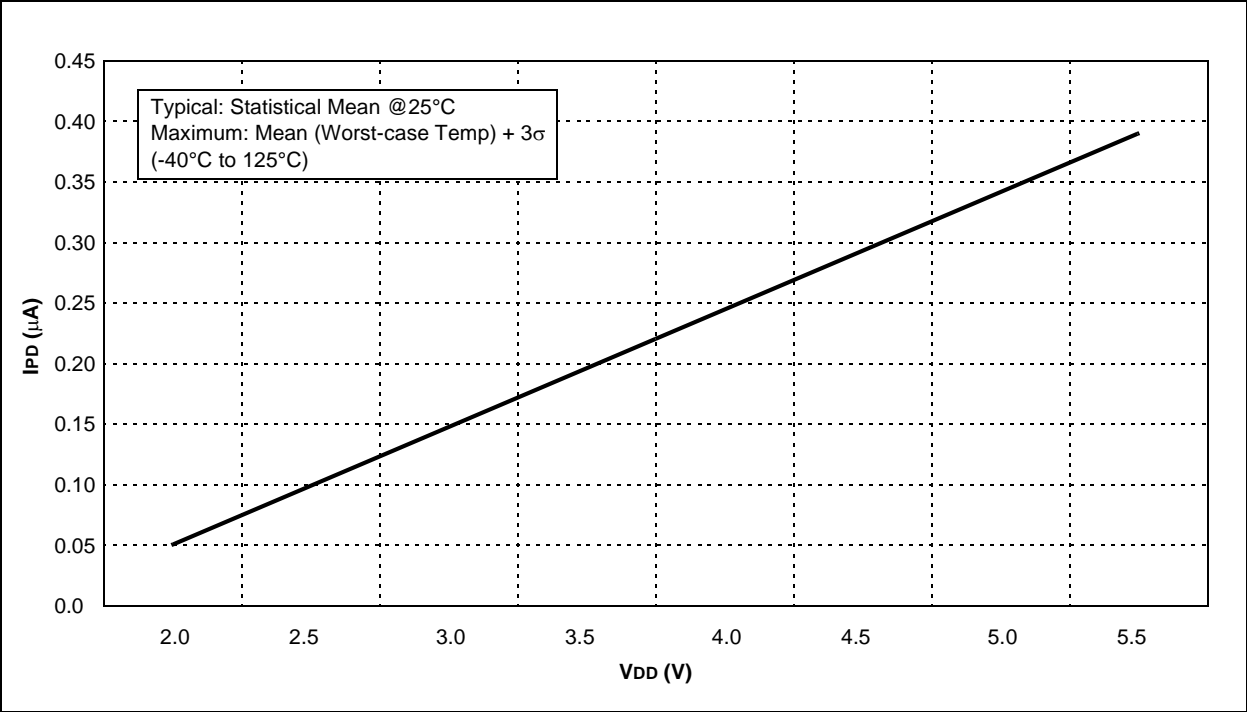


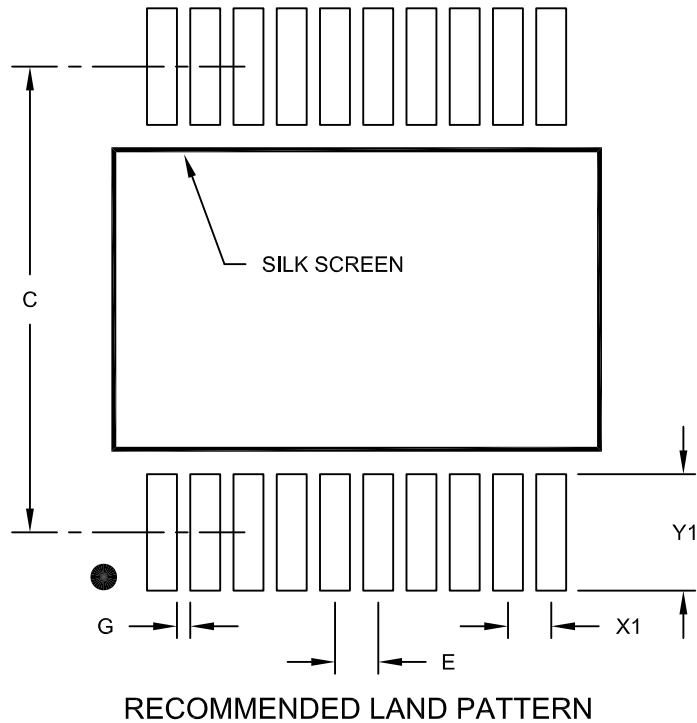
FIGURE 18-13: TYPICAL  $I_{PD}$  vs.  $V_{DD}$  (SLEEP MODE, ALL PERIPHERALS DISABLED)



# PIC16F631/677/685/687/689/690

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

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ISBN: 978-1-63277-235-0

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