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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 18 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 20-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f689-i-so |

## 2.0 MEMORY ORGANIZATION

### 2.1 Program Memory Organization

The PIC16F631/677/685/687/689/690 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) is physically implemented for the PIC16F631, the first 2K x 14 (0000h-07FFh) for the PIC16F677/PIC16F687, and the first 4K x 14 (0000h-0FFFh) for the PIC16F685/PIC16F689/PIC16F690. Accessing a location above these boundaries will cause a wrap-around. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 2-1 through 2-3).

**FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F631**

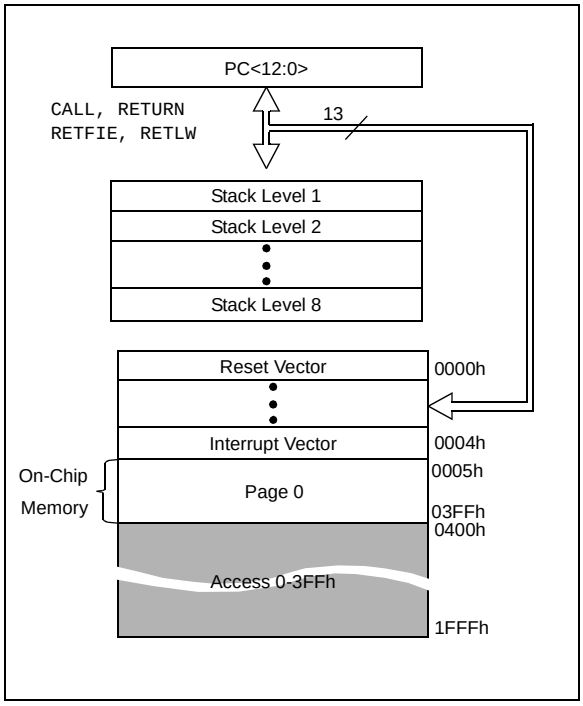



**FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F685/689/690**

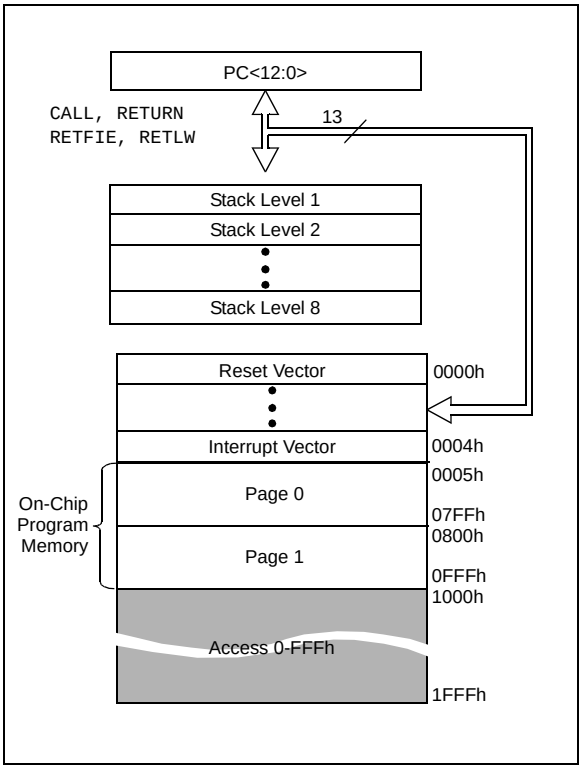



**FIGURE 2-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F677/PIC16F687**

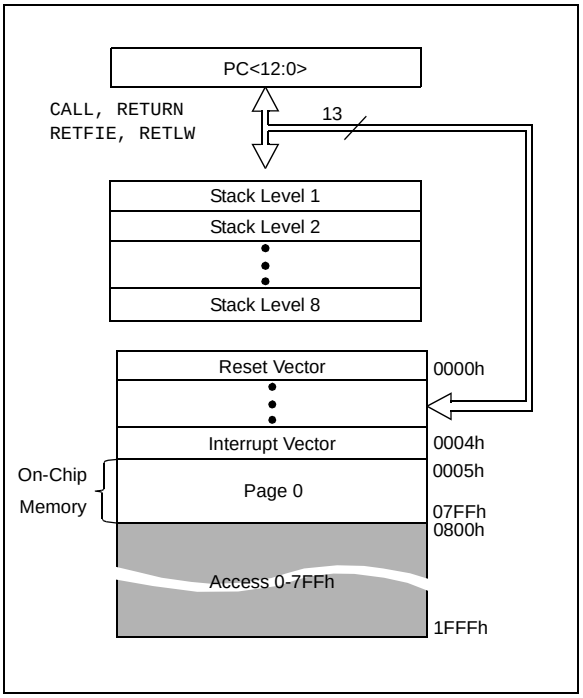


**FIGURE 2-4: PIC16F631 SPECIAL FUNCTION REGISTERS**

| Bank 0 | File Address | Bank 1 | File Address | Bank 2 | File Address | Bank 3 | File Address |
|---|---|---|---|---|---|---|---|
| Indirect addr. (1) | 00h | Indirect addr. (1) | 80h | Indirect addr. (1) | 100h | Indirect addr. (1) | 180h |
| TMR0 | 01h | OPTION_REG | 81h | TMR0 | 101h | OPTION_REG | 181h |
| PCL | 02h | PCL | 82h | PCL | 102h | PCL | 182h |
| STATUS | 03h | STATUS | 83h | STATUS | 103h | STATUS | 183h |
| FSR | 04h | FSR | 84h | FSR | 104h | FSR | 184h |
| PORTA | 05h | TRISA | 85h | PORTA | 105h | TRISA | 185h |
| PORTB | 06h | TRISB | 86h | PORTB | 106h | TRISB | 186h |
| PORTC | 07h | TRISC | 87h | PORTC | 107h | TRISC | 187h |
| | 08h | | 88h | | 108h | | 188h |
| | 09h | | 89h | | 109h | | 189h |
| PCLATH | 0Ah | PCLATH | 8Ah | PCLATH | 10Ah | PCLATH | 18Ah |
| INTCON | 0Bh | INTCON | 8Bh | INTCON | 10Bh | INTCON | 18Bh |
| PIR1 | 0Ch | PIE1 | 8Ch | EEDAT | 10Ch | EECON1 | 18Ch |
| PIR2 | 0Dh | PIE2 | 8Dh | EEADR | 10Dh | EECON2(1) | 18Dh |
| TMR1L | 0Eh | PCON | 8Eh | | 10Eh | | 18Eh |
| TMR1H | 0Fh | OSCCON | 8Fh | | 10Fh | | 18Fh |
| T1CON | 10h | OSCTUNE | 90h | | 110h | | 190h |
| | 11h | | 91h | | 111h | | 191h |
| | 12h | | 92h | | 112h | | 192h |
| | 13h | | 93h | | 113h | | 193h |
| | 14h | | 94h | | 114h | | 194h |
| | 15h | WPUA | 95h | WPUB | 115h | | 195h |
| | 16h | IOCA | 96h | IOCB | 116h | | 196h |
| | 17h | WDTCON | 97h | | 117h | | 197h |
| | 18h | | 98h | VRCON | 118h | | 198h |
| | 19h | | 99h | CM1CON0 | 119h | | 199h |
| | 1Ah | | 9Ah | CM2CON0 | 11Ah | | 19Ah |
| | 1Bh | | 9Bh | CM2CON1 | 11Bh | | 19Bh |
| | 1Ch | | 9Ch | | 11Ch | | 19Ch |
| | 1Dh | | 9Dh | | 11Dh | | 19Dh |
| | 1Eh | | 9Eh | ANSEL | 11Eh | SRCON | 19Eh |
| | 1Fh | | 9Fh | | 11Fh | | 19Fh |
| | 20h – 3Fh | | A0h | | 120h | | 1A0h |
| General Purpose Registers 64 Bytes | 40h – 6Fh | | EFh | | 16Fh | | 1EFh |
| | 70h – 7Fh | accesses 70h-7Fh | F0h – FFh | accesses 70h-7Fh | 170h – 17Fh | accesses 70h-7Fh | 1F0h – 1FFh |

Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

## 4.2 Additional Pin Functions

Every PORTA pin on this device family has an interrupt-on-change option and a weak pull-up option. RA0 also has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

### 4.2.1 ANSEL AND ANSELH REGISTERS

The ANSEL and ANSELH registers are used to disable the input buffers of I/O pins, which allow analog voltages to be applied to those pins without causing excessive current. Setting the ANSx bit of a corresponding pin will cause all digital reads of that pin to return '0' and also permit analog functions of that pin to operate correctly.

The state of the ANSx bit has no effect on the digital output function of its corresponding pin. A pin with the TRISx bit clear and ANSx bit set will operate as a digital output, together with the analog input function of that pin. Pins with the ANSx bit set always read '0', which can cause unexpected behavior when executing read or write operations on the port due to the read-modify-write sequence of all such operations.

### 4.2.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the RABPU bit of the OPTION register. A weak pull-up is automatically enabled for RA3 when configured as MCLR and disabled when RA3 is an I/O. There is no software control of the MCLR pull-up.

### 4.2.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 4-6. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (RABIF) in the INTCON register (Register 2-6).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTA. This will end the mismatch condition, then,
b) Clear the flag bit RABIF.

A mismatch condition will continue to set flag bit RABIF. Reading PORTA will end the mismatch condition and allow flag bit RABIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOR Reset. After these Resets, the RABIF flag will continue to be set if a mismatch is present.

| | |
|---|---|
| **Note:** | If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RABIF interrupt flag may not get set. |

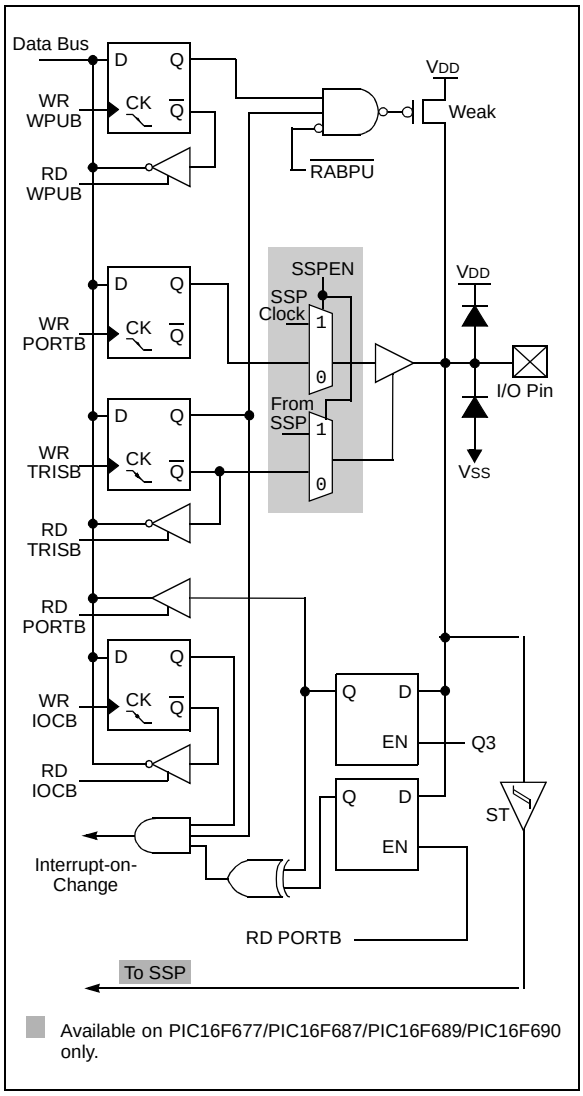
#### 4.4.3.3 RB6/SCK/SCL

Figure 4-9 shows the diagram for this pin. The RB6/SCK/SCL(1) pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI clock
- an $I^2C$™ clock

| | |
|---|---|
| **Note 1:** | SCK and SCL are available on PIC16F677/PIC16F687/PIC16F689/PIC16F690 only. |

**FIGURE 4-9: BLOCK DIAGRAM OF RB6**



### 4.5.7 RC6/AN8/$\overline{SS}$

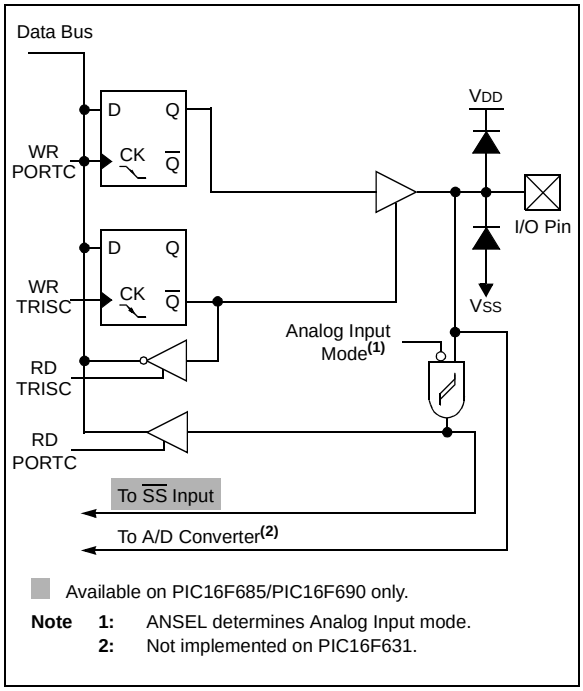
The RC6/AN8/$\overline{SS}$**(1,2)** is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- a slave select input

**Note 1:** $\overline{SS}$ is available on PIC16F687/PIC16F689/PIC16F690 only.

**2:** AN8 is not implemented on PIC16F631.

**FIGURE 4-15: BLOCK DIAGRAM OF RC6**




### 4.5.8 RC7/AN9/SDO

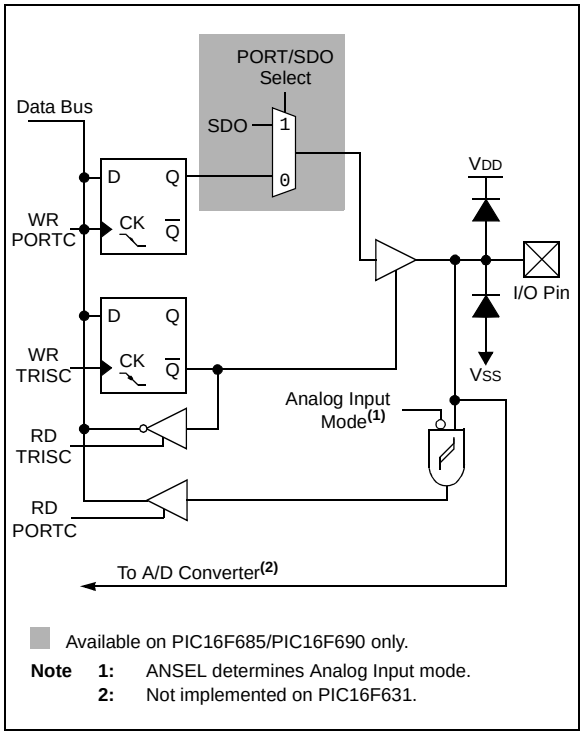
The RC7/AN9/SDO**(1,2)** is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC (except PIC16F631)
- a serial data output

**Note 1:** SDO is available on PIC16F687/PIC16F689/PIC16F690 only.

**2:** AN9 is not implemented on PIC16F631.

**FIGURE 4-16: BLOCK DIAGRAM OF RC7**



## 7.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

### 7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (FOSC/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

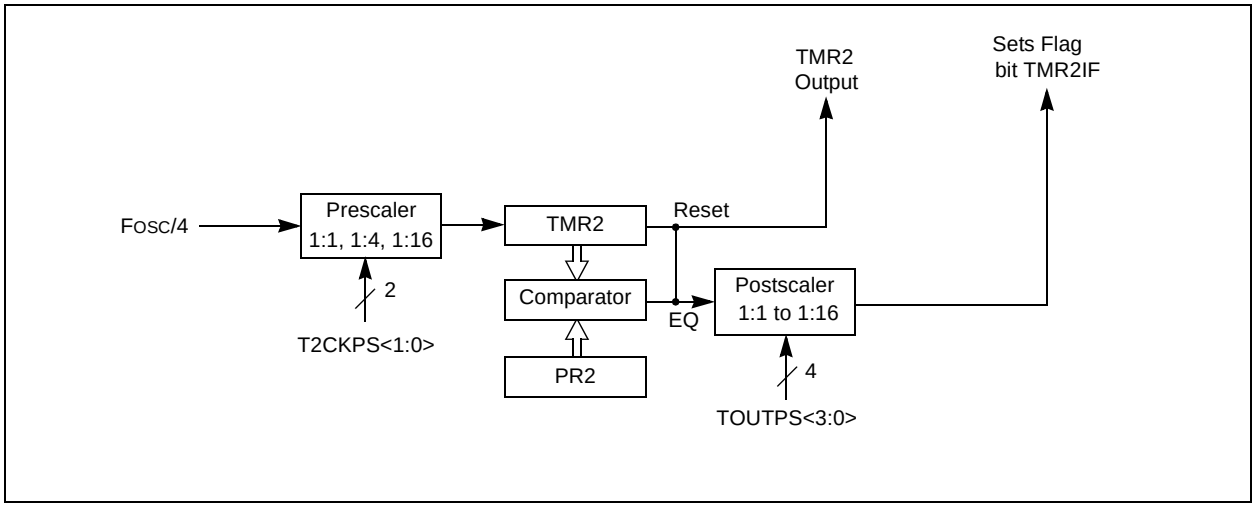
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset or Brown-out Reset).

**Note:** TMR2 is not cleared when T2CON is written.

**FIGURE 7-1: TIMER2 BLOCK DIAGRAM**



## 8.9 Comparator SR Latch

The SR Latch module provides additional control of the comparator outputs. The module consists of a single SR latch and output multiplexers. The SR latch can be set, reset or toggled by the comparator outputs. The SR latch may also be set or reset, independent of comparator output, by control bits in the SRCON control register. The SR latch output multiplexers select whether the latch outputs or the comparator outputs are directed to the I/O port logic for eventual output to a pin.

### 8.9.1 LATCH OPERATION

The latch is a Set-Reset latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. Each latch input is connected to a comparator output and a software controlled pulse generator. The latch can be set by C1OUT or the PULSS bit of the SRCON register. The latch can be reset by C2OUT or the PULSR bit of the SRCON register. The latch is reset-dominant, therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the PULSS and PULSR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch set or reset operation.

### 8.9.2 LATCH OUTPUT

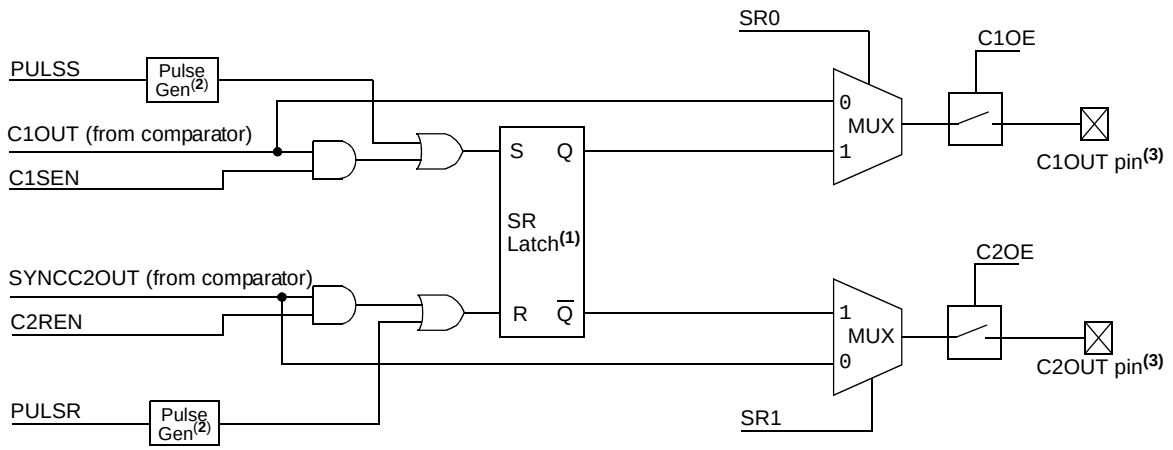
The SR<1:0> bits of the SRCON register control the latch output multiplexers and determine four possible output configurations. In these four configurations, the CxOUT I/O port logic is connected to:

- C1OUT and C2OUT
- C1OUT and SR latch $\overline{Q}$
- C2OUT and SR latch Q
- SR latch Q and $\overline{Q}$

After any Reset, the default output configuration is the unlatched C1OUT and C2OUT mode. This maintains compatibility with devices that do not have the SR latch feature.

The applicable TRIS bits of the corresponding ports must be cleared to enable the port pin output drivers. Additionally, the CxOE comparator output enable bits of the CMxCON0 registers must be set in order to make the comparator or latch outputs available on the output pins. The latch configuration enable states are completely independent of the enable states for the comparators.

**FIGURE 8-7: SR LATCH SIMPLIFIED BLOCK DIAGRAM**




**Note 1:** If R = 1 and S = 1 simultaneously, Q = 0, $\overline{Q}$ = 1
**2:** Pulse generator causes a 1/2 Q-state (1 Tosc) pulse width.
**3:** Output shown for reference only. See I/O port pin block diagram for more detail.

**REGISTER 8-5: VRCON: VOLTAGE REFERENCE CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| C1VREN | C2VREN | VRR | VP6EN | VR3 | VR2 | VR1 | VR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **C1VREN:** Comparator 1 Voltage Reference Enable bit
1 = $CV_{REF}$ circuit powered on and routed to $C1V_{REF}$ input of Comparator C1
0 = 0.6 Volt constant reference routed to $C1V_{REF}$ input of Comparator C1

bit 6 **C2VREN:** Comparator 2 Voltage Reference Enable bit
1 = $CV_{REF}$ circuit powered on and routed to $C2V_{REF}$ input of Comparator C2
0 = 0.6 Volt constant reference routed to $C2V_{REF}$ input of Comparator C2

bit 5 **VRR:** $CV_{REF}$ Range Selection bit
1 = Low range
0 = High range

bit 4 **VP6EN:** 0.6V Reference Enable bit
1 = Enabled
0 = Disabled

bit 3-0 **VR<3:0>:** Comparator Voltage Reference $CV_{REF}$ Value Selection bits ($0 \leq$ VR<3:0> $\leq 15$)
When VRR = 1: $CV_{REF} = (VR<3:0>/24) * V_{DD}$
When VRR = 0: $CV_{REF} = V_{DD}/4 + (VR<3:0>/32) * V_{DD}$

**TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ANSEL | ANS7 | ANS6 | ANS5 | ANS4 | ANS3 | ANS2 | ANS1 | ANS0 | 1111 1111 | 1111 1111 |
| CM1CON0 | C1ON | C1OUT | C1OE | C1POL | — | C1R | C1CH1 | C1CH0 | 0000 -000 | 0000 0000 |
| CM2CON0 | C2ON | C2OUT | C2OE | C2POL | — | C2R | C2CH1 | C2CH0 | 0000 -000 | 0000 -000 |
| CM2CON1 | MC1OUT | MC2OUT | — | — | — | — | T1GSS | C2SYNC | 00-- --10 | 00-- --10 |
| INTCON | GIE | PEIE | T0IE | INTE | RABIE | T0IF | INTF | RABIF | 0000 000x | 0000 000x |
| PIE2 | OSFIE | C2IE | C1IE | EEIE | — | — | — | — | 0000 ---- | 0000 ---- |
| PIR2 | OSFIF | C2IF | C1IF | EEIF | — | — | — | — | 0000---- | 0000---- |
| PORTA | — | — | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --xx xxxx | --uu uuuu |
| PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | uuuu uuuu |
| SRCON | SR1 | SR0 | C1SEN | C2REN | PULSS | PULSR | — | — | 0000 00-- | 0000 00-- |
| TRISA | — | — | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | --11 1111 | --11 1111 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 1111 1111 | 1111 1111 |
| VRCON | C1VREN | C2VREN | VRR | VP6EN | VR3 | VR2 | VR1 | VR0 | 0000 0000 | 0000 0000 |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used for comparator.

**EXAMPLE 9-1: A/D CONVERSION**

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSELADCON1;
MOVLWB'01110000';ADC Frc clock
MOVWFADCON1;
BANKSELTRISA;
BSF TRISA,0;Set RA0 to input
BANKSELANSEL;
BSF ANSEL,0;Set RA0 to analog
BANKSELADCON0;
MOVLWB'10000001';Right justify,
MOVWFADCON0; Vdd Vref, AN0, On
CALLSampleTime;Acquisiton delay
BSF ADCON0,GO;Start conversion
BTFSCADCON0,GO;Is conversion done?
GOTO$-1 ;No, test again
BANKSELADRESH;
MOVFADRESH,W;Read upper 2 bits
MOVWFRESULTHI;store in GPR space
BANKSELADRESL;
MOVFADRESL,W;Read lower 8 bits
MOVWFRESULTLO;Store in GPR space
```

### 9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

**TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| EECON1 | EEPGD(1) | — | — | — | WRERR | WREN | WR | RD | x--- x000 | 0--- q000 |
| EECON2 | EEPROM Control Register 2 (not a physical register) | | | | | | | | ---- ---- | ---- ---- |
| EEADR | EEADR7(2) | EEADR6 | EEADR5 | EEADR4 | EEADR3 | EEADR2 | EEADR1 | EEADR0 | 0000 0000 | 0000 0000 |
| EEADRH(1) | — | — | — | — | EEADRH3 | EEADRH2 | EEADRH1 | EEADRH0 | ---- 0000 | ---- 0000 |
| EEDAT | EEDAT7 | EEDAT6 | EEDAT5 | EEDAT4 | EEDAT3 | EEDAT2 | EEDAT1 | EEDAT0 | 0000 0000 | 0000 0000 |
| EEDATH(1) | — | — | EEDATH5 | EEDATH4 | EEDATH3 | EEDATH2 | EEDATH1 | EEDATH0 | --00 0000 | --00 0000 |
| INTCON | GIE | PEIE | T0IE | INTE | RABIE | T0IF | INTF | RABIF | 0000 0000 | 0000 0000 |
| PIE2 | OSFIE | C2IE | C1IE | EEIE | — | — | — | — | 0000 ---- | 0000 ---- |
| PIR2 | OSFIF | C2IF | C1IF | EEIF | — | — | — | — | 0000 ---- | 0000 ---- |

**Legend:** x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by data EEPROM module.

**Note 1:** PIC16F685/PIC16F689/PIC16F690 only.

**2:** PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.

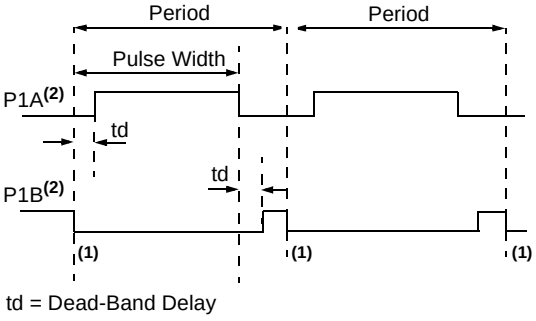
### 11.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 11-6). This mode can be used for Half-Bridge applications, as shown in Figure 11-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 11.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

**FIGURE 11-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT**



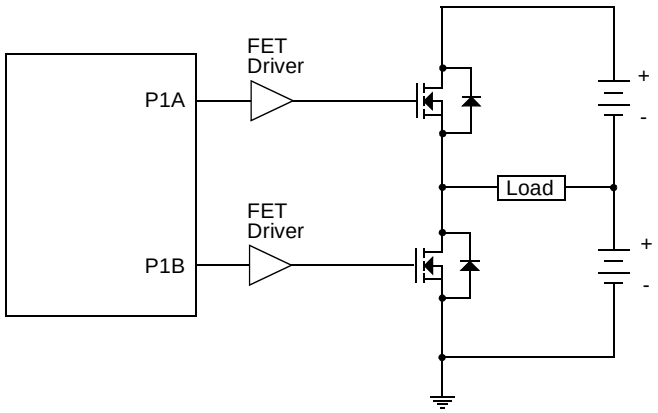

td = Dead-Band Delay

**Note 1:** At this time, the TMR2 register is equal to the PR2 register.

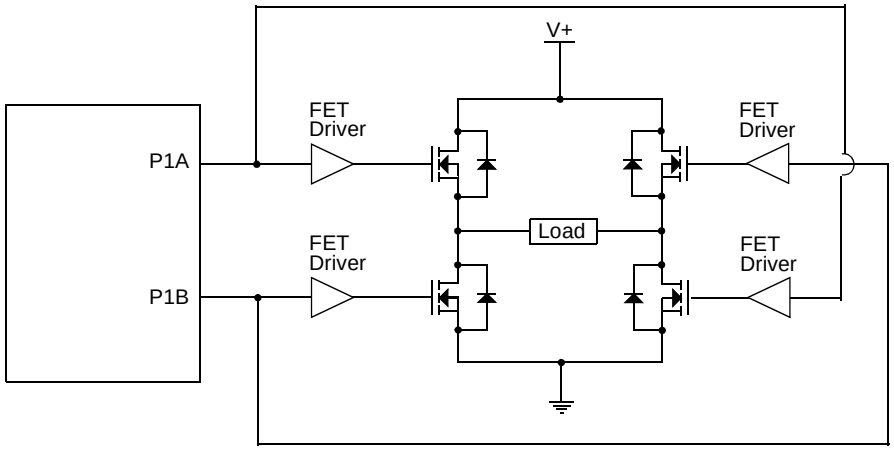
**2:** Output signals are shown as active-high.

**FIGURE 11-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS**

**Standard Half-Bridge Circuit ("Push-Pull")**




**Half-Bridge Output Driving a Full-Bridge Circuit**

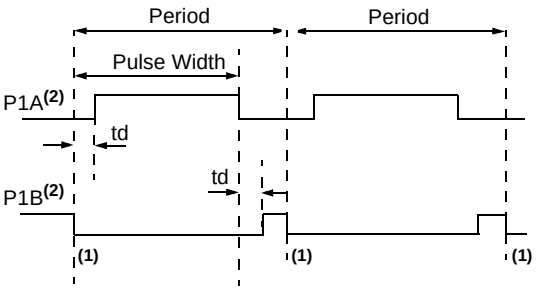


### 11.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In Half-Bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 11-8 for illustration. The lower seven bits of the associated PWM1CON register (Register 11-3) sets the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

**FIGURE 11-17: EXAMPLE OF HALF-BRIDGE PWM OUTPUT**

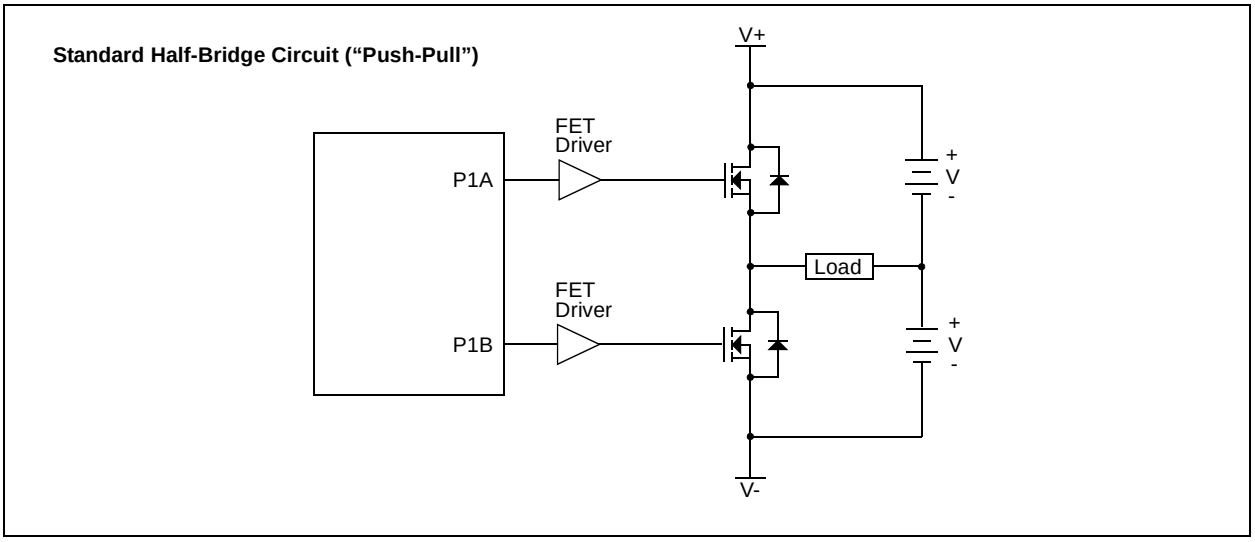



td = Dead-Band Delay

**Note 1:** At this time, the TMR2 register is equal to the PR2 register.

**2:** Output signals are shown as active-high.

**FIGURE 11-18: EXAMPLE OF HALF-BRIDGE APPLICATIONS**



### 11.4.7 PULSE STEERING MODE

In Single Output mode, pulse steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can be simultaneously available on multiple pins.

Once the Single Output mode is selected (CCP1M<3:2> = 11 and P1M<1:0> = 00 of the CCP1CON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STR<D:A> bits of the PSTRCON register, as shown in Figure 11-19.

| **Note:** | The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin. |
|---|---|

While the PWM Steering mode is active, CCP1M<1:0> bits of the CCP1CON register select the PWM output polarity for the P1<D:A> pins.

The PWM auto-shutdown operation also applies to PWM Steering mode as described in **Section 11.4.4 "Enhanced PWM Auto-shutdown mode"**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

**REGISTER 11-4: PSTRCON: PULSE STEERING CONTROL REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | STRSYNC | STRD | STRC | STRB | STRA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **STRSYNC:** Steering Sync bit
1 = Output steering update occurs on next PWM period
0 = Output steering update occurs at the beginning of the instruction cycle boundary

bit 3 **STRD:** Steering Enable bit D
1 = P1D pin has the PWM waveform with polarity control from CCP1M<1:0>
0 = P1D pin is assigned to port pin

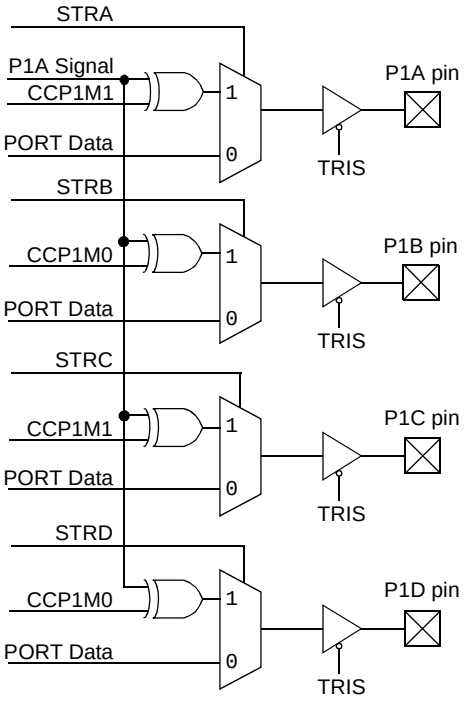
bit 2 **STRC:** Steering Enable bit C
1 = P1C pin has the PWM waveform with polarity control from CCP1M<1:0>
0 = P1C pin is assigned to port pin

bit 1 **STRB:** Steering Enable bit B
1 = P1B pin has the PWM waveform with polarity control from CCP1M<1:0>
0 = P1B pin is assigned to port pin

bit 0 **STRA:** Steering Enable bit A
1 = P1A pin has the PWM waveform with polarity control from CCP1M<1:0>
0 = P1A pin is assigned to port pin

**Note 1:** The PWM Steering mode is available only when the CCP1CON register bits CCP1M<3:2> = 11 and P1M<1:0> = 00.

**FIGURE 11-19: SIMPLIFIED STEERING BLOCK DIAGRAM**




**Note 1:** Port outputs are configured as shown when the CCP1CON register bits P1M<1:0> = 00 and CCP1M<3:2> = 11.

**2:** Single PWM output requires setting at least one of the STRx bits.

### 14.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit (PCON<4>) enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 14-2 for the Configuration Word definition.

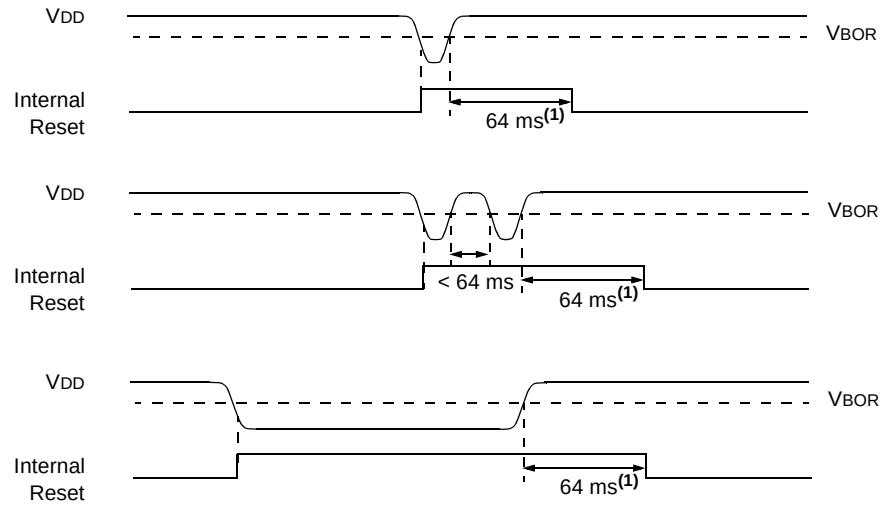
If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 17.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 14-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

| **Note:** | The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word register. |
|---|---|

If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

**FIGURE 14-3: BROWN-OUT SITUATIONS**




**Note 1:** 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

### 14.2.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figures 14-4, 14-5 and 14-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 3.7.2 "Two-speed Start-up Sequence"** and **Section 3.8 "Fail-Safe Clock Monitor"**).

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 14-5). This is useful for testing purposes or to synchronize more than one PIC16F631/677/685/687/689/690 device operating in parallel.

Table 14-5 shows the Reset conditions for some special registers, while Table 14-4 shows the Reset conditions for all the registers.

### 14.2.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is BOR (Brown-out Reset). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if BOR = 0, indicating that a Brown-out has occurred. The BOR Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 4.2.4 "Ultra Low-Power Wake-up"** and **Section 14.2.4 "Brown-out Reset (BOR)"**.

**TABLE 14-1: TIME-OUT IN VARIOUS SITUATIONS**

| Oscillator Configuration | Power-up | | Brown-out Reset | | Wake-up from Sleep |
|---|---|---|---|---|---|
| | PWRTE = 0 | PWRTE = 1 | PWRTE = 0 | PWRTE = 1 | |
| XT, HS, LP | TPWRT + 1024 • TOSC | 1024 • TOSC | TPWRT + 1024 • TOSC | 1024 • TOSC | 1024 • TOSC |
| LP, T1OSCIN = 1 | TPWRT | — | TPWRT | — | — |
| RC, EC, INTOSC | TPWRT | — | TPWRT | — | — |

**TABLE 14-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE**

| POR | BOR | TO | PD | Condition |
|---|---|---|---|---|
| 0 | x | 1 | 1 | Power-on Reset |
| u | 0 | 1 | 1 | Brown-out Reset |
| u | u | 0 | u | WDT Reset |
| u | u | 0 | 0 | WDT Wake-up |
| u | u | u | u | MCLR Reset during normal operation |
| u | u | 1 | 0 | MCLR Reset during Sleep |

**Legend:** u = unchanged, x = unknown

**TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| PCON | — | — | ULPWUE | SBOREN | — | — | POR | BOR | --01 --qq | --0u --uu |
| STATUS | IRP | RP1 | RPO | TO | PD | Z | DC | C | 0001 1xxx | 000q quuu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.
**Note 1:** Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

**TABLE 17-15: A/D CONVERTER (ADC) CHARACTERISTICS**:

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| AD01 | NR | Resolution | — | — | 10 bits | bit | |
| AD02 | EIL | Integral Error | — | — | ±1 | LSb | VREF = 5.12V |
| AD03 | EDL | Differential Error | — | — | ±1 | LSb | No missing codes to 10 bits<br>VREF = 5.12V |
| AD04 | EOFF | Offset Error | — | — | ±1 | LSb | VREF = 5.12V |
| AD04A | | | — | +1.5 | +3.0 | LSb | (PIC16F677 only) |
| AD07 | EGN | Gain Error | — | — | ±1 | LSb | VREF = 5.12V |
| AD06<br>AD06A | VREF | Reference Voltage(3) | 2.2<br>2.5 | — | —<br>VDD | V | <br>Absolute minimum to ensure 1 LSb accuracy |
| AD07 | VAIN | Full-Scale Range | VSS | — | VREF | V | |
| AD08 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | |
| AD09* | IREF | VREF Input Current(3) | 10 | — | 1000 | μA | During VAIN acquisition.<br>Based on differential of VHOLD to VAIN. |
| | | | — | — | 50 | μA | During A/D conversion cycle |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.

**2:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**3:** ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

**4:** When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

**FIGURE 18-24: MAXIMUM VP6 REFERENCE IPD VS. VDD OVER TEMPERATURE**

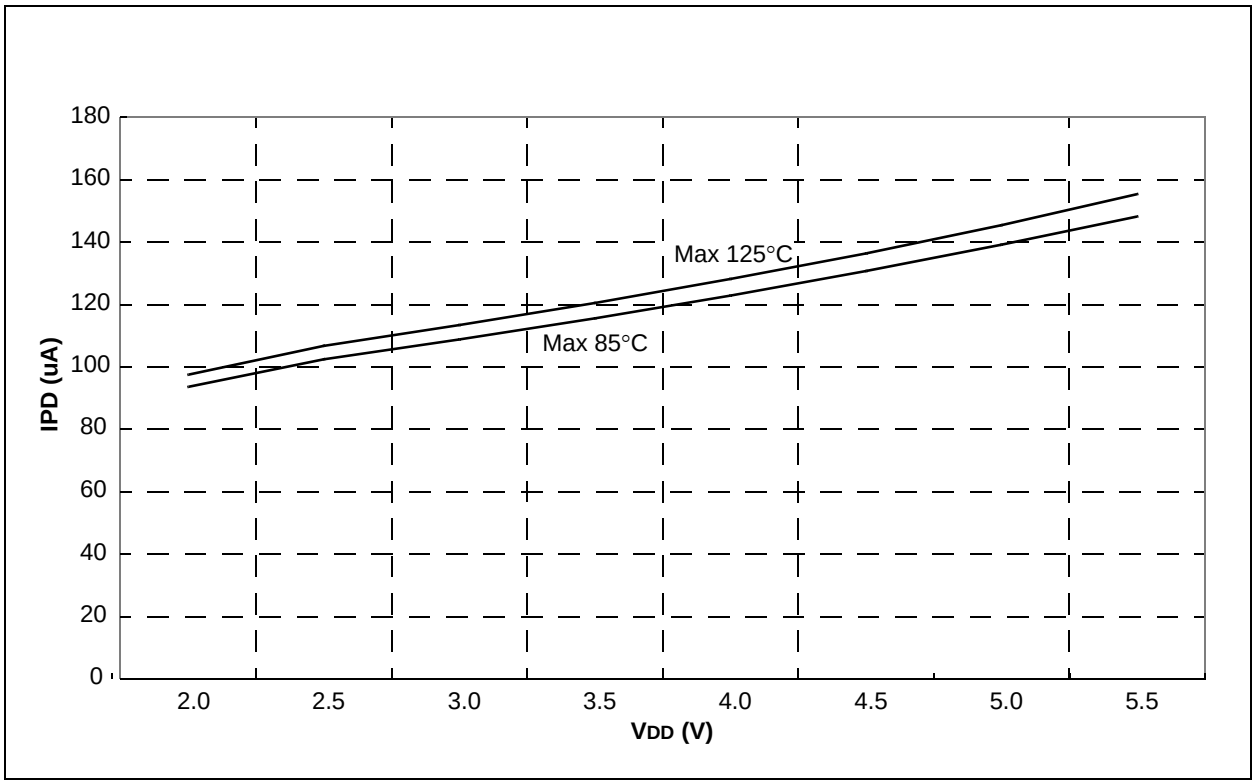



**FIGURE 18-25: T1OSC IPD VS. VDD OVER TEMPERATURE (32 kHz)**

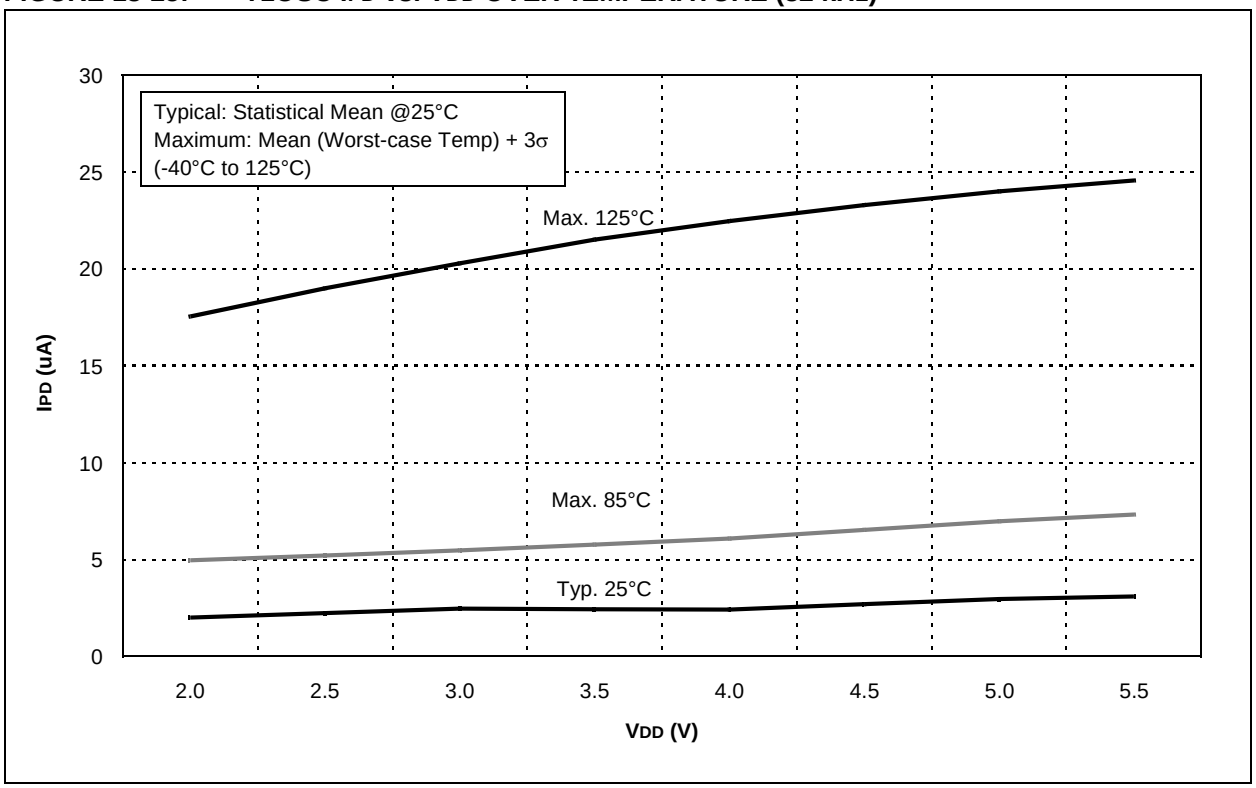


**FIGURE 18-32: COMPARATOR RESPONSE TIME (RISING EDGE)**

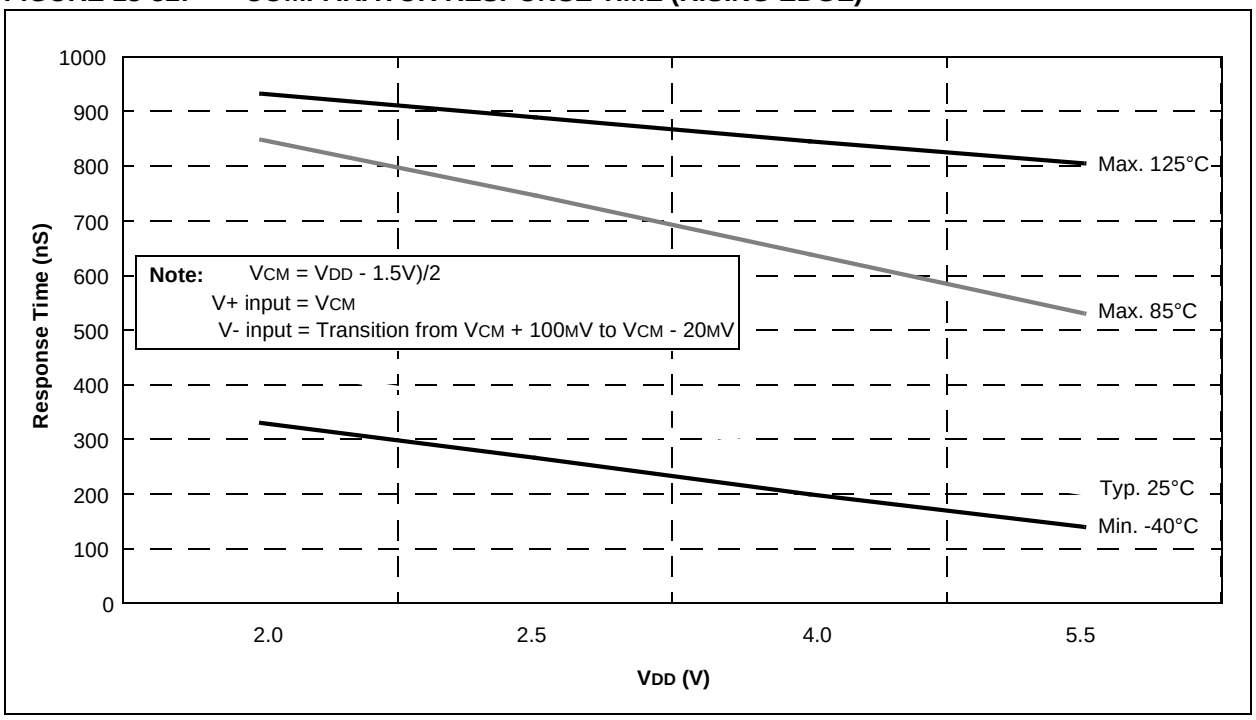
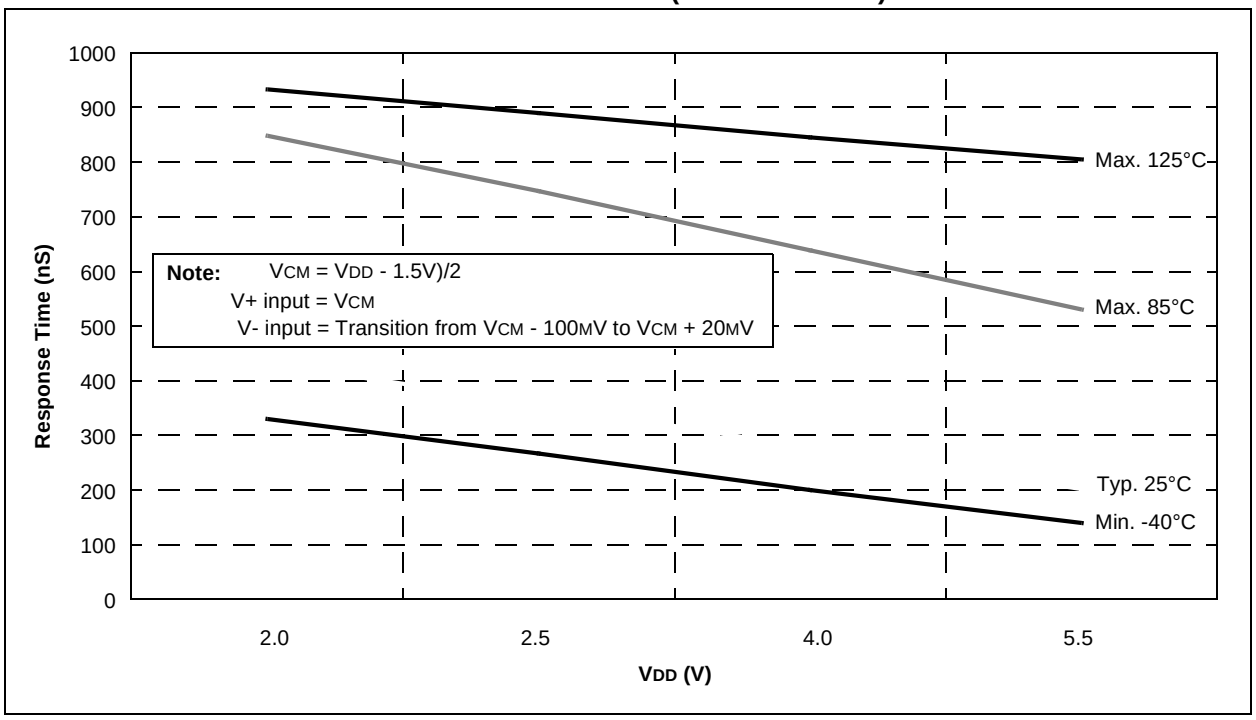



**FIGURE 18-33: COMPARATOR RESPONSE TIME (FALLING EDGE)**

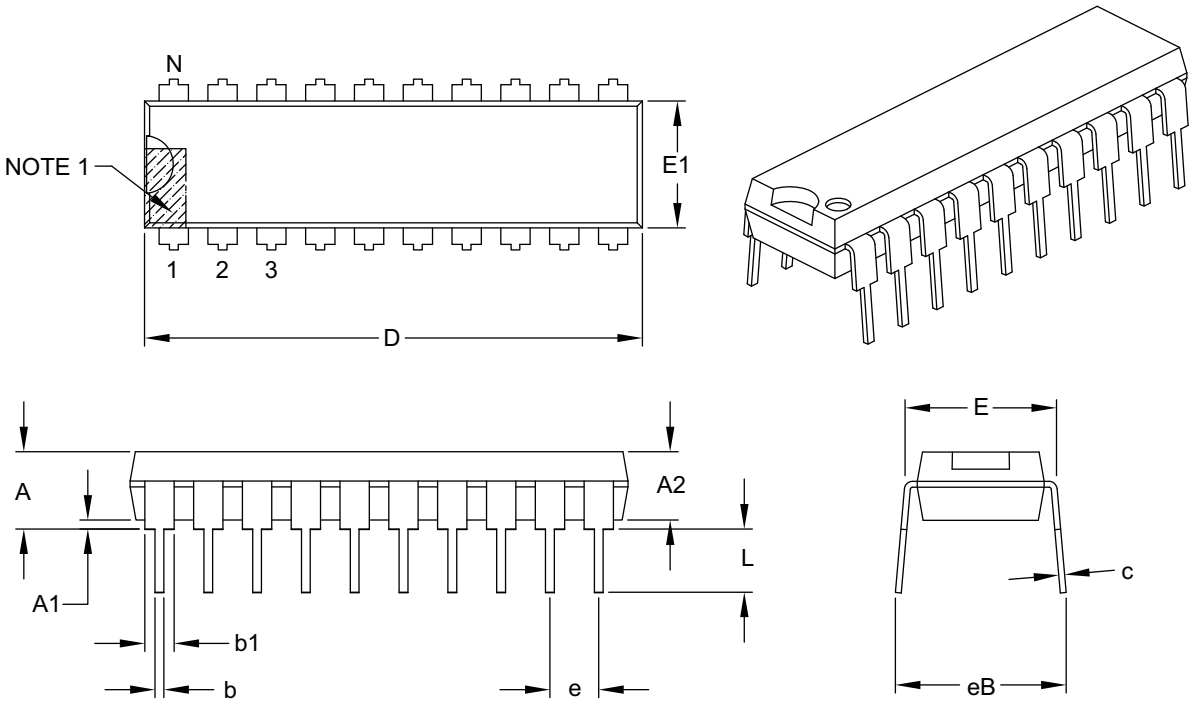


## 19.2 Package Details

The following sections give the technical details of the packages.

### 20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .980 | 1.030 | 1.060 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B