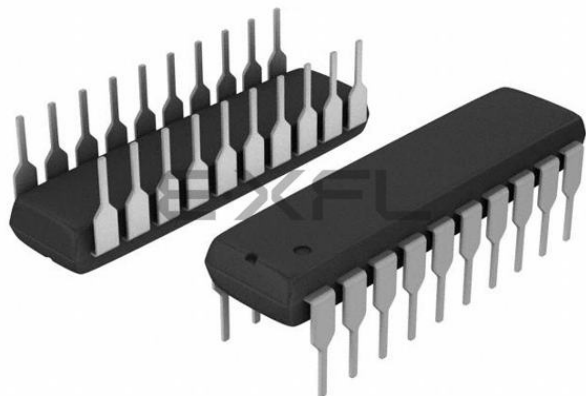




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f690-i-p

PIC16F631/677/685/687/689/690

TABLE 1-2: PINOUT DESCRIPTION – PIC16F677 (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
RC0/AN4/C2IN+	RC0	ST	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	C2IN+	AN	—	Comparator C2 non-inverting input.
RC1/AN5/C12IN1-	RC1	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	C12IN1-	AN	—	Comparator C1 or C2 inverting input.
RC2/AN6/C12IN2-	RC2	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	C12IN2-	AN	—	Comparator C1 or C2 inverting input.
RC3/AN7/C12IN3-	RC3	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	C12IN3-	AN	—	Comparator C1 or C2 inverting input.
RC4/C2OUT	RC4	ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
RC5	RC5	ST	CMOS	General purpose I/O.
RC6/AN8/SS	RC6	ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	SS	ST	—	Slave Select input.
RC7/AN9/SDO	RC7	ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	SDO	—	CMOS	SPI data output.
VSS	VSS	Power	—	Ground reference.
VDD	VDD	Power	—	Positive supply.

Legend: AN = Analog input or output
TTL = TTL compatible input
HV = High Voltage
CMOS=CMOS compatible input or output
ST= Schmitt Trigger input with CMOS levels
XTAL= Crystal

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TABLE 2-2: PIC16F631/677/685/687/689/690 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	43,200
81h	OPTION_REG	RABPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	36,200
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	43,200
83h	STATUS	IRP	RP1	RP0	T0	PD	Z	DC	C	0001 1xxx	35,200
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	43,200
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	57,200
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	68,201
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	74,200
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				---	0 0000	43,200
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF ⁽¹⁾	0000 000x	37,200
8Ch	PIE1	—	ADIE ⁽⁴⁾	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE ⁽⁵⁾	CCP1IE ⁽³⁾	TMR2IE ⁽³⁾	TMR1IE	-000 0000	38,201
8Dh	PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----	39,201
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	POR	BOR	--01 --qq	42,201
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	46,201
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	50,201
91h	—	Unimplemented								—	—
92h	PR2 ⁽³⁾	Timer2 Period Register								1111 1111	89,201
93h	SSPADD ^(5, 7)	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	184,201
93h	SSPMSK ^(5, 7)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111	187,201
94h	SSPSTAT ⁽⁵⁾	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	176,201
95h	WPUA ⁽⁶⁾	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	60,201
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	60,201
97h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	208,201
98h	TXSTA ⁽²⁾	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	157,201
99h	SPBRG ⁽²⁾	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	160,201
9Ah	SPBRGH ⁽²⁾	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	160,201
9Bh	BAUDCTL ⁽²⁾	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	159,201
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL ⁽⁴⁾	A/D Result Register Low Byte								xxxx xxxx	113,201
9Fh	ADCON1 ⁽⁴⁾	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	112,201

- Legend:** — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
- Note 1:** MCLR and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.
- 2:** PIC16F687/PIC16F689/PIC16F690 only.
- 3:** PIC16F685/PIC16F690 only.
- 4:** PIC16F677/PIC16F685/PIC16F687/PIC16F689/PIC16F690 only.
- 5:** PIC16F677/PIC16F687/PIC16F689/PIC16F690 only.
- 6:** RA3 pull-up is enabled when pin is configured as MCLR in Configuration Word.
- 7:** Accessible only when SSPCON register bits SSPM<3:0> = 1001.

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3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							
							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7-5
- bit 4-0
- Unimplemented: Read as '0'

TUN<4:0>: Frequency Tuning bits

01111 = Maximum frequency

01110 =

.

.

.

00001 =

00000 = Oscillator module is running at the factory-calibrated frequency.

11111 =

.

.

.

10000 = Minimum frequency

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3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

FIGURE 3-7: TWO-SPEED START-UP

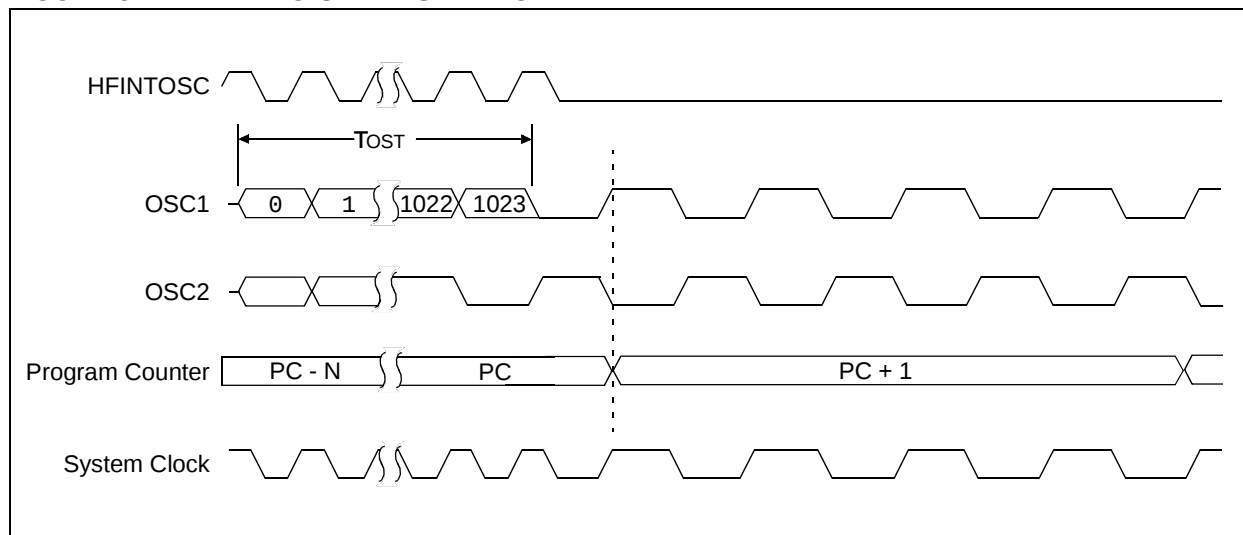
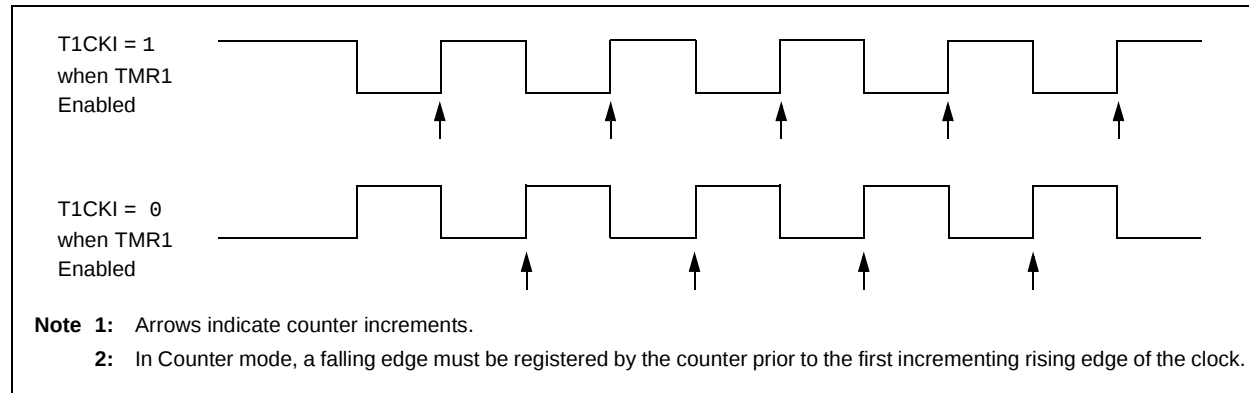


FIGURE 6-2: TIMER1 INCREMENTING EDGE



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TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 0000	0000 0000
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

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11.0 ENHANCED CAPTURE/ COMPARE/PWM MODULE

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

Table 11-1 shows the timer resources required by the ECCP module.

**TABLE 11-1: ECCP MODE – TIMER
RESOURCES REQUIRED**

ECCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 11-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

P1M<1:0>: PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as port pins

If CCP1M<3:2> = 11:

00 = Single output; P1A modulated; P1B, P1C, P1D assigned as port pins

01 = Full-Bridge output forward; P1D modulated; P1A active; P1B, P1C inactive

10 = Half-Bridge output; P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins

11 = Full-Bridge output reverse; P1B modulated; P1C active; P1A, P1D inactive

bit 5-4

DC1B<1:0>: PWM Duty Cycle Least Significant bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSBs of the PWM duty cycle. The eight MSBs are found in CCPR1L.

bit 3-0

CCP1M<3:0>: ECCP Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCP module)

0001 = Unused (reserved)

0010 = Compare mode, toggle output on match (CCP1IF bit is set)

0011 = Unused (reserved)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCP1IF bit is set)

1001 = Compare mode, clear output on match (CCP1IF bit is set)

1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)

1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 or TMR2, and starts an A/D conversion, if the ADC module is enabled)

1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high

1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low

1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high

1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

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11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 3.0 “Oscillator Module (With Fail-Safe Clock Monitor)”** for additional details.

11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output driver by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B<1:0> bits of the CCP1CON register.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Enable the CCP1 pin output driver by clearing the associated TRIS bit.

11.4 PWM (Enhanced Mode)

The Enhanced PWM Mode can generate a PWM signal on up to four different output pins with up to ten bits of resolution. It can do this through four different PWM Output modes:

- Single PWM
- Half-Bridge PWM
- Full-Bridge PWM, Forward mode
- Full-Bridge PWM, Reverse mode

To select an Enhanced PWM mode, the P1M bits of the CCP1CON register must be set appropriately.

The PWM outputs are multiplexed with I/O pins and are designated P1A, P1B, P1C and P1D. The polarity of the PWM pins is configurable and is selected by setting the CCP1M bits in the CCP1CON register appropriately.

Table 11-4 shows the pin assignments for each Enhanced PWM mode.

Figure 11-5 shows an example of a simplified block diagram of the Enhanced PWM module.

Note:	To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.
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FIGURE 11-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

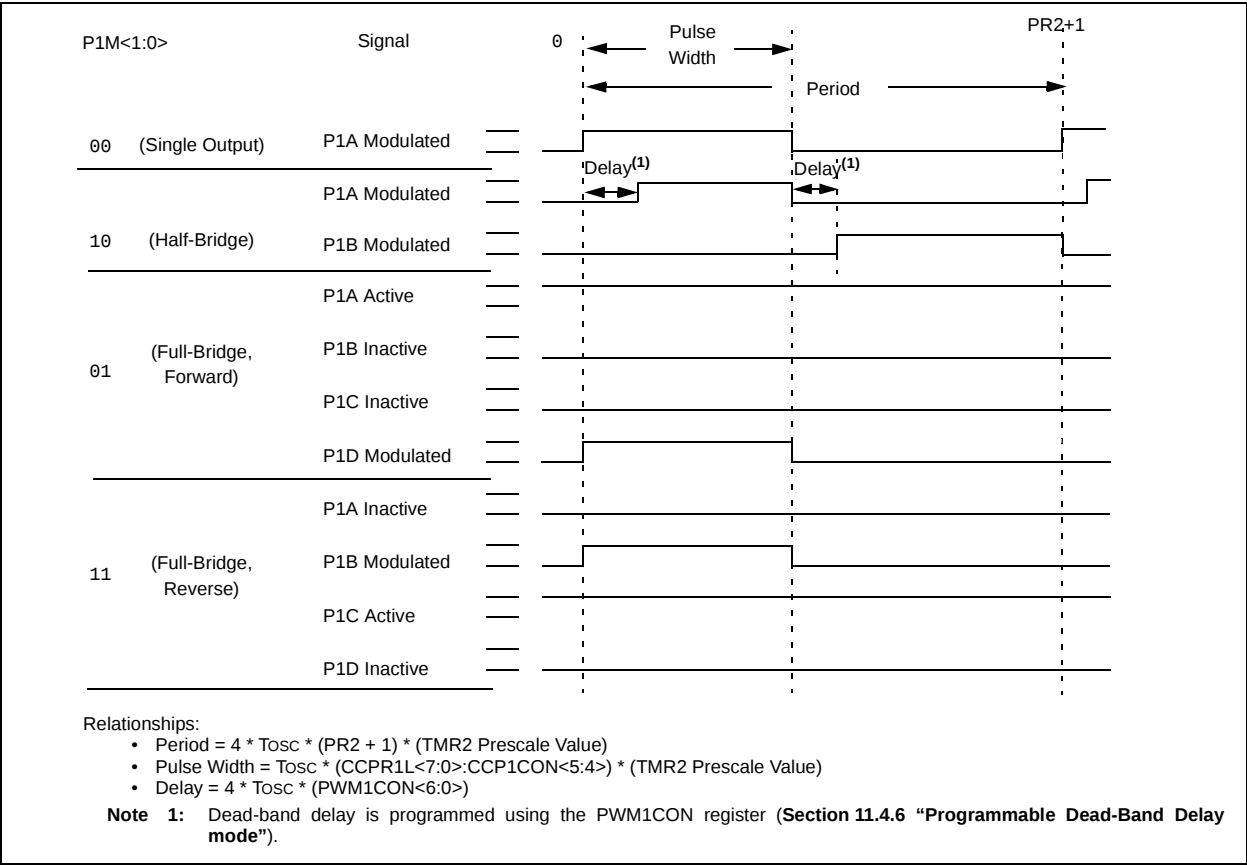
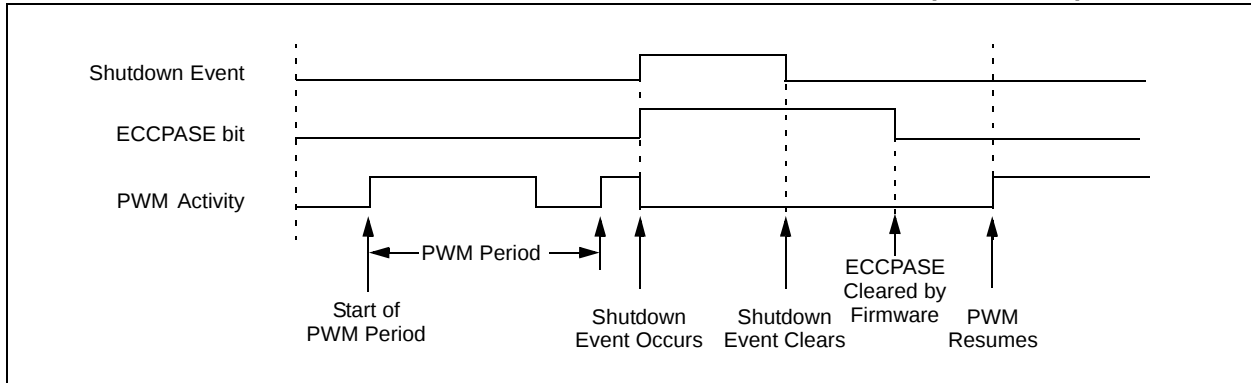


FIGURE 11-15: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)

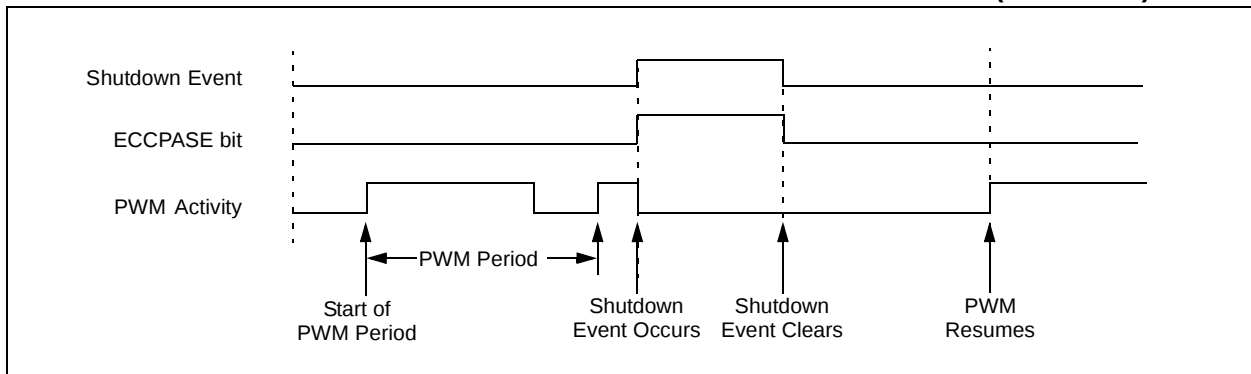


11.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 11-16: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)



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TABLE 12-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00
INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF	0000 000x	0000 000x
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
RCREG	EUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000	0000 0000
TRISB	TRISB7	TRISB6	TRISB5	TRISB4					1111 ----	1111 ----
TXREG	EUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	0000 0010	0000 0010

Legend: x = unknown, – = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

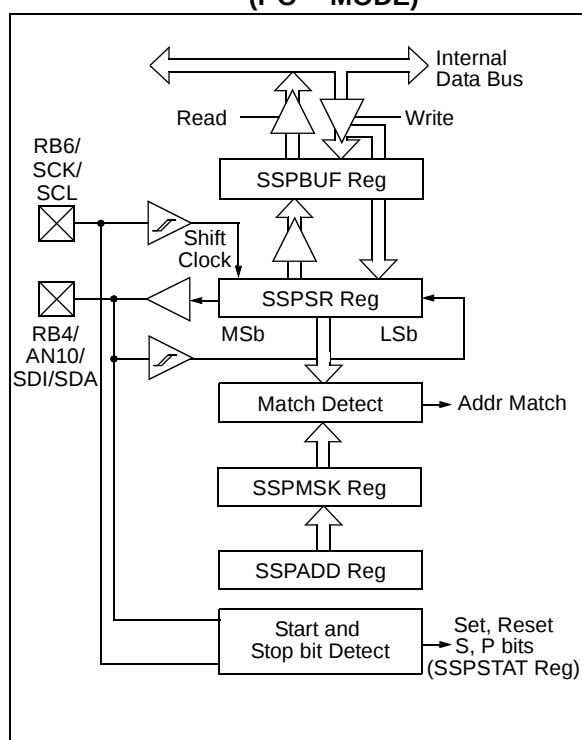
13.11 SSP I²C Operation

The SSP module in I²C mode, fully implements all slave functions, except general call support, and provides interrupts on Start and Stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RB6/SCK/SCL pin, which is the clock (SCL), and the RB4/AN10/SDI/SDA pin, which is the data (SDA).

The SSP module functions are enabled by setting SSP enable bit SSPEN (SSPCON<5>).

FIGURE 13-7: SSP BLOCK DIAGRAM (I²C™ MODE)



The SSP module has six registers for the I²C operation, which are listed below.

- SSP Control register (SSPCON)
- SSP Status register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift register (SSPSR) – Not directly accessible
- SSP Address register (SSPADD)
- SSP Mask register (SSPMSK)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I²C Slave mode (10-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I²C Start and Stop bit interrupts enabled to support Firmware Master mode; Slave is idle

Selection of any I²C mode with the SSPEN bit set forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISB bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

13.12 Slave Mode

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISB<6,4> are set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (ACK) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this ACK pulse. They include (either or both):

- The Buffer Full bit BF of the SSPSTAT register was set before the transfer was received.
- The overflow bit SSPOV of the SSPCON register was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 13-3 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. For high and low times of the I²C specification, as well as the requirements of the SSP module, see **Section 17.0 “Electrical Specifications”**.

13.13 Master Mode

Master mode of operation is supported in firmware using interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit is set or the bus is idle and both the S and P bits are clear.

In Master mode, the SCL and SDA lines are manipulated by clearing the corresponding TRISB<6,4> bit(s). The output level is always low, irrespective of the value(s) in PORTB<6,4>. So when transmitting data, a '1' data bit must have the TRISB<4> bit set (input) and a '0' data bit must have the TRISB<4> bit cleared (output). The same scenario is true for the SCL line with the TRISB<6> bit. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt will occur if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the Slave mode idle (SSPM<3:0> = 1011), or with the Slave active. When both Master and Slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

13.14 Multi-Master Mode

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions, allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the Stop condition occurs.

In Multi-Master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISB<6,4>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

13.14.1 CLOCK SYNCHRONIZATION AND THE CKP BIT

When the CKP bit is cleared, the SCL output is forced to '0'; however, setting the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I²C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I²C bus have deasserted SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 13-12).

14.2 Reset

The PIC16F631/677/685/687/689/690 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

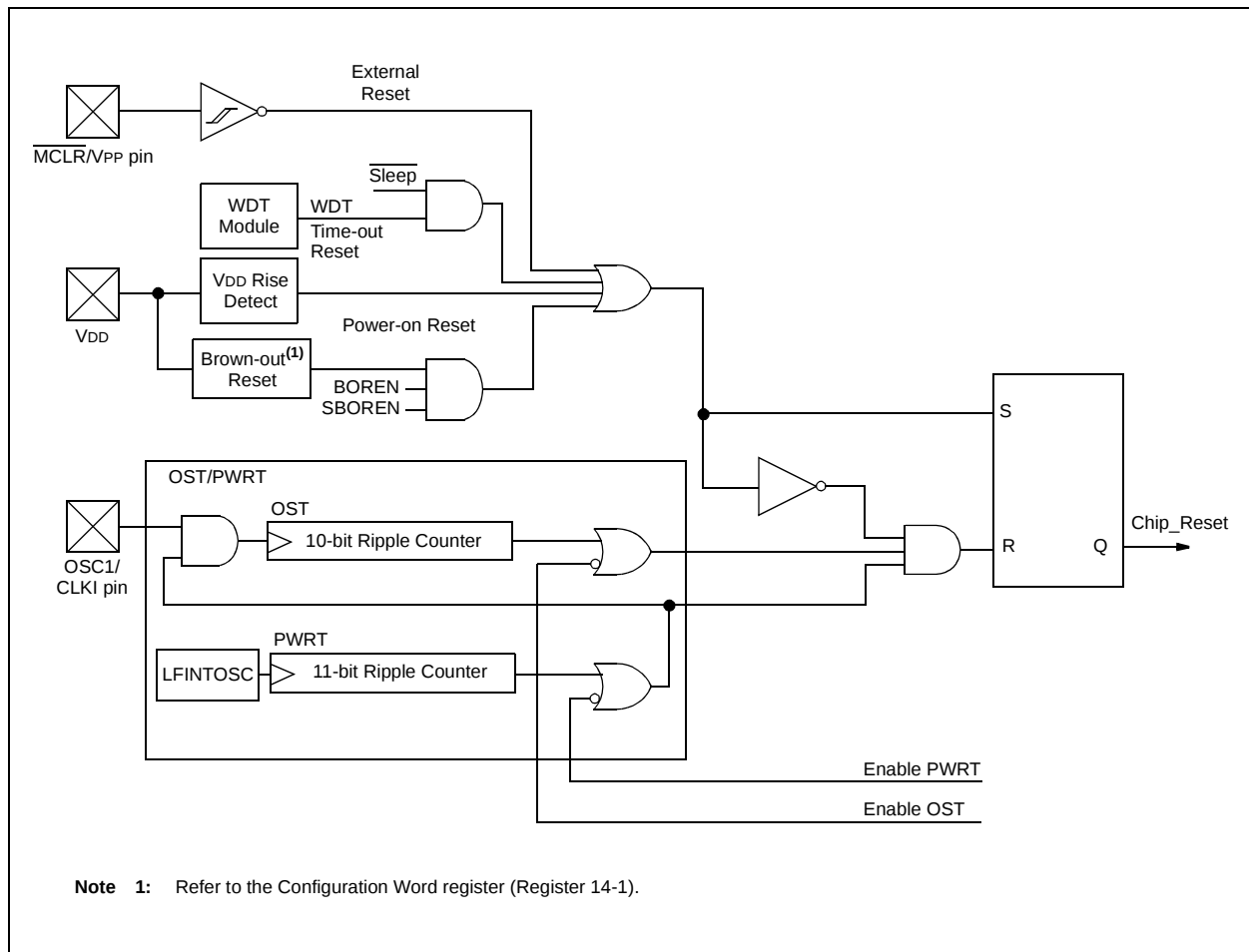
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

They are not affected by a WDT Wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 14-2. These bits are used in software to determine the nature of the Reset. See Table 14-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 14-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 17.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 14-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



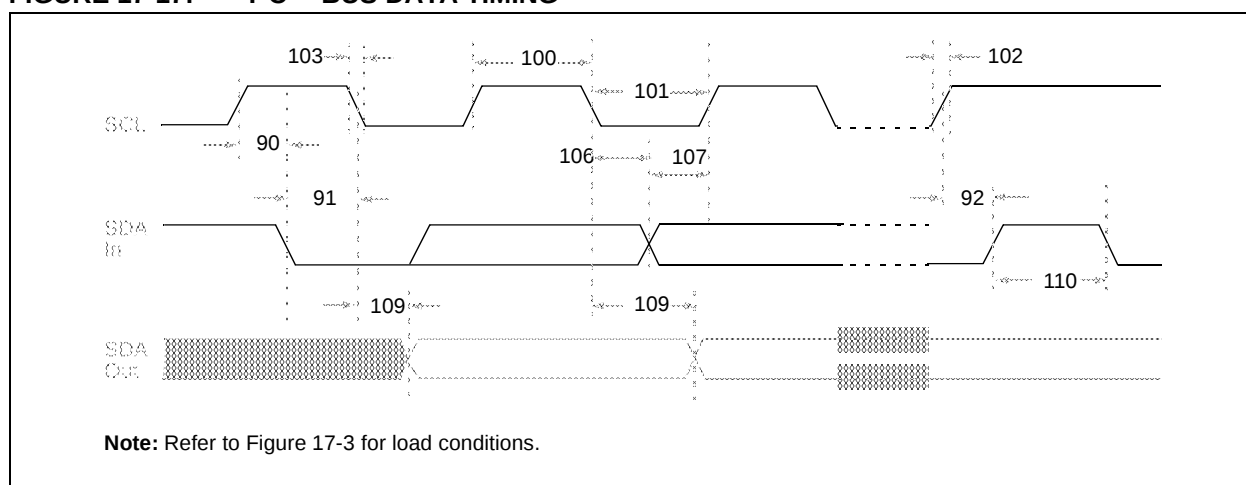
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TABLE 17-13: I²C™ BUS START/STOP BITS REQUIREMENTS

Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
90*	TSU:STA	Start condition	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
		Setup time	400 kHz mode	600	—	—		
91*	THD:STA	Start condition	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92*	TSU:STO	Stop condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	Stop condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 17-17: I²C™ BUS DATA TIMING



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TABLE 17-15: A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	± 1	LSb	$V_{REF} = 5.12\text{V}$
AD03	EDL	Differential Error	—	—	± 1	LSb	No missing codes to 10 bits $V_{REF} = 5.12\text{V}$
AD04	E _{OFF}	Offset Error	—	—	± 1	LSb	$V_{REF} = 5.12\text{V}$
AD04A			—	+1.5	+3.0	LSb	(PIC16F677 only)
AD07	E _{GN}	Gain Error	—	—	± 1	LSb	$V_{REF} = 5.12\text{V}$
AD06 AD06A	V _{REF}	Reference Voltage ⁽³⁾	2.2 2.5	—	— V _{DD}	V	Absolute minimum to ensure 1 LSb accuracy
AD07	V _{AIN}	Full-Scale Range	V _{SS}	—	V _{REF}	V	
AD08	Z _{AIN}	Recommended Impedance of Analog Voltage Source	—	—	10	k Ω	
AD09*	I _{REF}	V _{REF} Input Current ⁽³⁾	10	—	1000	μA	During V _{AIN} acquisition. Based on differential of V _{HOLD} to V _{AIN} .
			—	—	50	μA	During A/D conversion cycle

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC V_{REF} is from external V_{REF} or V_{DD} pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

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FIGURE 18-22: CVREF IPD vs. VDD OVER TEMPERATURE (LOW RANGE)

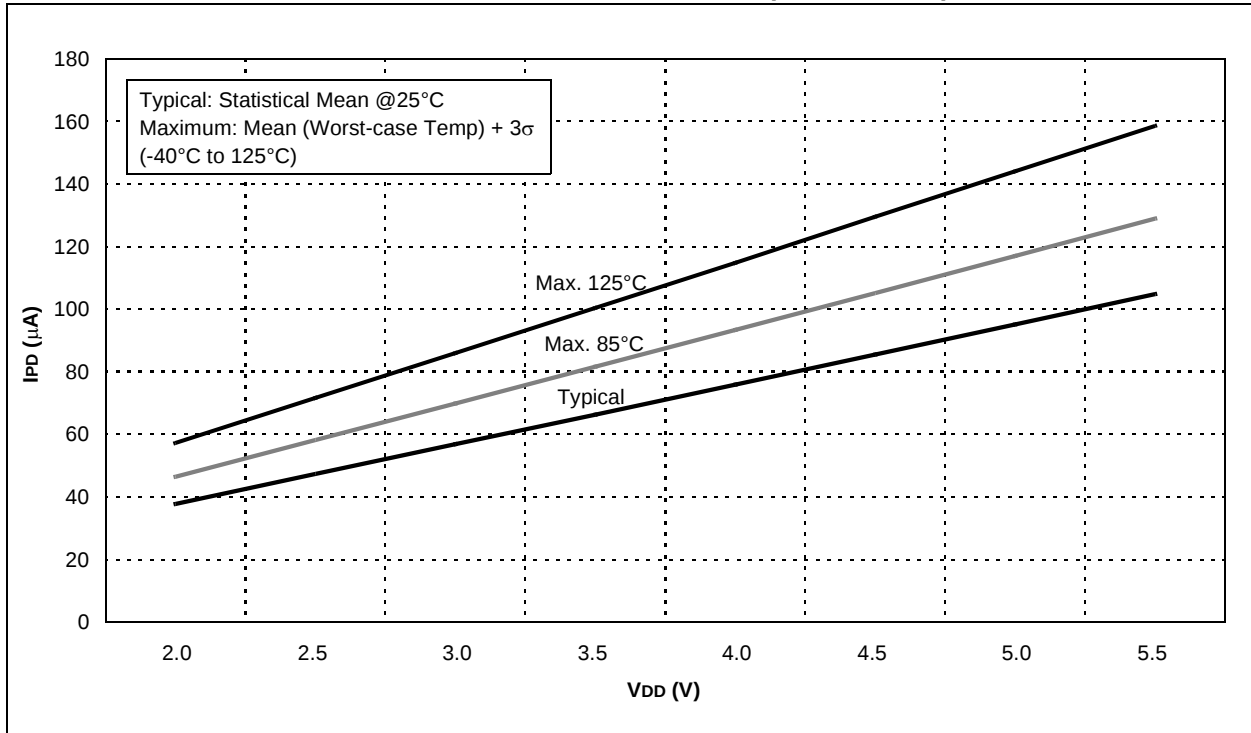
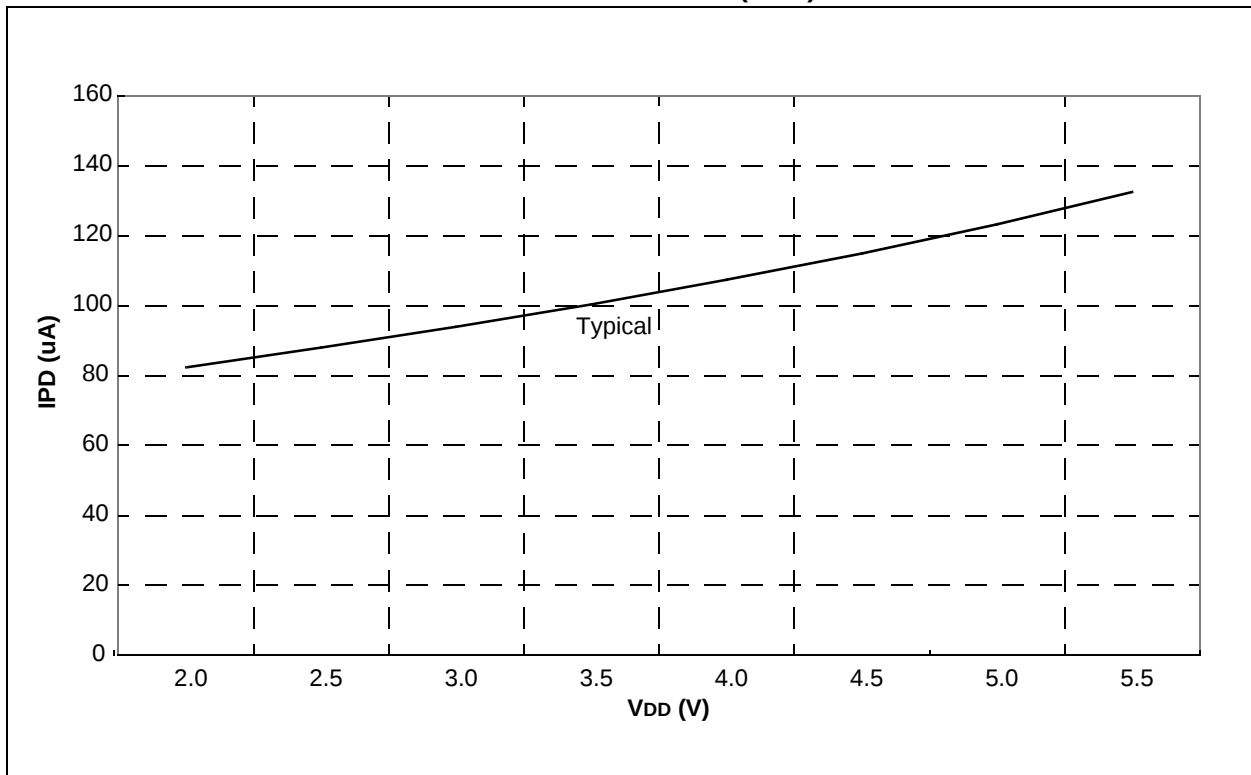


FIGURE 18-23: TYPICAL VP6 REFERENCE IPD vs. VDD (25°C)



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FIGURE 18-30: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

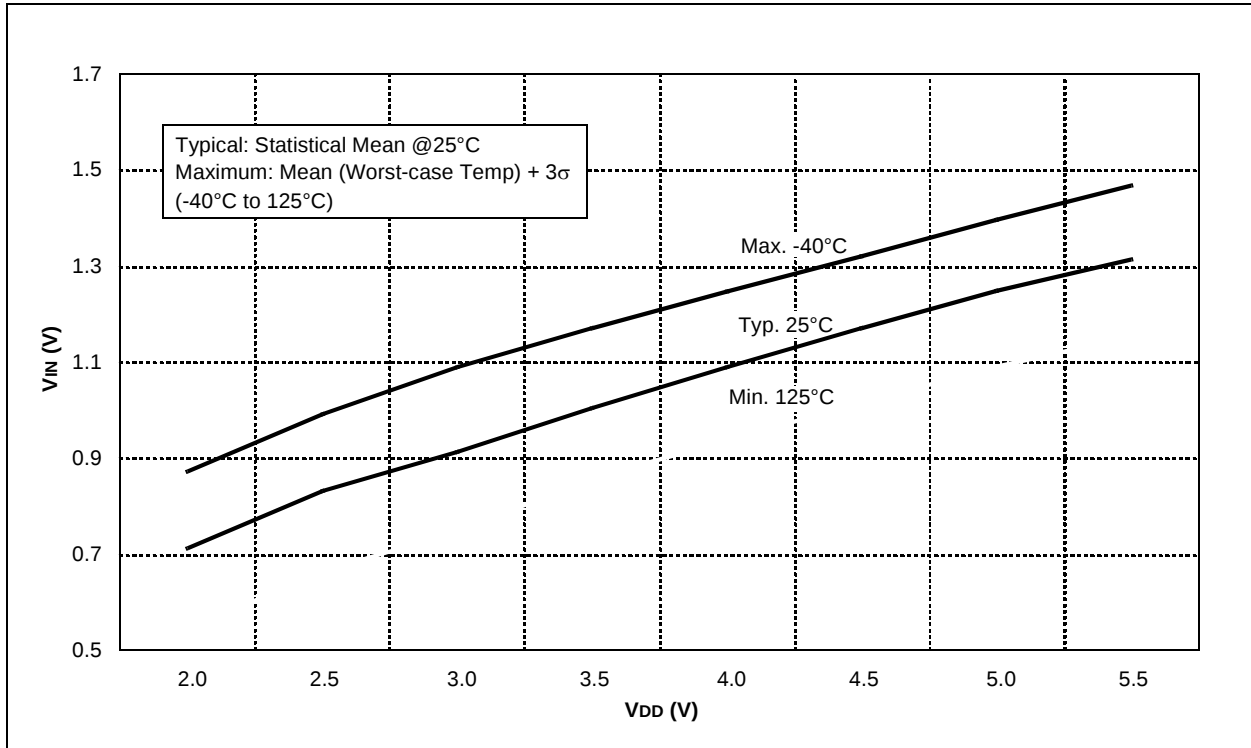
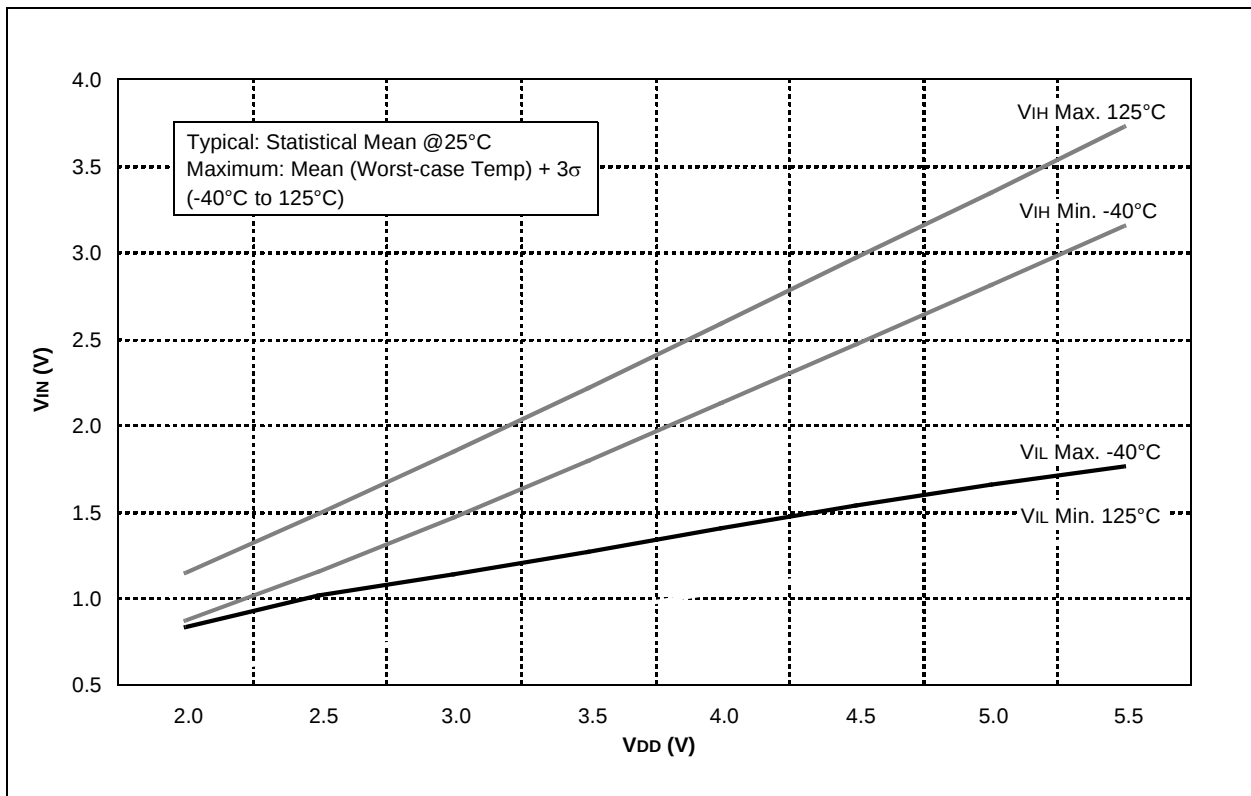


FIGURE 18-31: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE



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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (March 2005)

This is a new data sheet.

Revision B (May 2006)

Added 631/677 part numbers; Added pin summary tables after pin diagrams; Incorporated Golden Chapters.

Revision C (July 2006)

Revised Section 4.2.1, ANSEL and ANSELH Registers; Register 4-3, ANSEL Analog Select; Added Register 4-4, ANSELH Analog Select High; Section 11.3.2, Revised CCP1<1:0> to DC1B<1:0>; Section 11.3.7, Number 4 - Revised CCP1 to DC1B; Figure 11-5, Revised CCP1 to DC1B; Table 11-4, Revised P1M to P1M<1:0>; Section 12.3.1, Revised Paragraph 3; Revised Note 2; Revised Figure 12-6 Title.

Revision D (February 2007)

Removed Preliminary status; Changed PICmicro to PIC; Replaced Dev. Tool Section; Replaced Package Drawings.

Revision E (March 2008)

Add Char Data charts; Updated EUSART Golden Chapter; Updated the Electrical Specification section; Updated Package Drawings as needed.

Revision F (April 2015)

Added Section 17.8: High Temperature Operation in the Electrical Specifications section.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC16F6XX Family of devices.

B.1 PIC16F676 to PIC16F685

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F685
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	4096
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2
ECCP+	N	Y
Ultra Low-Power Wake-up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	31 kHz-8 MHz
Clock Switching	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

PIC16F631/677/685/687/689/690

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device: PIC16F631⁽¹⁾, PIC16F677⁽¹⁾, PIC16F685⁽¹⁾, PIC16F687⁽¹⁾, PIC16F689⁽¹⁾, PIC16F690⁽¹⁾; VDD range 2.0V to 5.5V Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) Package: ML = QFN (Quad Flat, no lead) P = PDIP SO = SOIC SS = SSOP Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise)			

Examples:	
a)	PIC16F685 - I/ML 301 = Industrial temp., QFN package, QTP pattern #301.
b)	PIC16F689 - I/SO = Industrial temp., SOIC package.
c)	PIC16F690T - E/SS = Extended temp., SSOP package.

Note	1: T = in tape and reel SSOP, SOIC and QFN packages only.
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