Analog Devices Inc. - ADSP-BF592BCPZ-2 Datasheet

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	I²C, I²S, IrDA, PPI, SPI, SPORT, UART
Clock Rate	200MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	64kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.29V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf592bcpz-2

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initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine whether the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

Timers

There are four general-purpose programmable timer units in the processor. Three timers have an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

Serial Ports

The ADSP-BF592 processor incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processor has two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and many SPI chip select output pins ($\overline{\text{SPIx\_SEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

UART Port

The ADSP-BF592 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Parallel Peripheral Interface (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel analog-to-digital and digital-to-analog converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate, and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

Note that when a GPIO pin is used to trigger wake from deep sleep, the programmed wake level must linger for at least 10ns to guarantee detection.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling clocks to the processor core (CCLK) and to all of the peripherals (SCLK), as well as signaling an external voltage regulator that V_{DDINT} can be shut off. Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Writing b#0 to the $\overline{\text{HIBERNATE}}$ bit causes EXT_WAKE to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

As long as V_{DDEXT} is applied, the VR_CTL register maintains its state during hibernation. All other internal registers and memories, however, lose their content in the hibernate state.

Power Savings

As shown in Table 3, the processor supports two different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions, even if the feature/peripheral is not used.

Table 3. Power Domains

Power Domain	V_{DD} Range
All internal logic and memories	V_{DDINT}
All other I/O	V_{DDEXT}

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

$$\textit{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ \textit{Power Savings} = (1 - \textit{Power Savings Factor}) \times 100\%$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

VOLTAGE REGULATION

The ADSP-BF592 processor requires an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, the external supply, V_{DDEXT}, can still be applied, eliminating the need for external buffers. The external voltage regulator can be activated from this power-down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. EXT_WAKE indicates a wakeup to the external voltage regulator.

The power good ($\overline{\text{PG}}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the power-good functionality, refer to the *ADSP-BF59x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not

recommended. The two capacitors and the series resistor shown in Figure 4 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

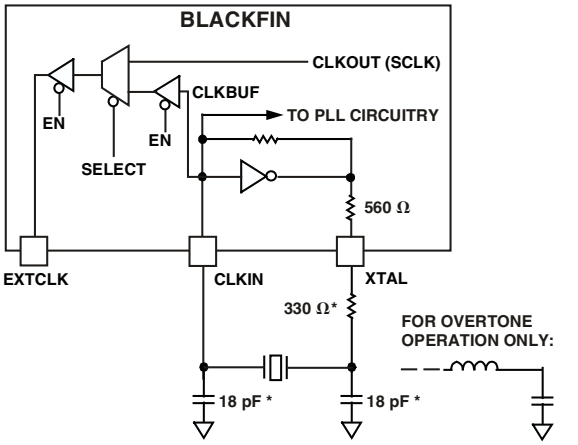

Figure 4. External Crystal Connections

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 5, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 6×, but it can be modified by a software instruction sequence.

On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}; the VCO is always permitted to run up to the frequency specified by the part's instruction rate. The EXTCLK pin can be configured to output either the SCLK frequency or the input buffered CLKIN frequency, called CLKBUF. When configured to output SCLK (CLKOUT), the EXTCLK pin acts as a reference signal in many timing specifications. While three-stated by default, it can be enabled using the VRCTL register.

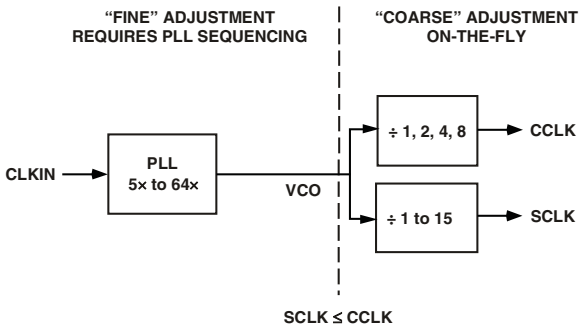

Figure 5. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 4 illustrates typical system clock ratios.

Table 4. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	100	50
0110	6:1	300	50
1010	10:1	400	40

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 5. This programmable core clock capability is useful for fast core frequency modifications.

Table 5. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency *both* depends on the part's instruction rate (see Ordering Guide) *and* depends on the applied V_{DDINT} voltage. See Table 8 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT} and V_{DDEXT} voltages (see Table 10).

BOOTING MODES

The processor has several mechanisms (listed in Table 6) for automatically loading internal and external memory after a reset. The boot mode is defined by the BMODE input pins dedicated to this purpose. There are two categories of boot modes. In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from external host devices.

Table 6. Booting Modes

BMODE2–0	Description
000	Idle/No Boot
001	Reserved
010	SPI1 master boot from Flash, using $\overline{\text{SPI1\_SSEL5}}$ on PG11
011	SPI1 slave boot from external master
100	SPI0 master boot from Flash, using $\overline{\text{SPI0\_SSEL2}}$ on PF8
101	Boot from PPI port
110	Boot from UART host device
111	Execute from Internal L1 ROM

The boot modes listed in Table 6 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time. The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 6.

- IDLE State/No Boot (BMODE - 0x0) — In this mode, the boot kernel transitions the processor into Idle state. The processor can then be controlled through JTAG for recovery, debug, or other functions.
- SPI1 master boot from flash (BMODE = 0x2) — In this mode, SPI1 is configured to operate in master mode and to connect to 8-, 16-, 24-, or 32-bit addressable devices. The processor uses the PG11/$\overline{\text{SPI1\_SSEL5}}$ to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0×00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected, and begins clocking data into the processor. Pull-up resistors are required on the SSEL and MISO pins. By default, a value of 0×85 is written to the SPI_BAUD register.
- SPI1 slave boot from external master (BMODE = 0x3) — In this mode, SPI1 is configured to operate in slave mode and to receive the bytes of the .LDR file from a SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal to the host device not to send any more bytes until the pin is deasserted. The host must interrogate the HWAIT signal, available on PG4, before transmitting every data unit to the processor. A pull-up resistor is required on the $\overline{\text{SPI1\_SS}}$ input. A pull-down on the serial clock may improve signal quality and booting robustness.
- SPI0 master boot from flash (BMODE = 0x4) — In this mode SPI0 is configured to operate in master mode and to connect to 8-, 16-, 24-, or 32-bit addressable devices. The processor uses the PF8/$\overline{\text{SPI0\_SSEL2}}$ to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0×00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected, and begins clocking data into the processor. Pull-up resistors are required on the SSEL and MISO pins. By default, a value of 0×85 is written to the SPI_BAUD register.
- Boot from PPI host device (BMODE = 0x5) — The processor operates in PPI slave mode and is configured to receive the bytes of the LDR file from a PPI host (master) agent.
- Boot from UART host device (BMODE = 0x6) — In this mode UART0 is used as the booting source. Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities. When performing the autobaud, the UART expects a "@" (0×40) character (eight bits data, one start bit, one stop bit, no parity bit) on the RXD pin to determine the bit rate. The UART then replies with an acknowledgment which is composed of 4 bytes (0xBF—the value of UART_DLL) and (0×00—the value of UART_DLH). The host can then download the boot stream. To hold off the host the processor signals the host with the boot host wait (HWAIT) signal. Therefore, the host must monitor the HWAIT, (on PG4), before every transmitted byte.
- Execute from internal L1 ROM (BMODE = 0x7) — In this mode the processor begins execution from the on-chip 64k byte L1 instruction ROM starting at address 0xFFA1 0000.

For each of the boot modes (except Execute from internal L1 ROM), a 16 byte header is first brought in from an external device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the latter case. Bits 7–4 in the system reset configuration (SYSCR) register can be used to bypass the boot kernel or simulate a wakeup-from-hibernate boot in case of a software reset.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to speed up booting by managing the PLL, clock frequencies, or serial bit rates.

The boot ROM also features C-callable functions that can be called by the user application at run time. This enables second stage boot or boot management schemes to be implemented with ease.

SPECIFICATIONS

Specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage	Non-Automotive Models	1.1		1.47	V
	Internal Supply Voltage	Automotive Models	1.33		1.47	V
V_{DDEXT}	External Supply Voltage	Non-Automotive Models	1.7	1.8/2.5/3.3	3.6	V
	External Supply Voltage	Automotive Models	2.7		3.6	V
V_{IH}	High Level Input Voltage[1, 2]	V_{DDEXT} = 1.9 V	1.1			V
$V_{IHCLKIN}$	High Level Input Voltage[1, 2]	V_{DDEXT} = 1.9 V	1.2			V
V_{IH}	High Level Input Voltage[1, 2]	V_{DDEXT} = 2.75 V	1.7			V
V_{IH}	High Level Input Voltage[1, 2]	V_{DDEXT} = 3.6 V	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[1, 2]	V_{DDEXT} = 3.6 V	2.2			V
V_{IHTWI}	High Level Input Voltage[3]	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{DDEXT}		3.6	V
V_{IL}	Low Level Input Voltage[1, 2]	V_{DDEXT} = 1.7 V			0.6	V
V_{IL}	Low Level Input Voltage[1, 2]	V_{DDEXT} = 2.25 V			0.7	V
V_{IL}	Low Level Input Voltage[1, 2]	V_{DDEXT} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage[3]	V_{DDEXT} = Minimum			0.3 × V_{DDEXT}	V
T_J	Junction Temperature	64-Lead LFCSP @ $T_{AMBIENT}$ = 0°C to +70°C	0		80	°C
T_J	Junction Temperature	64-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+95	°C
T_J	Junction Temperature	64-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+115	°C

[1] Bidirectional leads (PF15–0, PG15–0) and input leads (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF592 processor are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[2] Parameter value applies to all input and bidirectional leads, except SDA and SCL.

[3] Parameter applies to SDA and SCL.

ADSP-BF592 Clock Related Operating Conditions

Table 8 describes the core clock timing requirements for the ADSP-BF592 processor. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 10). Table 9 describes phase-locked loop operating conditions.

Table 8. Core Clock (CCLK) Requirements

Parameter		Min V_{DDINT}	Nom V_{DDINT}	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency (All Models)	1.33 V	1.400 V	400	MHz
	Core Clock Frequency (Industrial/Commercial Models)	1.16 V	1.225 V	300	MHz
	Core Clock Frequency (Industrial/Commercial Models)	1.10 V	1.150 V	250[1]	MHz

[1] See the Ordering Guide on Page 44.

Table 9. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Non-Automotive Models)	72	Instruction Rate[1]	MHz
	Voltage Controlled Oscillator (VCO) Frequency (Automotive Models)	84	Instruction Rate[1]	MHz

[1] See the Ordering Guide on Page 44.

Table 10. Maximum SCLK Conditions

Parameter[1]		V_{DDEXT} 1.8 V/2.5 V/3.3 V Nominal	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq 1.16$ V)	100	MHz
	CLKOUT/SCLK Frequency ($V_{DDINT} < 1.16$ V)	80	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK}.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V
V_{OLTWI}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V V
I_{IH}	High Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{IL}	Low Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10	µA
I_{IHP}	High Level Input Current JTAG[2]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V	10		50	µA
I_{OZH}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{OZHTWI}	Three-State Leakage Current[4]	V_{DDEXT} = 3.0 V, V_{IN} = 3.6 V			10	µA
I_{OZL}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10	µA
C_{IN}	Input Capacitance[5]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[6]	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.2 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		0.8		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.2 V, f_{SCLK} = 25 MHz, T_J = 25°C		4		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.2 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.35		6		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 200 MHz, T_J = 25°C, ASF = 1.00		40		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		66		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.4 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		91		mA
$I_{DDHIBERNATE}$[7]	Hibernate State Current	V_{DDEXT} = 3.3 V, T_J = 25°C, CLKIN = 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		20		µA
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 12	mA
I_{DDINT}[8]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 12 + (Table 13 × ASF)	mA

[1] Applies to input pins.
[2] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable pins.
[4] Applies to bidirectional pins SCL and SDA.
[5] Applies to all signal pins.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF59x Blackfin Processor Hardware Reference Manual* for definitions of sleep, deep sleep, and hibernate operating modes.
[8] See Table 11 for the list of I_{DDINT} power vectors covered.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 14 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	–0.3 V to +1.50 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT}+0.5 V
I_{OH}/I_{OL} Current per Pin Group	55 mA (Max)
I_{OH}/I_{OL} Current per Individual Pin	25 mA (Max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased (Non-Automotive Models)	+110°C
Junction Temperature While Biased (Automotive Models)	+115°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 15.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 Volts.

Table 15. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.5	+3.8	100%
–0.7	+4.0	40%
–0.8	+4.1	25%
–0.9	+4.2	15%
–1.0	+4.3	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, EXT_WAKE.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified, and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. The is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

Table 14 specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins and for individual pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PF0 and PF1 from Group 1 in Table 16 were sourcing or sinking 10 mA each, the total current for those pins would be 20 mA. This would allow up to 35 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. It should also be noted that the maximum source or sink current for an individual pin cannot exceed 25 mA. The list of all groups and their pins are shown in Table 16. Note that the V_{OH} and V_{OL} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 16. Total Current Pin Groups–V_{DDEXT} Groups

Group	Pins in Group
1	PF0, PF1, PF2, PF3
2	PF4, PF5, PF6, PF7
3	PF8, PF9, PF10, PF11
4	PF12, PF13, PF14, PF15
5	PG3, PG2, PG1, PG0
6	PG7, PG6, PG5, PG4
7	PG11, PG10, PG9, PG8
8	PG15, PG14, PG13, PG12
9	TDI, TDO, EMU, TCK, $\overline{TRST}$, TMS
10	BMODE2, BMODE1, BMODE0
11	EXT_WAKE, $\overline{PG}$, $\overline{RESET}$, $\overline{NMI}$, PPI_CLK, EXTCLK
12	SDA, SCL, CLKIN, XTAL

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, and CLKIN Pins are Stable and within Specification	$3500 \times t_{CKIN}$		µs

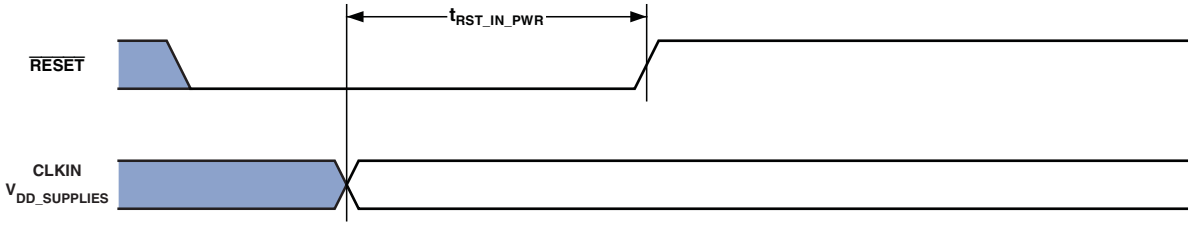

Figure 8. Power-Up Reset Timing

Parallel Peripheral Interface Timing

Table 20 and Figure 9 through Figure 13 describe parallel peripheral interface operations.

Table 20. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	t_{SCLK} – 1.5		t_{SCLK} – 1.5		ns
t_{PCLK}	PPI_CLK Period[1]	2 × t_{SCLK} – 1.5		2 × t_{SCLK} – 1.5		ns
Timing Requirements—GP Input and Frame Capture Modes						
t_{PSUD}	External Frame Sync Startup Delay[2]	4 × t_{PCLK}		4 × t_{PCLK}		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.8		1.6		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	4.1		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	2		1.6		ns
Switching Characteristics—GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		9.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.7		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	2.3		1.9		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] The PPI port is fully enabled 4 PPI clock cycles after the PAB write to the PPI port enable bit. Only after the PPI port is fully enabled are external frame syncs and data words guaranteed to be received correctly by the PPI peripheral.

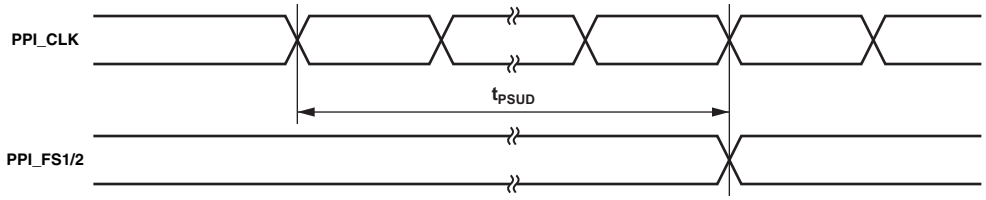

Figure 9. PPI with External Frame Sync Timing

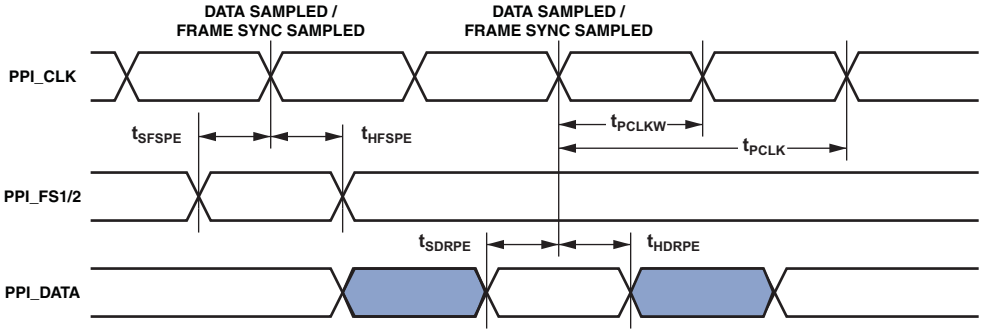

Figure 10. PPI GP Rx Mode with External Frame Sync Timing

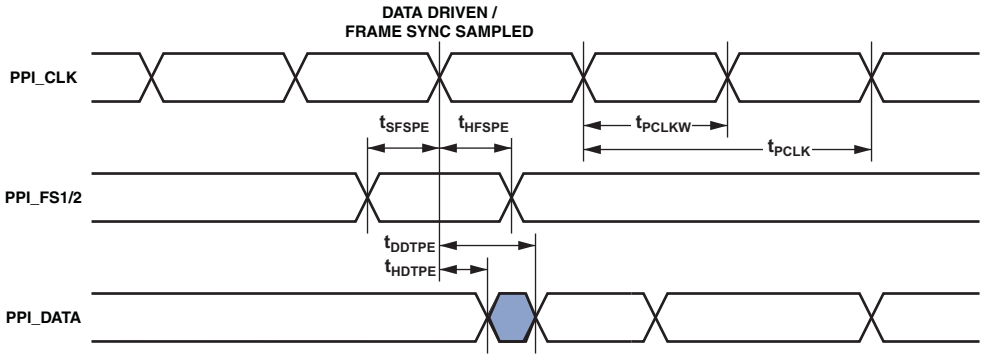

Figure 11. PPI GP Tx Mode with External Frame Sync Timing

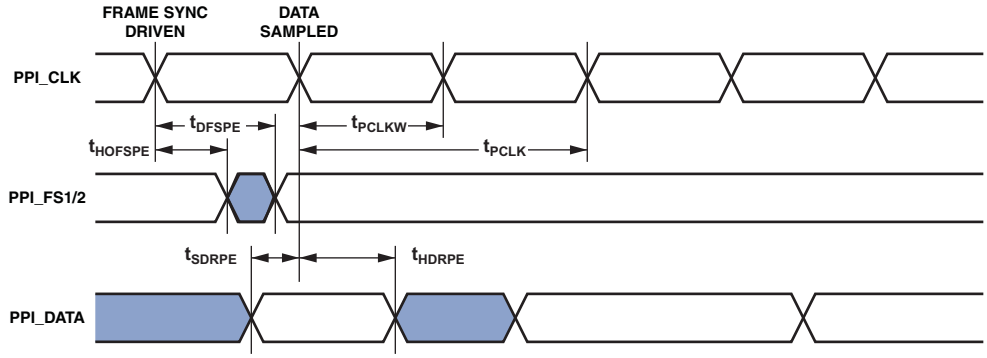

Figure 12. PPI GP Rx Mode with Internal Frame Sync Timing

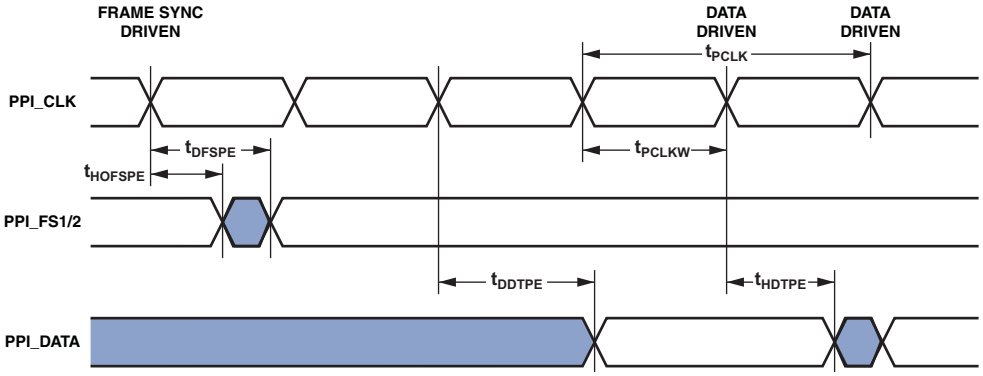

Figure 13. PPI GP Tx Mode with Internal Frame Sync Timing

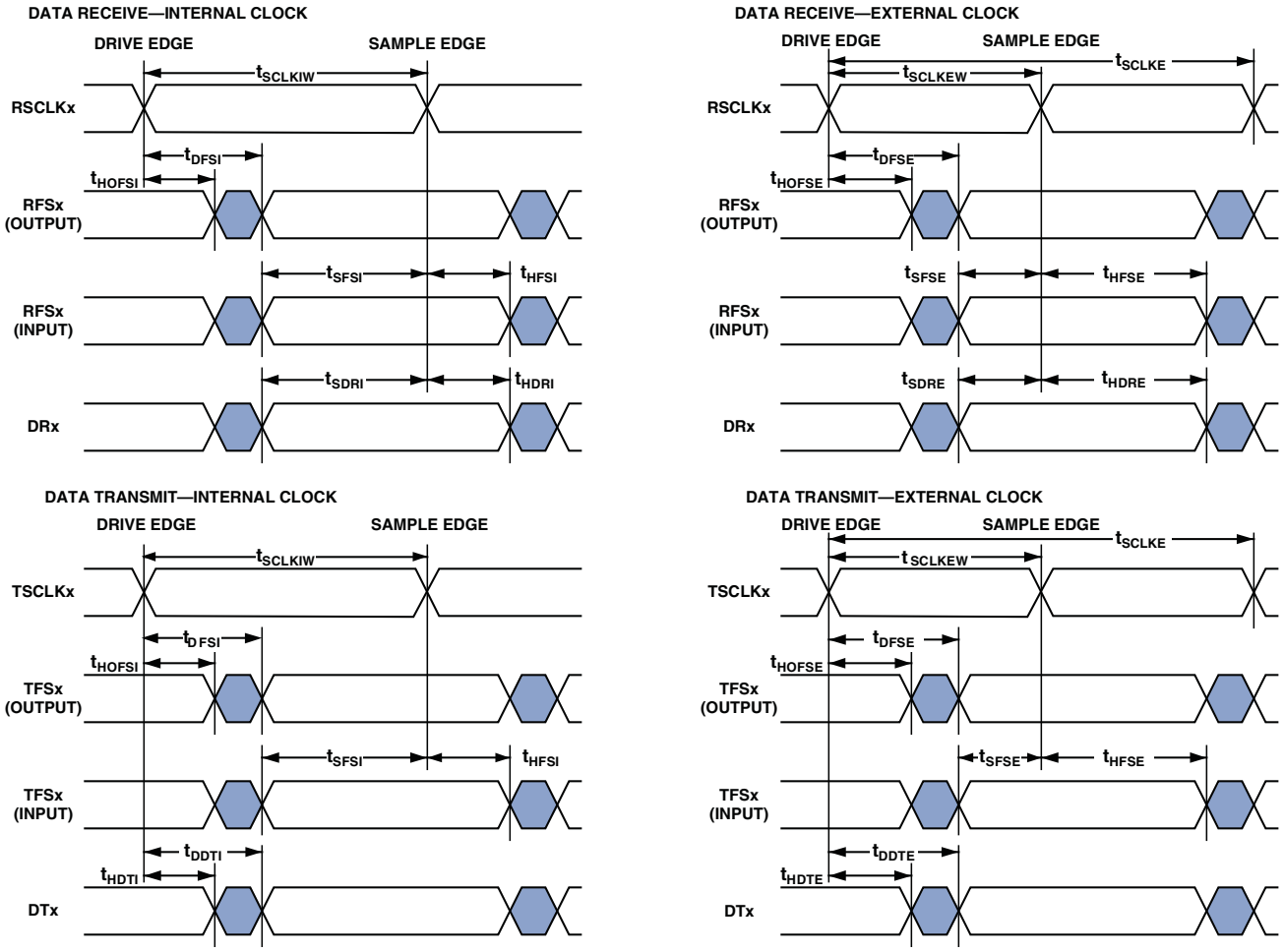

Figure 14. Serial Ports

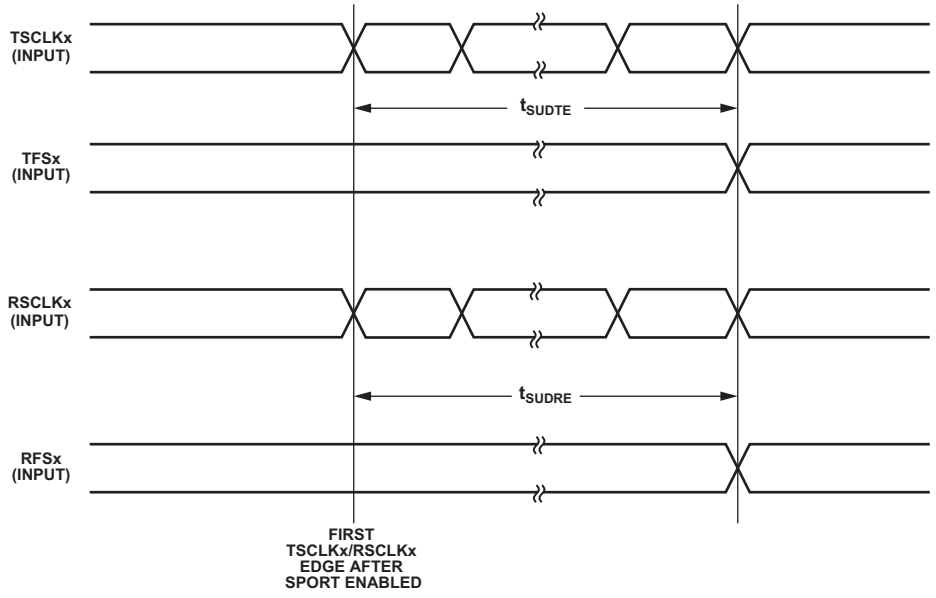

Figure 15. Serial Port Start Up with External Clock and Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 26 and Figure 19 describe SPI port master operations.

Table 26. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		9.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPI\_SELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPI\_SELx}$ High	$2 \times t_{SCLK} - 2$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1		–1		ns

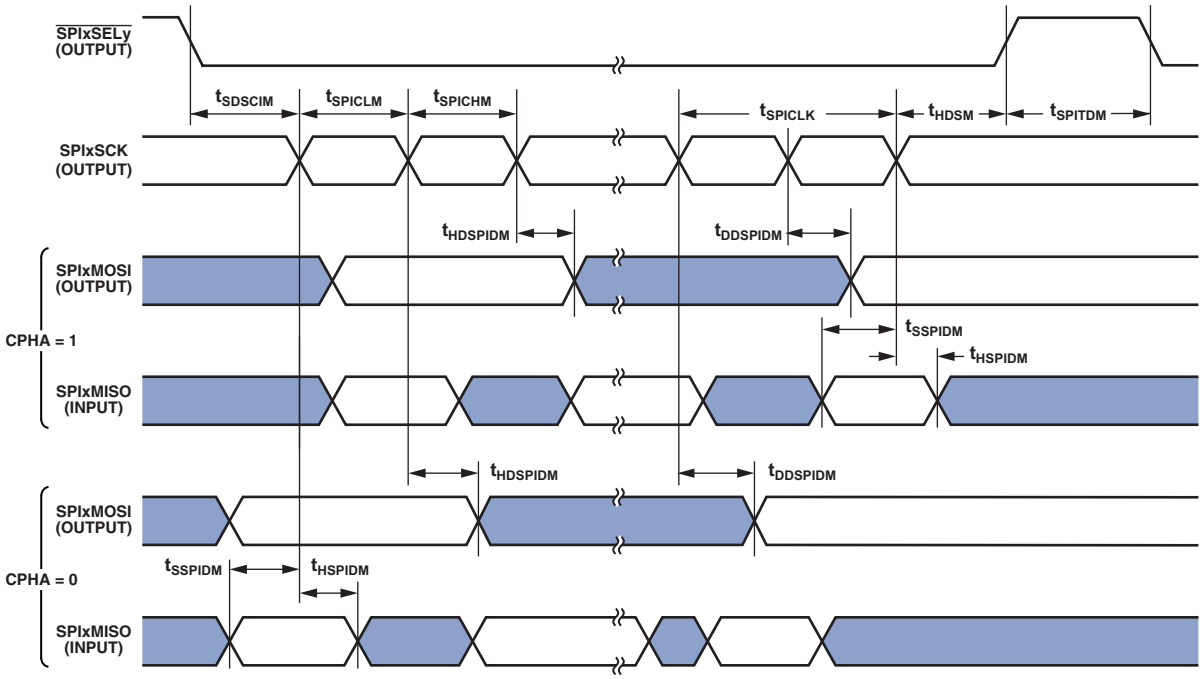

Figure 19. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 27 and Figure 20 describe SPI port slave operations.

Table 27. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPI\_SS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPI\_SS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	2		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPI\_SS}$ Assertion to Data Out Active	0	12	0	10.3	ns
t_{DSDHI}	$\overline{SPI\_SS}$ Deassertion to Data High Impedance	0	11	0	9	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		ns

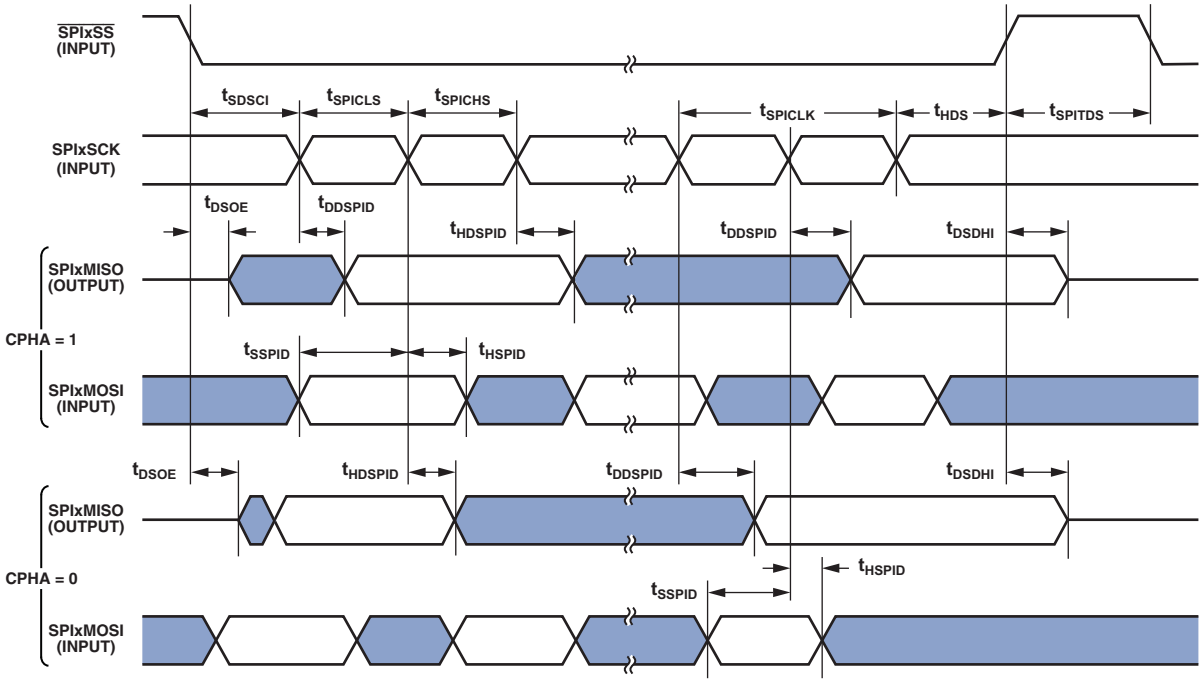

Figure 20. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF59x Hardware Reference Manual*.

General-Purpose Port Timing

Table 28 and Figure 21 describe general-purpose port operations.

Table 28. General-Purpose Port Timing

Parameter		V_{DDEXT} 1.8 V/2.5 V/3.3 V Nominal Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	0	11	ns

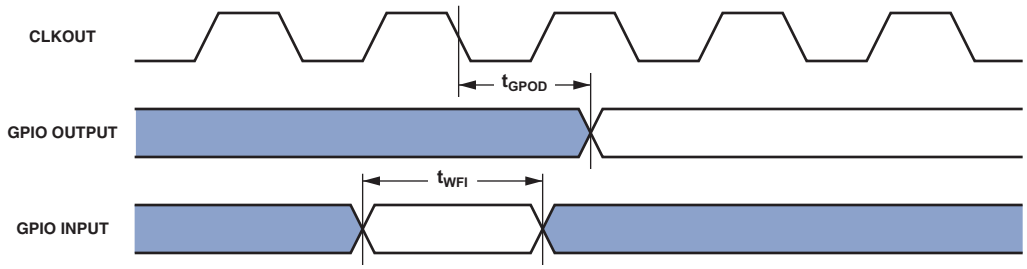

Figure 21. General-Purpose Port Timing

JTAG Test And Emulation Port Timing

Table 31 and Figure 24 describe JTAG port operations.

Table 31. JTAG Port Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		5		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]		13		13	ns

[1] System inputs = SCL, SDA, PF15–0, PG15–0, PH2–0, TCK, $\overline{NMI}$, BMODE3–0, $\overline{PG}$.
[2] 50 MHz maximum.
[3] System outputs = CLKOUT, SCL, SDA, PF15–0, PG15–0, PH2–0, TDO, $\overline{EMU}$, EXT_WAKE.

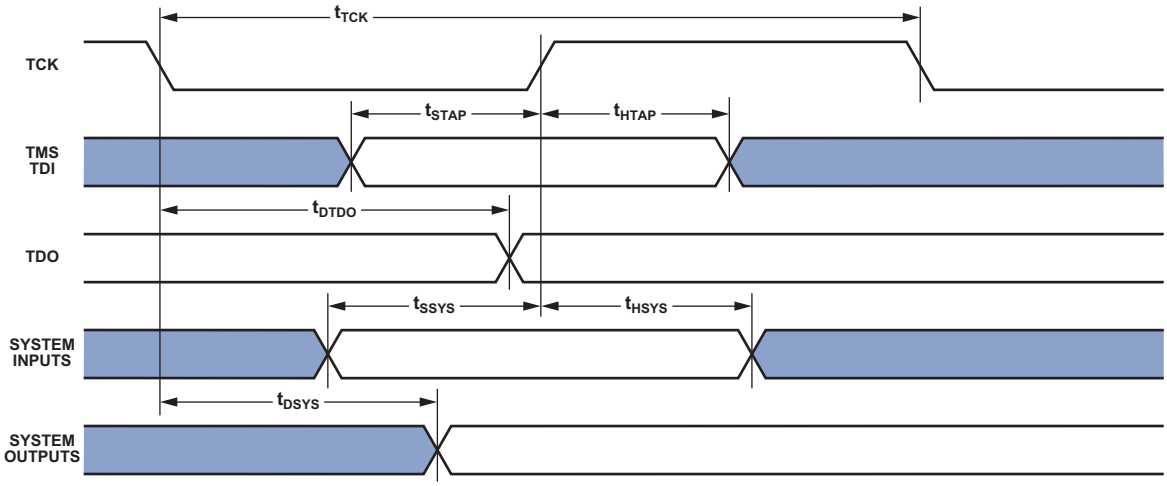

Figure 24. JTAG Port Timing

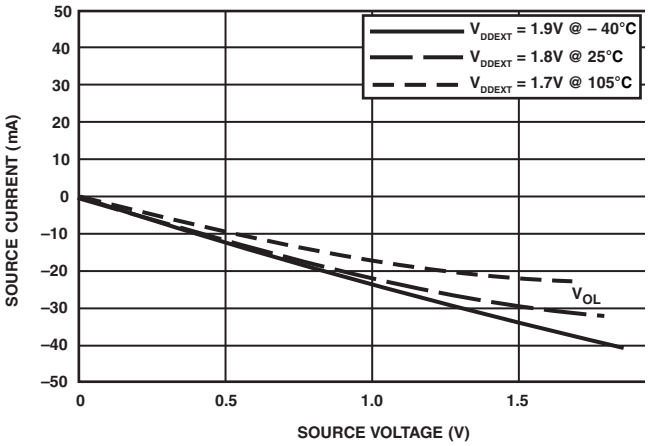

Figure 30. Driver Type B Current (1.8V V_{DDEXT})

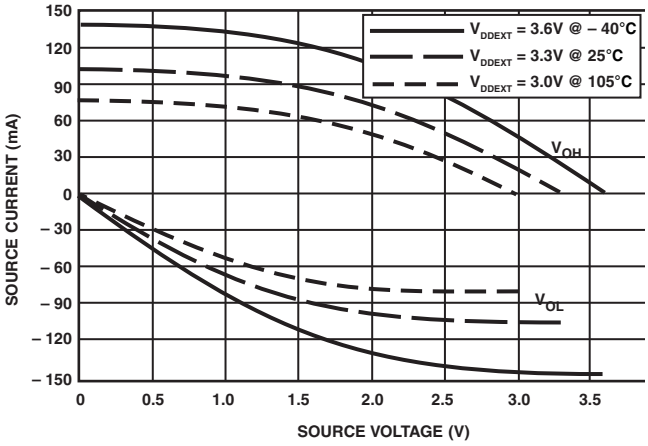

Figure 31. Driver Type C Current (3.3V V_{DDEXT})

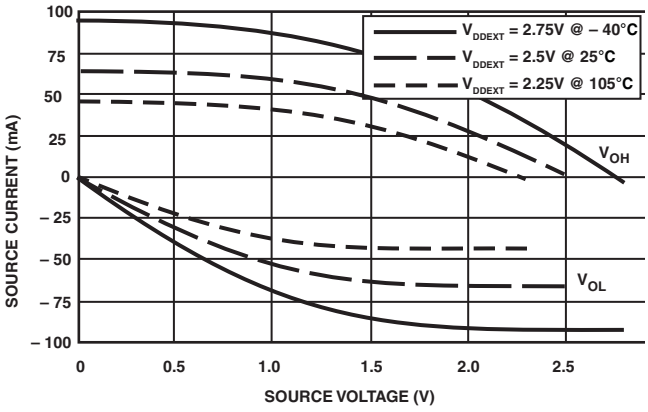

Figure 32. Driver Type C Current (2.5V V_{DDEXT})

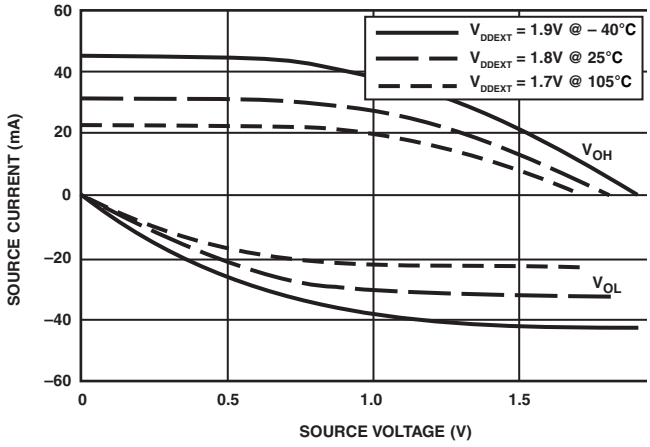

Figure 33. Driver Type C Current (1.8V V_{DDEXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 34 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ for V_{DDEXT} (nominal) = 1.8 V/2.5 V/3.3 V.

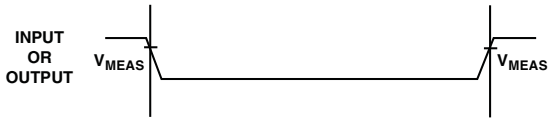

Figure 34. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 35.

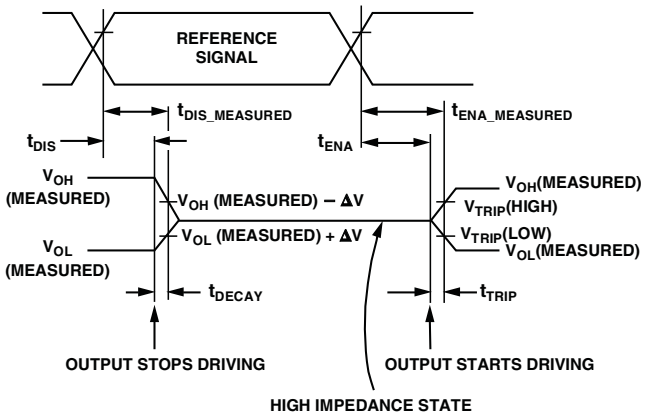

Figure 35. Output Enable/Disable

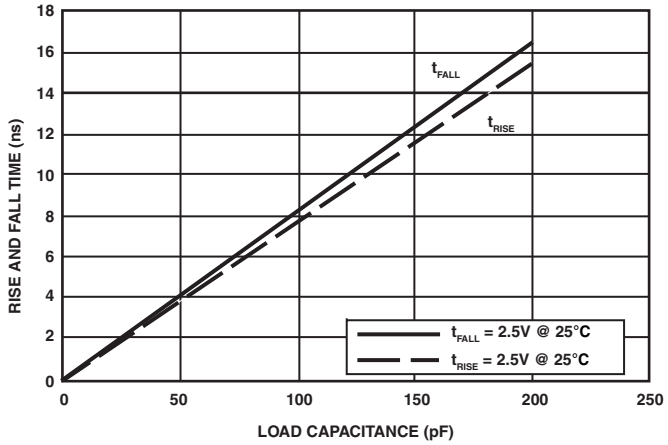

Figure 38. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT})

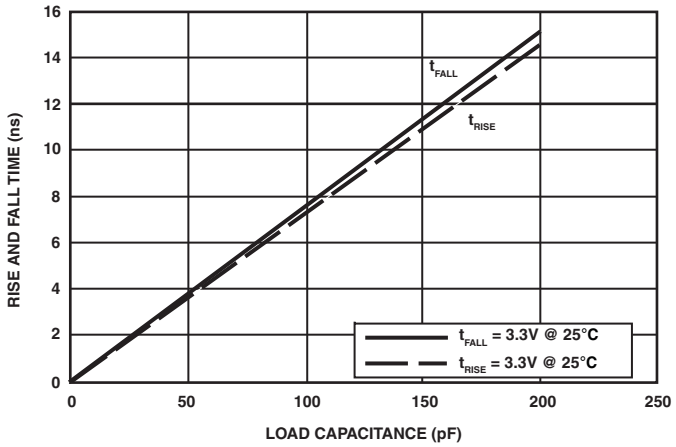

Figure 39. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT})

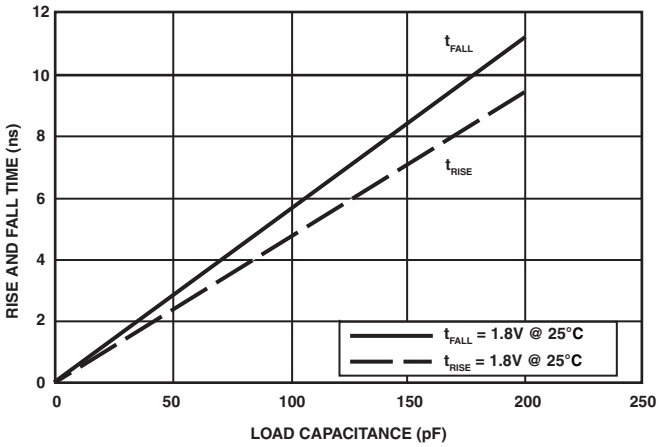

Figure 40. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT})

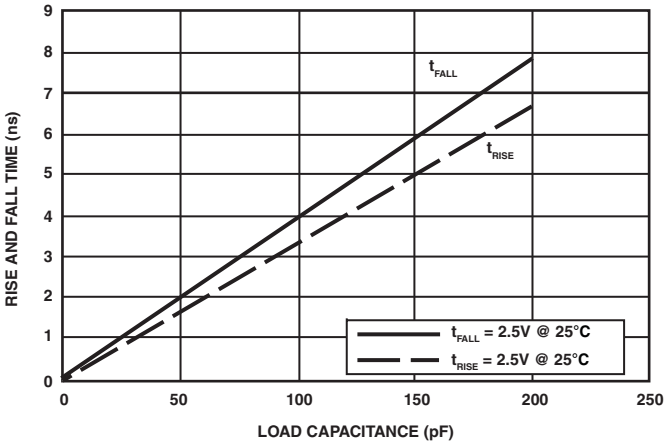

Figure 41. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT})

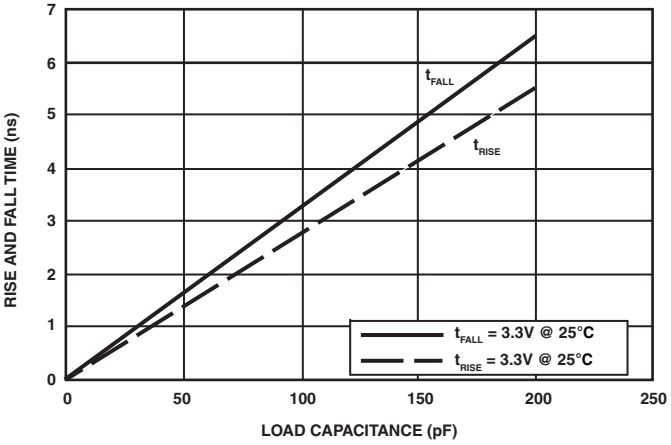

Figure 42. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT})

Figure 43 shows the top view of the LFCSP lead configuration.
Figure 44 shows the bottom view of the LFCSP lead configuration.

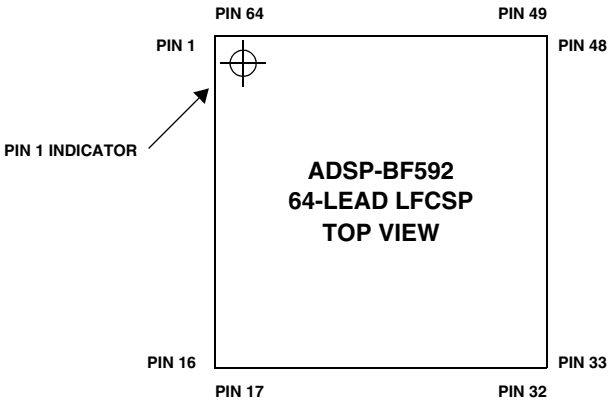

Figure 43. 64-Lead LFCSP Lead Configuration (Top View)

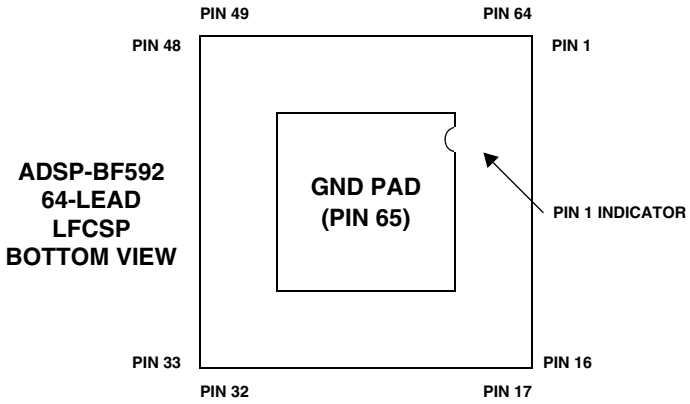

Figure 44. 64-Lead LFCSP Lead Configuration (Bottom View)