What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm002-e-sp

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN19 AN24-AN32 AN48, AN49 AN51-AN56	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 to 4.
OCFA	I	ST	Yes	Compare Fault A input (for compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 to 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD5-RD6, RD8	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send.
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
$\overline{\text{U2CTS}}$	I	ST	Yes	UART2 Clear-to-Send.
$\overline{\text{U2RTS}}$	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
$\overline{\text{SS1}}$	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
PPS = Peripheral Pin Select   TTL = TTL input buffer

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16-bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All V_{DD} and V_{SS} pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AV_{DD} and AV_{SS} pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- V_{CAP}
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (V_{CAP})"**)
- $\overline{MCLR}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

> **Note:** The AV_{DD} and AV_{SS} pins must be connected, regardless of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as V_{DD}, V_{SS}, AV_{DD} and AV_{SS}, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10V-20V is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.

- **Placement on the Printed Circuit Board (PCB):** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.

- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.

- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.

FIGURE 4-11: PAGED DATA MEMORY SPACE
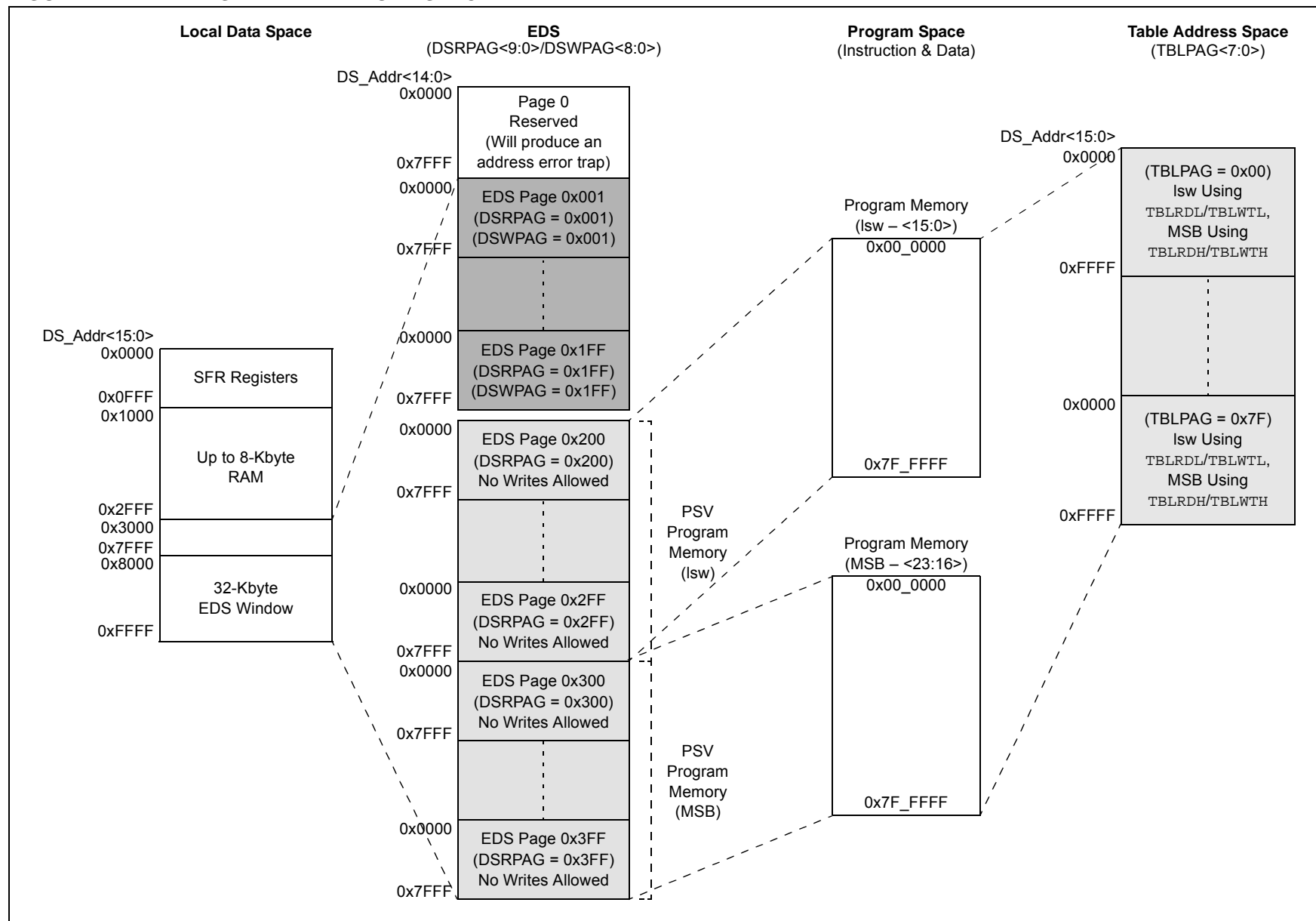
REGISTER 5-5: **NVMSRCADRH: NVM DATA MEMORY UPPER ADDRESS REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7-0   **NVMSRCADRH<23:16>:** Data Memory Upper Address bits

REGISTER 5-6: **NVMSRCADRL: NVM DATA MEMORY LOWER ADDRESS REGISTER**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	r-0
NVMSRCADR<7:1>							—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1   **NVMSRCADRL<15:1>:** Data Memory Lower Address bits

bit 0   **Reserved:** Maintain as '0'

7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EVXXXGM00X/10X CPU. The Interrupt Vector Table (IVT) provides 246 interrupt sources (unused sources are reserved for future use) that can be programmed with different priority levels.

The interrupt controller has the following features:

- Interrupt Vector Table with up to 246 Vectors
- Alternate Interrupt Vector Table (AIVT)
- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Software can Generate any Peripheral Interrupt
- Alternate Interrupt Vector Table (AIVT) is available if Boot Security is Enabled and AIVTEN = 1

7.1 Interrupt Vector Table

The dsPIC33EVXXXGM00X/10X family IVT, shown in Figure 7-2, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 187 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-1, is available if the Boot Segment (BS) is defined, the AIVTEN bit is set in the INTCON2 register and if the AIVTDIS Configuration bit is set to '1'. The AIVT begins at the start of the last page of the Boot Segment.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel or channels are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

• Four DMA Channels
• Register Indirect with Post-Increment Addressing mode
• Register Indirect without Post-Increment Addressing mode

• Peripheral Indirect Addressing mode (peripheral generates destination address)
• CPU Interrupt after Half or Full Block Transfer Complete
• Byte or Word Transfers
• Fixed Priority Channel Arbitration
• Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
• One-Shot or Auto-Repeat Block Transfer modes
• Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer complete)
• DMA Request for Each Channel can be Selected from any Supported Interrupt Source
• Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
External Interrupt 0 (INT0)	00000000	—	—
Input Capture 1 (IC1)	00000001	0x0144 (IC1BUF)	—
Input Capture 2 (IC2)	00000101	0x014C (IC2BUF)	—
Input Capture 3 (IC3)	00100101	0x0154 (IC3BUF)	—
Input Capture 4 (IC4)	00100110	0x015C (IC4BUF)	—
Output Compare 1 (OC1)	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
Output Compare 2 (OC2)	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
Output Compare 3 (OC3)	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
Output Compare 4 (OC4)	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
Timer2 (TMR2)	00000111	—	—
Timer3 (TMR3)	00001000	—	—
Timer4 (TMR4)	00011011	—	—
Timer5 (TMR5)	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1 Receiver (UART1RX)	00001011	0x0226 (U1RXREG)	—
UART1 Transmitter (UART1TX)	00001100	—	0x0224 (U1TXREG)
UART2 Receiver (UART2RX)	00011110	0x0236 (U2RXREG)	—
UART2 Transmitter (UART2TX)	00011111	—	0x0234 (U2TXREG)
RX Data Ready (CAN1)	00100010	0x0440 (C1RXD)	—
TX Data Request (CAN1)	01000110	—	0x0442 (C1TXD)
ADC1 Convert Done (ADC1)	00001101	0x0300 (ADC1BUF0)	—

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0

bit 15   bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0

bit 7   bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8   **IC4R<7:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
                (see Table 11-2 for input pin selection numbers)
                10110101 = Input tied to RPI181
                •
                •
                •
                00000001 = Input tied to CMP1
                00000000 = Input tied to Vss

bit 7-0   **IC3R<7:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
                (see Table 11-2 for input pin selection numbers)
                10110101 = Input tied to RPI181
                •
                •
                •
                00000001 = Input tied to CMP1
                00000000 = Input tied to Vss

NOTES:

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:

    a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.

    b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

    > **Note:** This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using $\overline{SSx}$ from a master):

    a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.

    b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

    > **Note:** This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

    > **Note:** Not all third-party devices support Frame mode timing. For more information, refer to the SPI specifications in **Section 30.0 "Electrical Characteristics"**.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

REGISTER 19-1:   I2CxCON1: I2Cx CONTROL REGISTER 1 (CONTINUED)

bit 7   **GCEN:** General Call Enable bit (I^{2}C Slave mode only)

1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6   **STREN:** SCLx Clock Stretch Enable bit

In I^{2}C Slave mode only, used in conjunction with the SCLREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5   **ACKDT:** Acknowledge Data bit

In I^{2}C Master mode, during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^{2}C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4   **ACKEN:** Acknowledge Sequence Enable bit

In I^{2}C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3   **RCEN:** Receive Enable bit (I^{2}C Master mode only)

1 = Enables Receive mode for I^{2}C, automatically cleared by hardware at the end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2   **PEN:** Stop Condition Enable bit (I^{2}C Master mode only)

1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1   **RSEN:** Restart Condition Enable bit (I^{2}C Master mode only)

1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0   **SEN:** Start Condition Enable bit (I^{2}C Master mode only)

1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1:   Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2:   Automatically cleared to '0' at the beginning of slave transmission.

BUFFER 22-3: **CANx MESSAGE BUFFER WORD 2**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10   **EID<5:0>:** Extended Identifier bits

bit 9   **RTR:** Remote Transmission Request bit

When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.

bit 8   **RB1:** Reserved Bit 1

User must set this bit to '0' per CAN protocol.

bit 7-5   **Unimplemented:** Read as '0'

bit 4   **RB0:** Reserved Bit 0

User must set this bit to '0' per CAN protocol.

bit 3-0   **DLC<3:0>:** Data Length Code bits

BUFFER 22-4: **CANx MESSAGE BUFFER WORD 3**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 1<15:8>				
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 0<7:0>				
bit 7							bit 0

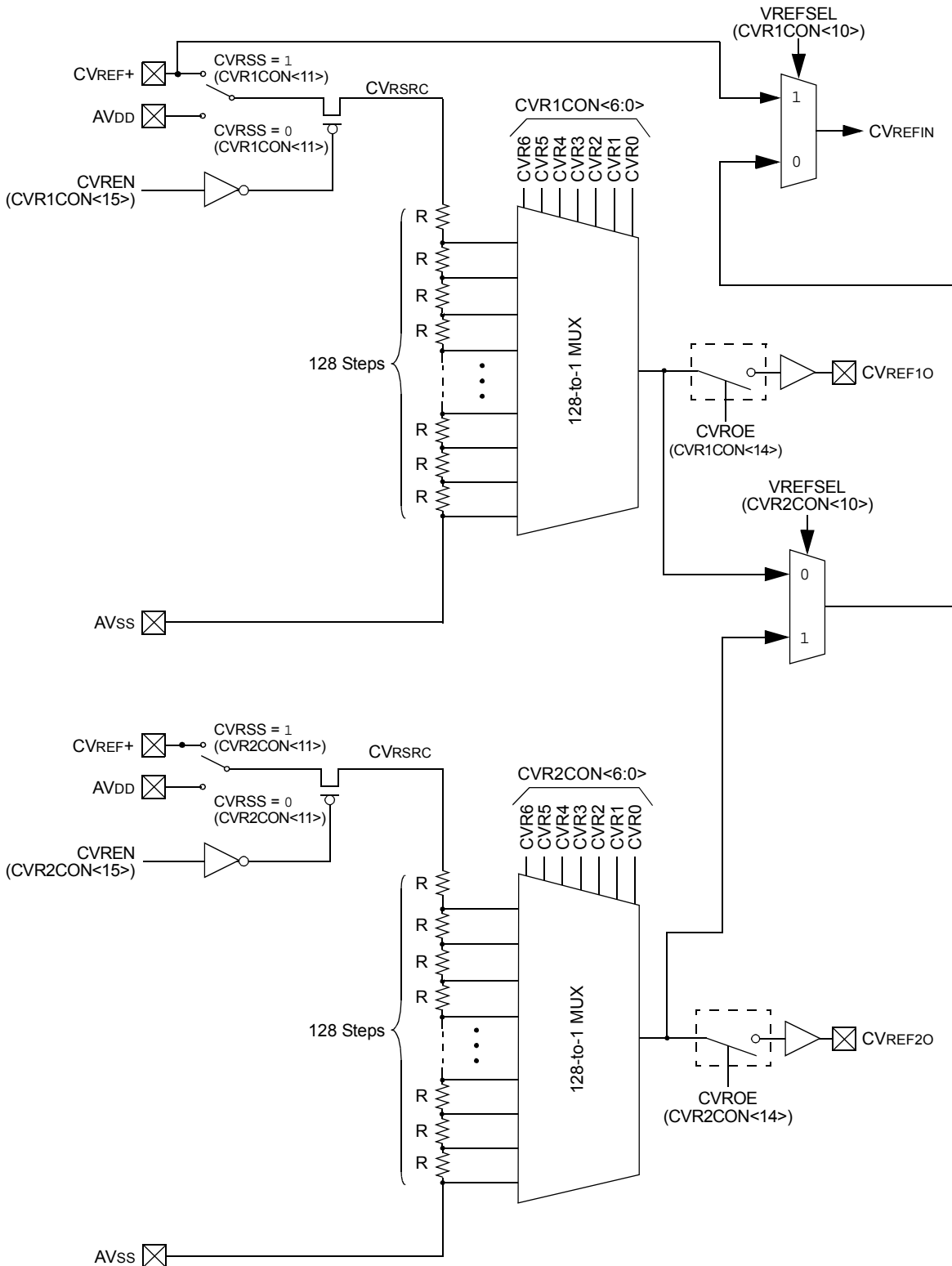| **Legend:**			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Byte 1<15:8>:** CANx Message Byte 1 bits

bit 7-0   **Byte 0<7:0>:** CANx Message Byte 0 bits

FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

Note 1: CVREF2O and CVROE (CVR2CON<14>) is not available on the 28-pin devices.

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TB10	TTxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB11	TTxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB15	TTxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TB20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TC10	TTxH	TxCK High Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTxL	TxCK Low Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTxP	TxCK Input Period	Synchronous, with Prescaler	2 TCY + 40	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TC20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

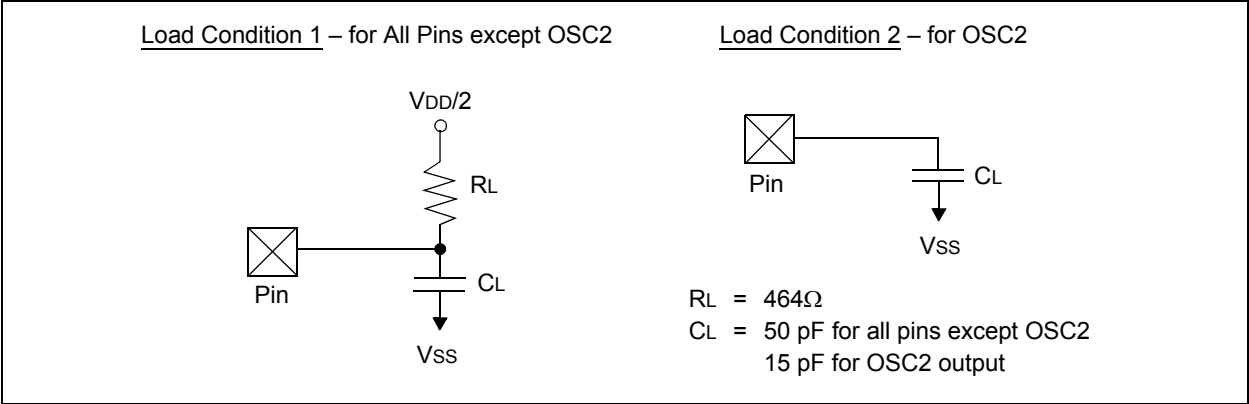**NOTES:**

31.2 AC Characteristics and Timing Parameters

The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature $-40°C \leq T_A \leq +150°C$ Operating voltage V_{DD} range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load Condition 1 – for All Pins except OSC2

Load Condition 2 – for OSC2

$V_{DD}/2$

R_L

Pin

C_L

V_{SS}

Pin

C_L

V_{SS}

R_L = 464Ω
C_L = 50 pF for all pins except OSC2
        15 pF for OSC2 output

32.2   IIDLE

FIGURE 32-7:   **TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 70 MHz, 5.5V MAX)**
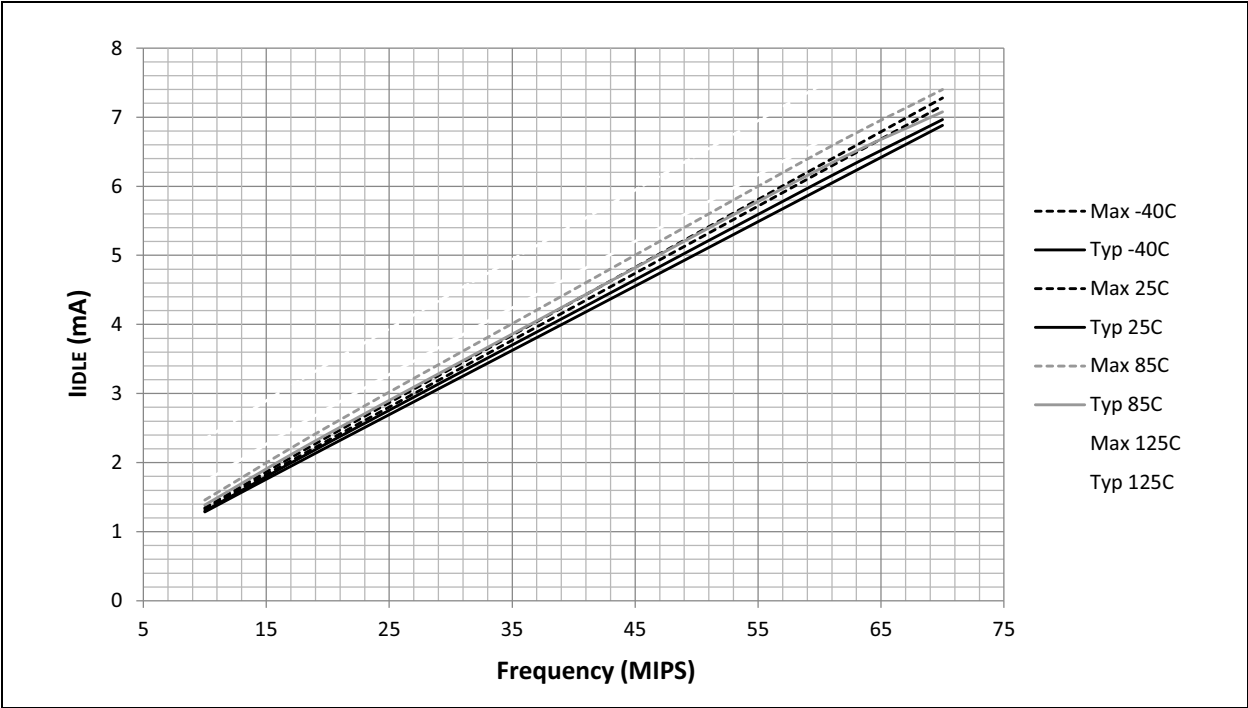
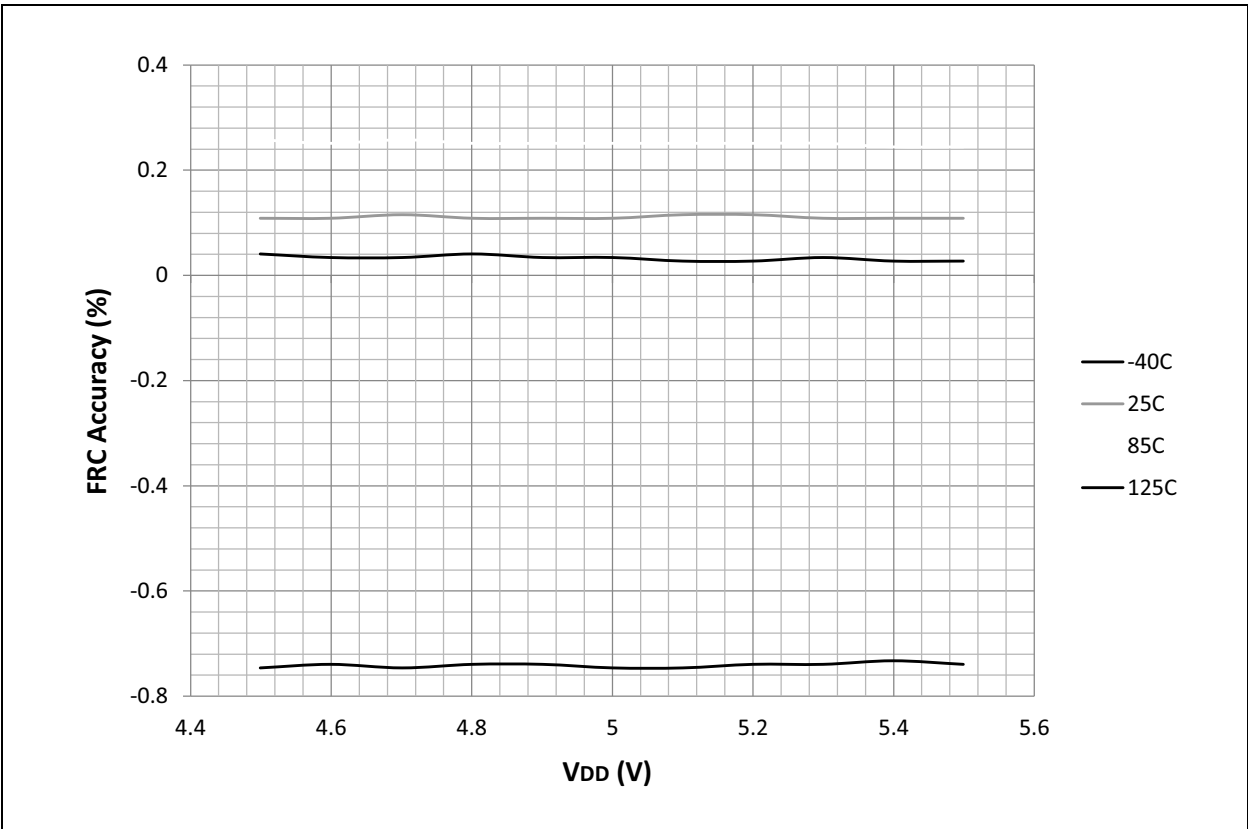**FIGURE 32-8:**   **TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)**
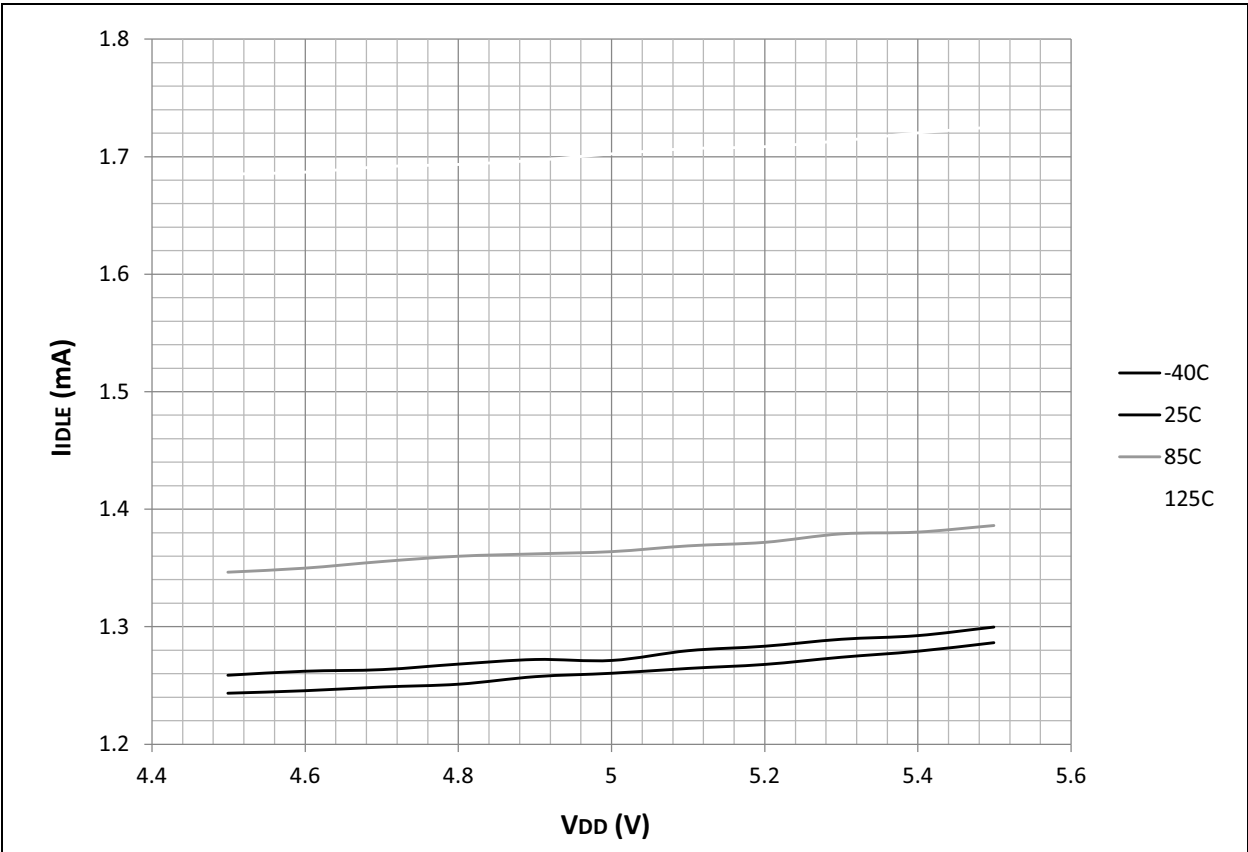
FIGURE 32-19: **TYPICAL/MAXIMUM ΔI$_{WDT}$ vs. TEMPERATURE**
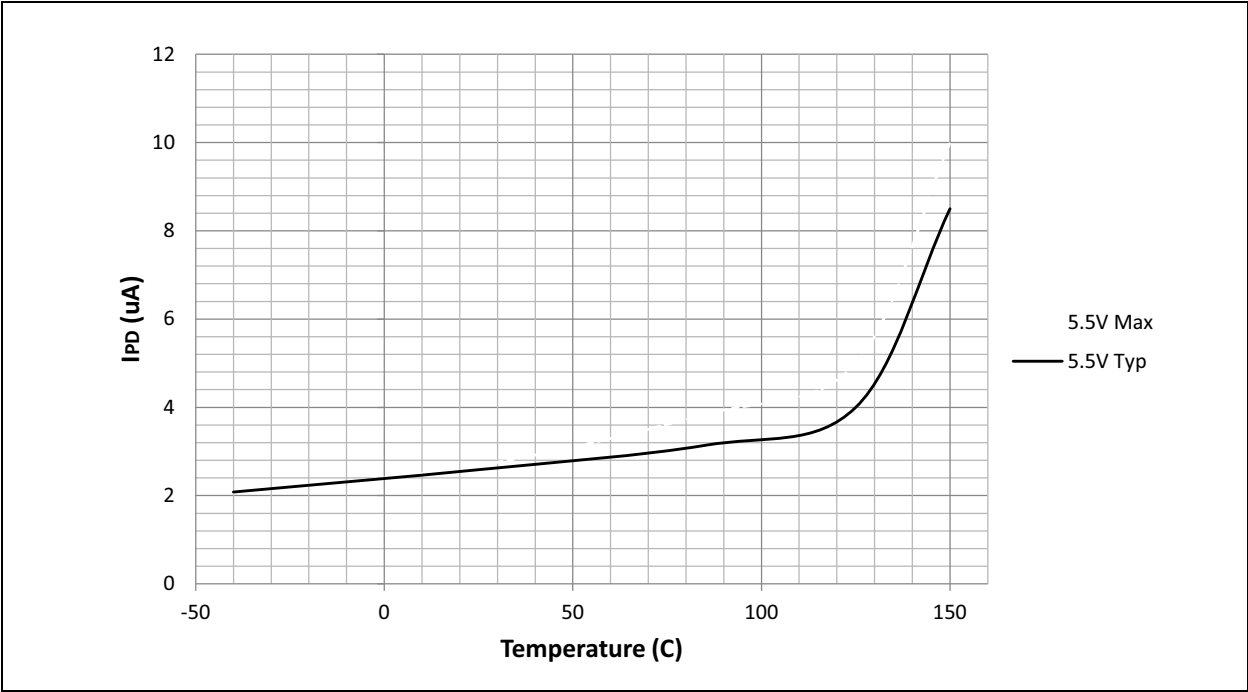
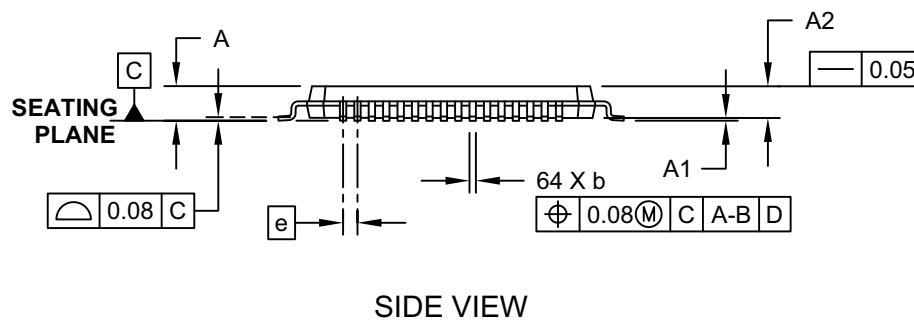## 32.5   FRC

FIGURE 32-20: **TYPICAL FRC ACCURACY vs. V$_{DD}$**

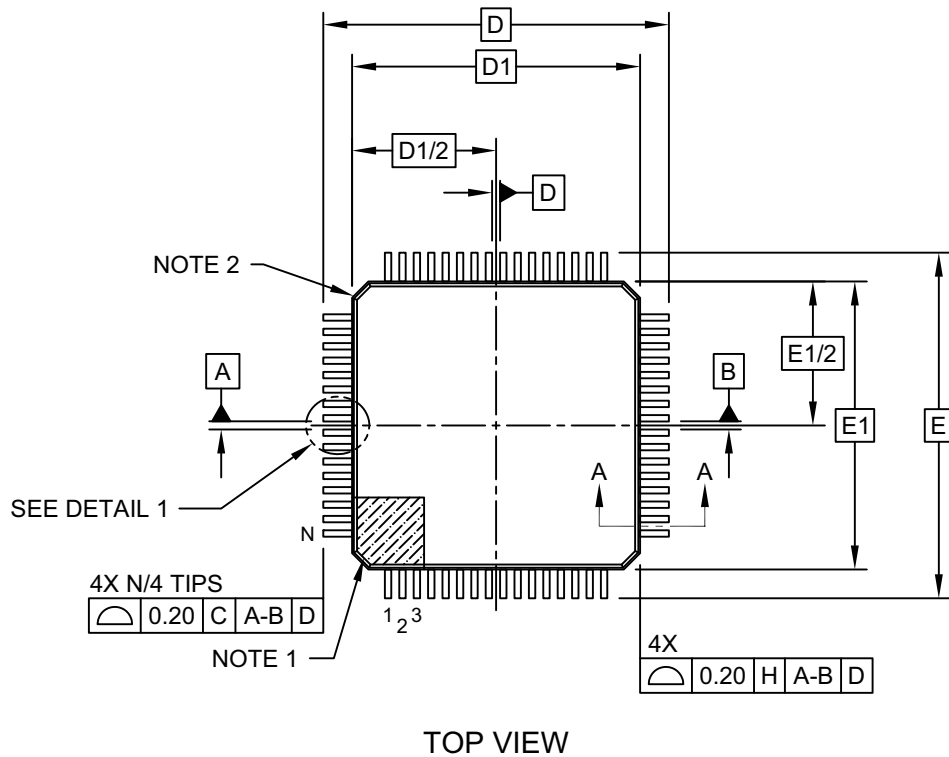**NOTES:**

dsPIC33EVXXXGM00X/10X FAMILY

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

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