What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm004-e-mlvao

dsPIC33EVXXXGM00X/10X FAMILY

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3.5 Programmer's Model

The programmer's model for the dsPIC33EVXXXGM00X/10X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EVXXXGM00X/10X family devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15[1]	Working Register Array
W0 through W14[1]	Alternate Working Register Array 1
W0 through W14[1]	Alternate Working Register Array 2
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Count Register
DOSTARTH[2], DOSTARTL[2]	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represents the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-2: TIMERS REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																0000
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (For 32-bit operations only)																0000
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	—	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	—	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E14	TRISB<15:0>																FFFF
PORTB	0E16	RB<15:0>																xxxx
LATB	0E18	LATB<15:0>																xxxx
ODCB	0E1A	ODCB<15:0>																0000
CNENB	0E1C	CNIEB<15:0>																0000
CNPUB	0E1E	CNPUB<15:0>																0000
CNPDB	0E20	CNPDB<15:0>																0000
ANSELB	0E22	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				038F
SR1B	0E24	—	—	—	—	—	—	SR1B<9:7>			—	—	SR1B4	—	—	—	—	0000
SR0B	0E26	—	—	—	—	—	—	SR0B<9:7>			—	—	SR0B4	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

4.7.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through the Data Space. The `TBLRDH` and `TBLWTH` instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. The `TBLRDL` and `TBLWTL` instructions access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

• `TBLRDL` (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>).
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

• `TBLRDH` (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address, as in the `TBLRDL` instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

Similarly, two table instructions, `TBLWTH` and `TBLWTL`, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space. Accessing the program memory with table instructions is shown in Figure 4-18.

FIGURE 4-18: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

dsPIC33EVXXXGM00X/10X FAMILY
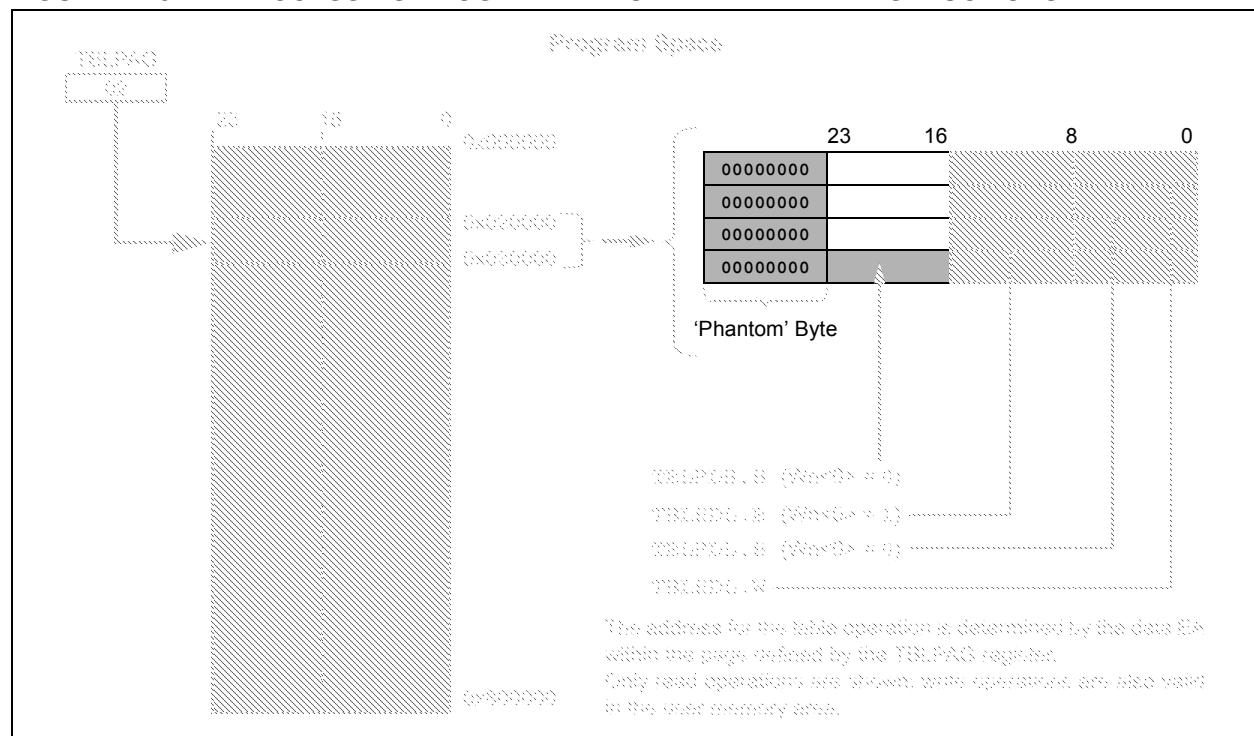
7.3 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EVXXXGM00X/10X family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

> **Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

7.4 Interrupt Control and Status Registers

dsPIC33EVXXXGM00X/10X family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- IFSx
- IECx
- IPCx
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from the INTCON1, INTCON2, INTCON3 and INTCON4 registers.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMT (Deadman Timer), DMA and DO stack overflow status trap sources.

The INTCON4 register contains the ECC Double-Bit Error (ECCDBE) and Software-Generated Hard Trap (SGHT) status bit.

7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared through software.

7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into Vector Number (VECNUM<7:0>) and Interrupt Priority Level bit (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 to Register 7-7.

Table 9-1 provides the Configuration bits which allow users to choose between the various clock modes.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>
Fast RC Oscillator with Divide-by-N (FRCDIVN)[1,2]	Internal	xx	111
Fast RC Oscillator with Divide-by-16 (FRCDIV16)[1]	Internal	xx	110
Low-Power RC Oscillator (LPRC)[1]	Internal	xx	101
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011
Primary Oscillator (EC) with PLL (ECPLL)[1]	Primary	00	011
Primary Oscillator (HS)	Primary	10	010
Primary Oscillator (XT)	Primary	01	010
Primary Oscillator (EC)[1]	Primary	00	010
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)[1]	Internal	xx	001
Fast RC Oscillator (FRC)[1]	Internal	xx	000

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.
2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **IC4R<7:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **IC3R<7:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-11: **RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SS2R<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **SS2R<7:0>:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-12: **RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1RXR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **C1RXR<7:0>:** Assign CAN1 RX Input (C1RX) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

13.0 TIMER2/3 AND TIMER4/5

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

• Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
• Single 32-Bit Timer
• Single 32-Bit Synchronous Counter

They also support these features:

• Timer Gate Operation
• Selectable Prescaler Settings
• Timer Operation during Idle and Sleep modes
• Interrupt on a 32-Bit Period Register Match
• Time Base for Input Capture and Output Compare Modules
• ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

> **Note:** For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

> **Note:** Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

16.0 OUTPUT COMPARE

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Output Compare"** (DS70005157) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
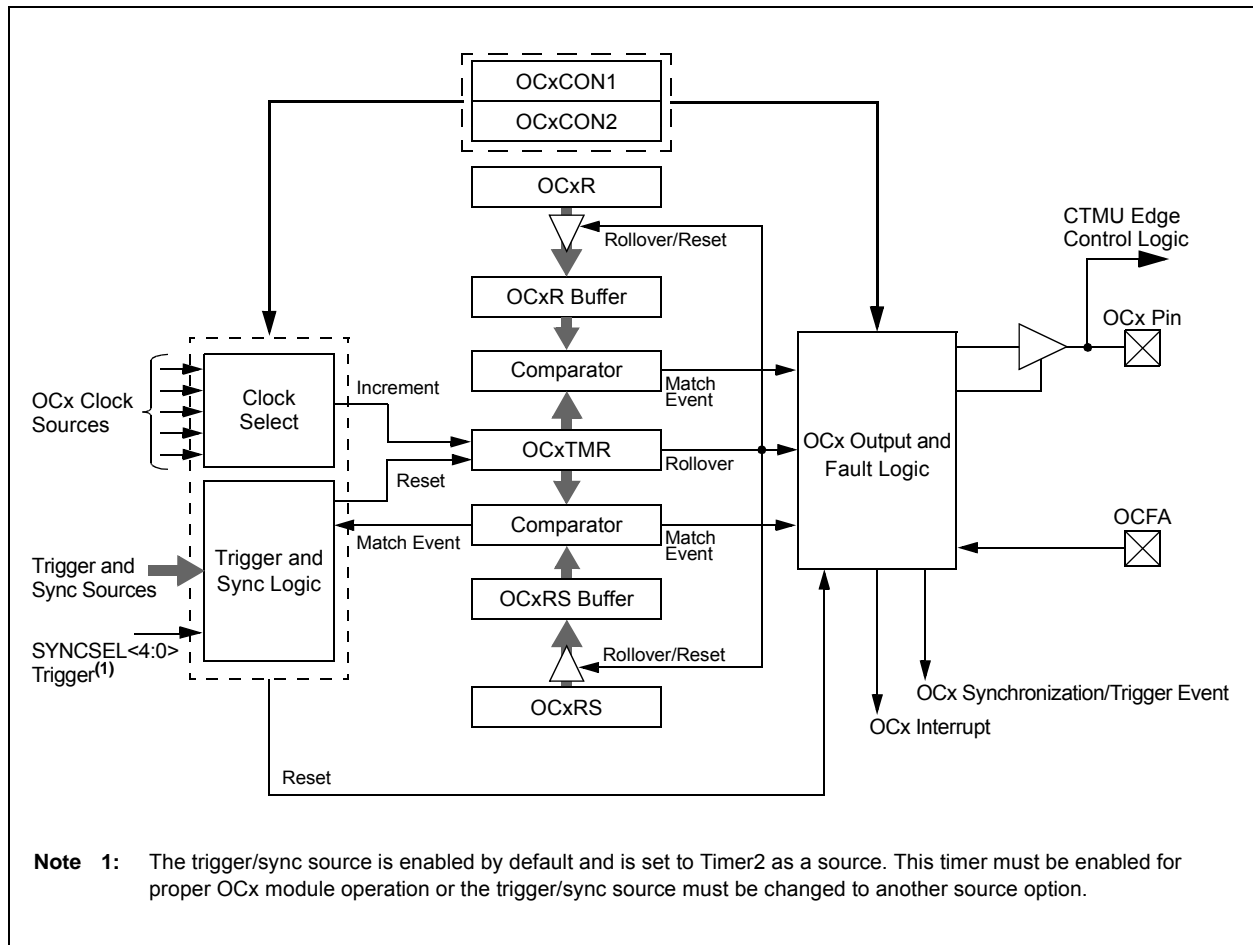
The dsPIC33EVXXXGM00X/10X family devices support up to 4 output compare modules. The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Figure 16-1 shows a block diagram of the output compare module.

> **Note:** For more information on OCxR and OCxRS register restrictions, refer to the **"Output Compare"** (DS70005157) section in the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 16-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM

Note 1: The trigger/sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the trigger/sync source must be changed to another source option.

NOTES:

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	Typ.(2)	Max.	Units	Conditions			
Operating Current (IDD)(1)							
DC20d	4.5	5.5	mA	-40°C		5.0V	10 MIPS
DC20a	4.65	5.6	mA	+25°C			
DC20b	4.85	6.0	mA	+85°C			
DC20c	5.6	7.2	mA	+125°C			
DC22d	8.6	10.6	mA	-40°C		5.0V	20 MIPS
DC22a	8.8	10.8	mA	+25°C			
DC22b	9.1	11.1	mA	+85°C			
DC22c	9.8	12.6	mA	+125°C			
DC23d	16.8	18.5	mA	-40°C		5.0V	40 MIPS
DC23a	17.2	19.0	mA	+25°C			
DC23b	17.55	19.2	mA	+85°C			
DC23c	18.3	21.0	mA	+125°C			
DC24d	25.15	28.0	mA	-40°C		5.0V	60 MIPS
DC24a	25.5	28.0	mA	+25°C			
DC24b	25.5	28.0	mA	+85°C			
DC24c	25.55	28.5	mA	+125°C			
DC25d	29.0	31.0	mA	-40°C		5.0V	70 MIPS
DC25a	28.5	31.0	mA	+25°C			
DC25b	28.3	31.0	mA	+85°C			

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing
  ```
  while(1)
  {
  NOP();
  }
  ```

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

| DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +125°C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.[1]	Max.	Units	Conditions
		Program Flash Memory					
D130	E_P	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	V_{PR}	V_{DD} for Read	4.5	—	5.5	V	
D132b	V_{PEW}	V_{DD} for Self-Timed Write	4.5	—	5.5	V	
D134	T_{RETD}	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	I_{DDP}	Supply Current During Programming	—	10	—	mA	
D136a	T_{RW}	Row Write Cycle Time	0.657	—	0.691	ms	T_{RW} = 4965 FRC cycles, T_A = +85°C (see **Note 2**)
D136b	T_{RW}	Row Write Cycle Time	0.651	—	0.698	ms	T_{RW} = 4965 FRC cycles, T_A = +125°C (see **Note 2**)
D137a	T_{PE}	Page Erase Time	19.44	—	20.44	ms	T_{PE} = 146893 FRC cycles, T_A = +85°C (see **Note 2**)
D137b	T_{PE}	Page Erase Time	19.24	—	20.65	ms	T_{PE} = 146893 FRC cycles, T_A = +125°C (see **Note 2**)
D138a	T_{WW}	Word Write Cycle Time	45.78	—	48.15	µs	T_{WW} = 346 FRC cycles, T_A = +85°C (see **Note 2**)
D138b	T_{WW}	Word Write Cycle Time	45.33	—	48.64	µs	T_{WW} = 346 FRC cycles, T_A = +125°C (see **Note 2**)

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

    2: Other conditions: FRC = 7.3728 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 30-20) and the value of the FRC Oscillator Tuning register.

TABLE 30-14: ELECTRICAL CHARACTERISTICS: INTERNAL BAND GAP REFERENCE VOLTAGE

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +125°C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DVR10	V_{BG}	Internal Band Gap Reference Voltage	1.14	1.2	1.26	V	

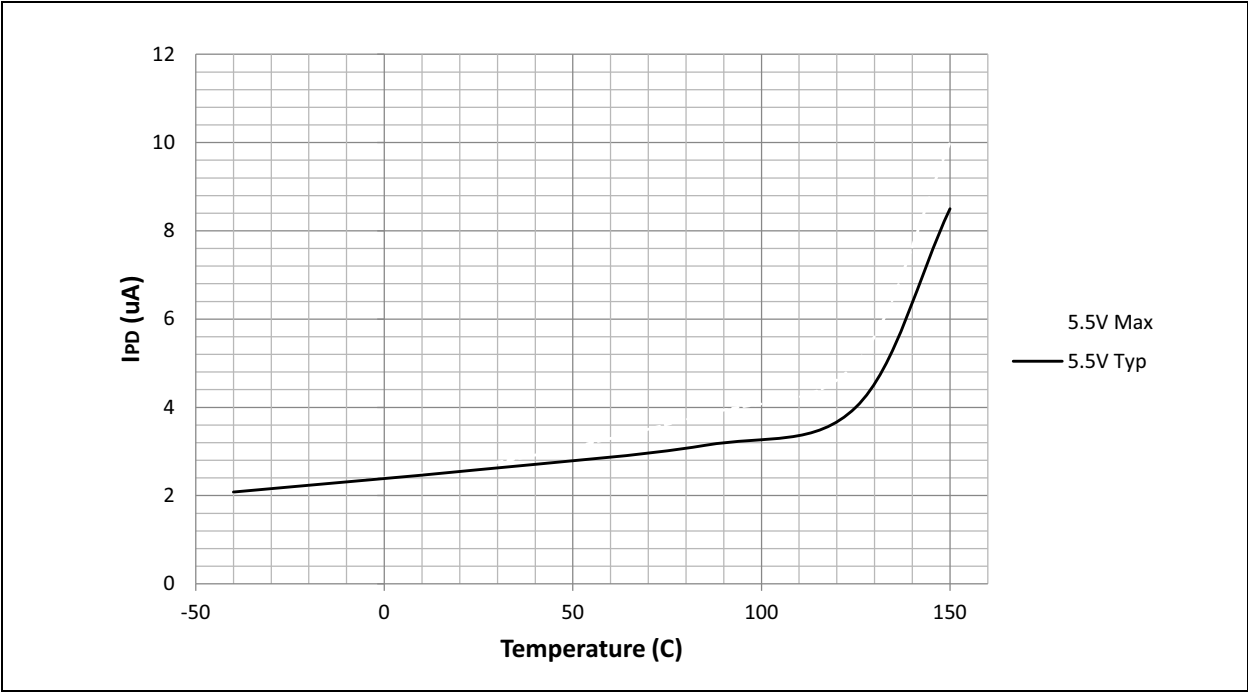**FIGURE 30-27:** **SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**
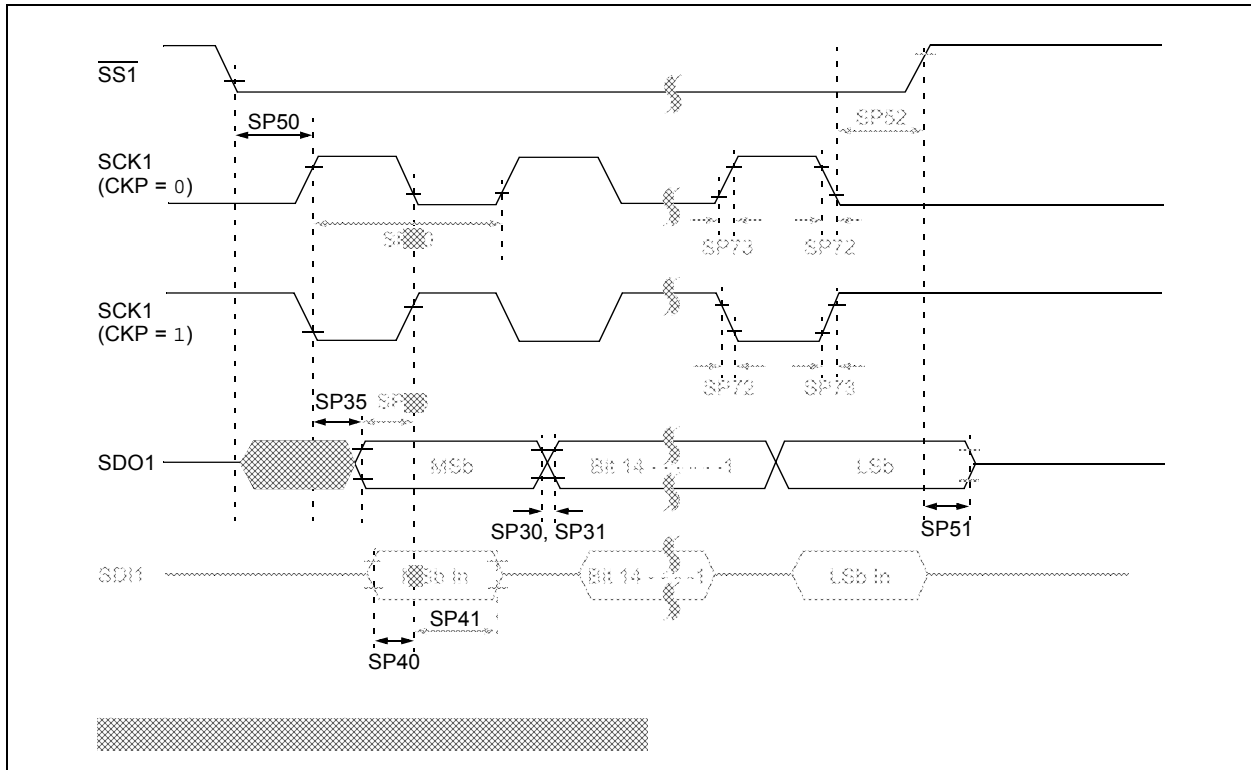
NOTES:

FIGURE 32-19: **TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE**

32.5 FRC

FIGURE 32-20: **TYPICAL FRC ACCURACY vs. VDD**
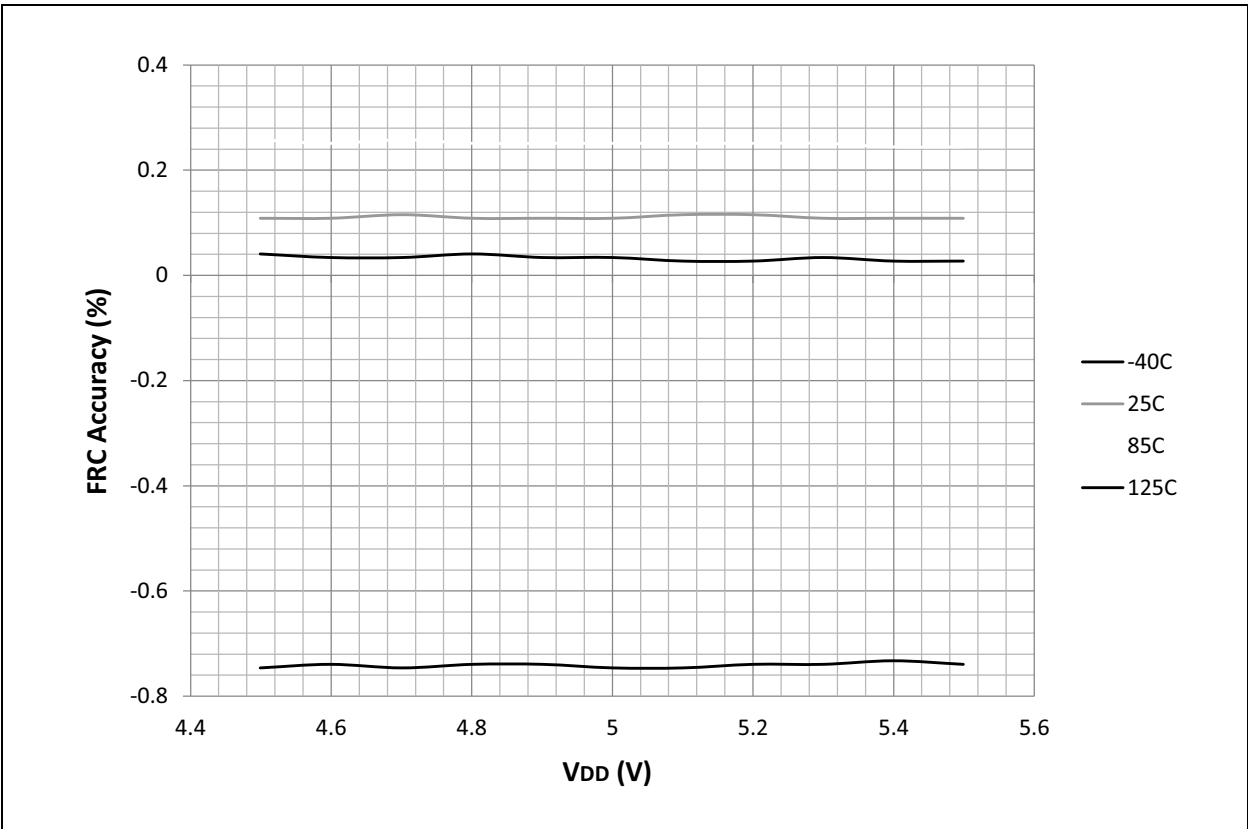
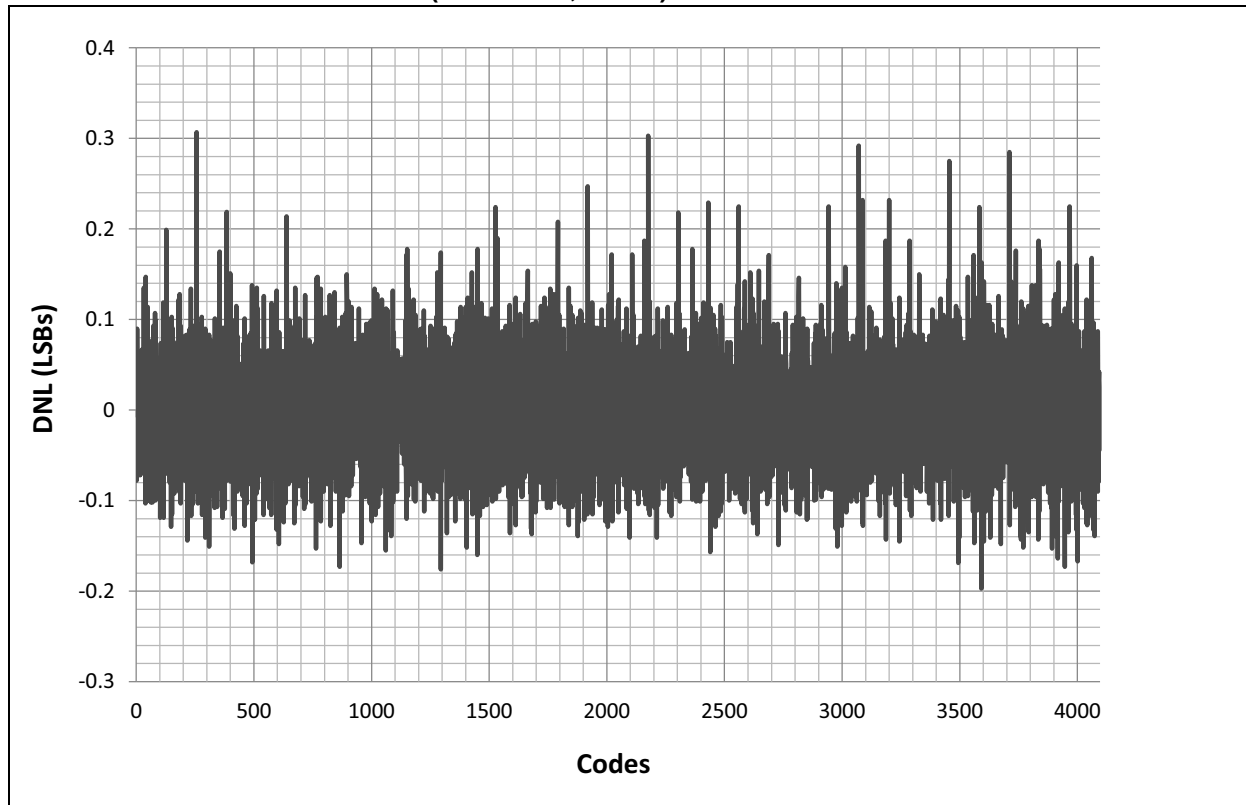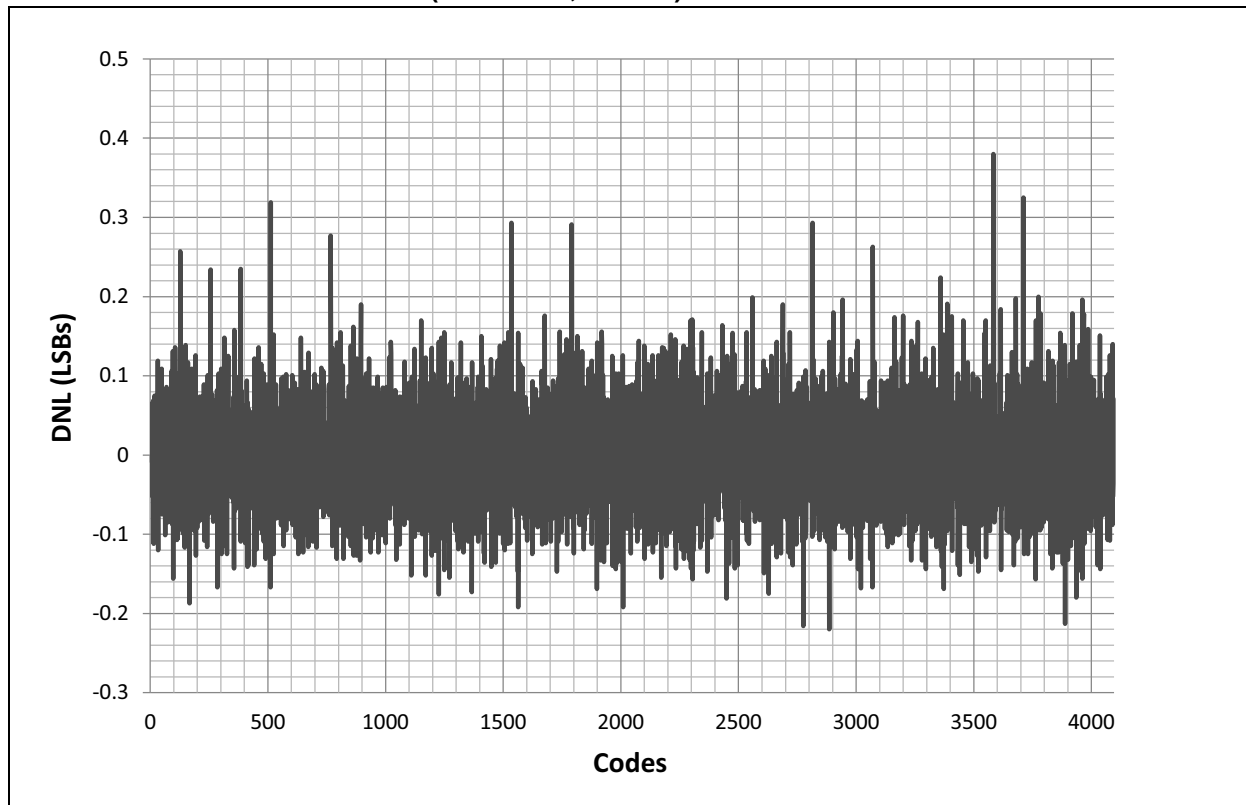**FIGURE 32-43:** TYPICAL DNL (V$_{DD}$ = 5.5V, +85°C)

FIGURE 32-44: TYPICAL DNL (V$_{DD}$ = 5.5V, +125°C)

33.14 Comparator Op Amp Offset
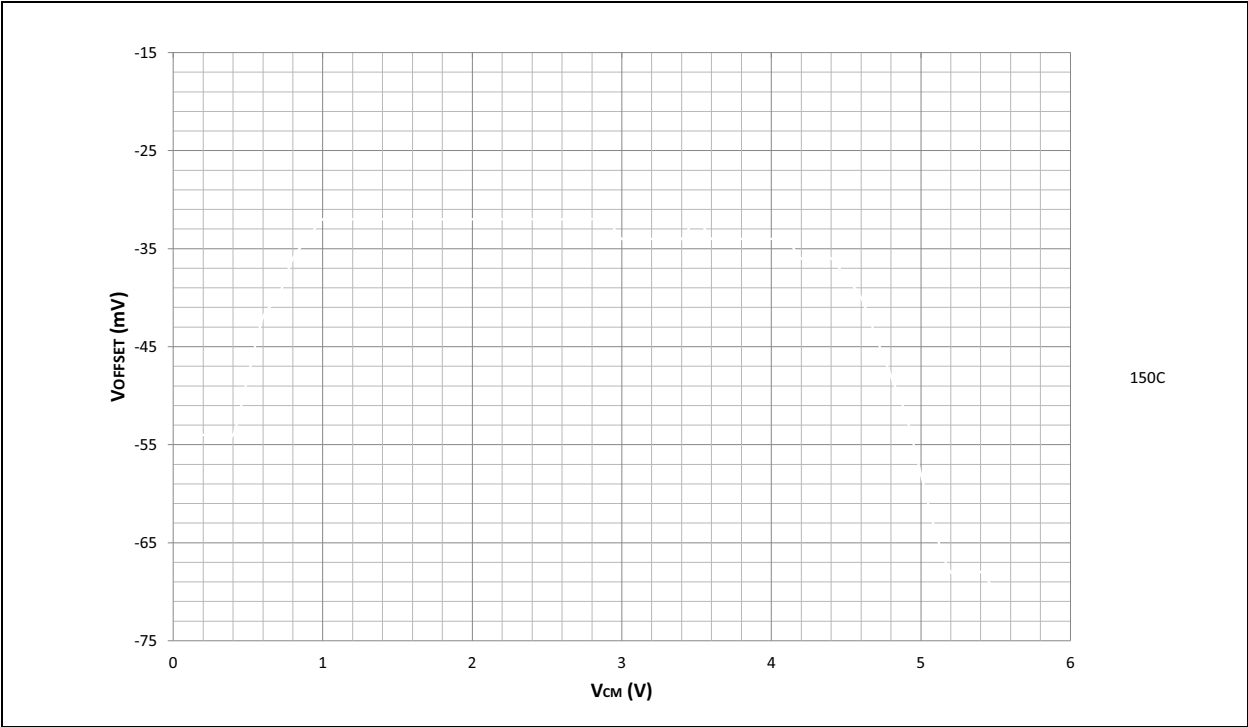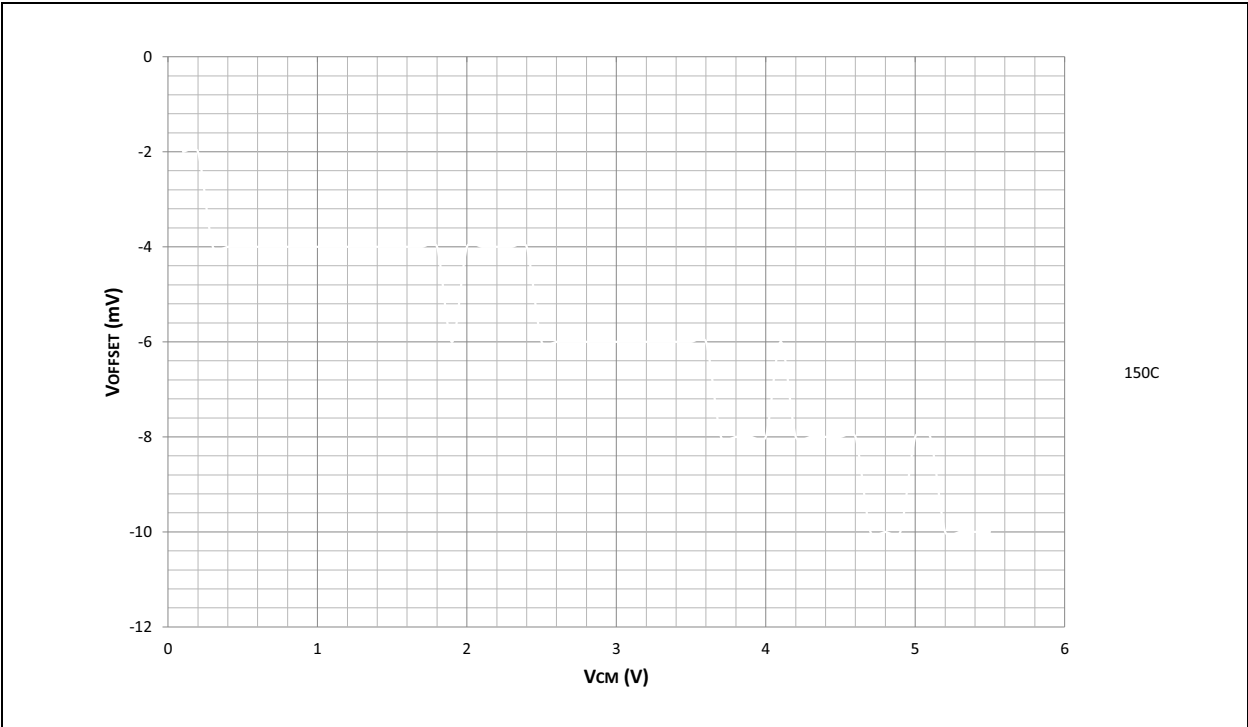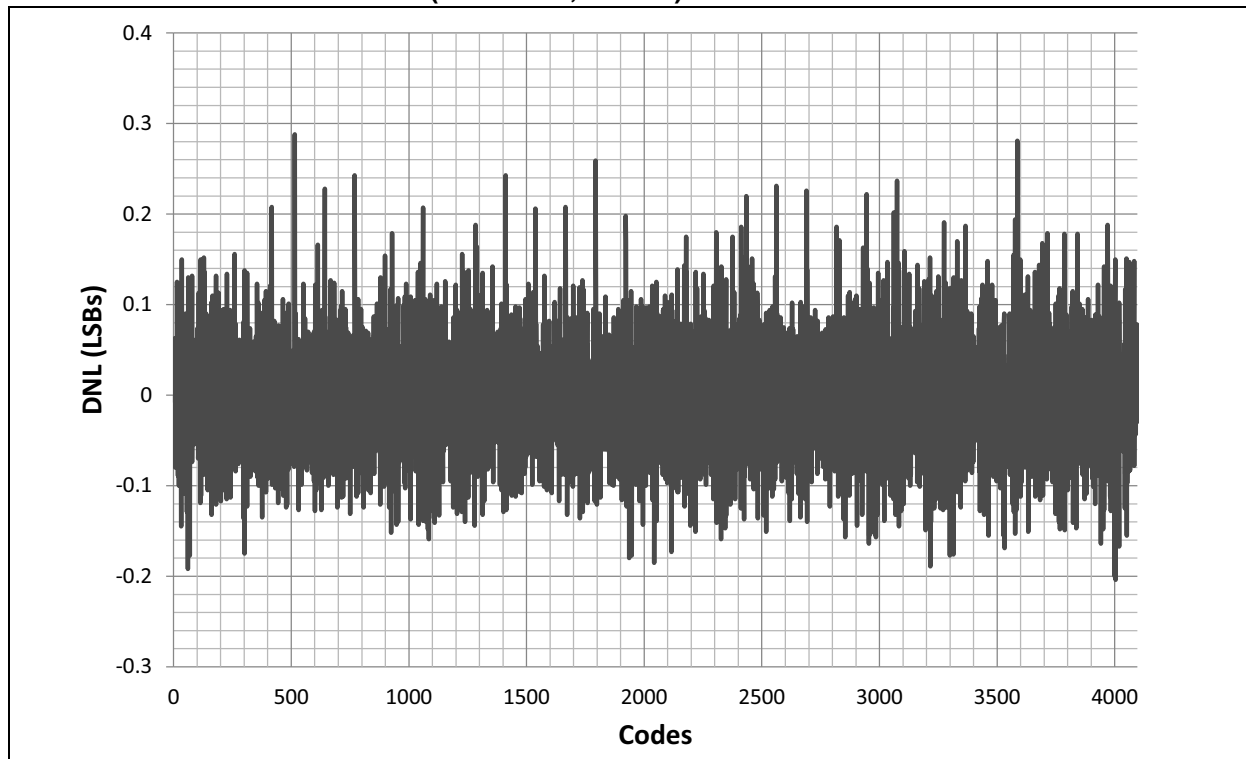
FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. V$_{CM}$

FIGURE 33-34: TYPICAL OP AMP OFFSET vs. V$_{CM}$

33.17 ADC DNL

FIGURE 33-37: TYPICAL DNL (V_DD = 5.5V, +150°C)

33.18 ADC INL

FIGURE 33-38: TYPICAL INL (V_DD = 5.5V, +150°C)