## Details

| | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm004-i-pt |

**FIGURE 4-2:** **PROGRAM MEMORY MAP FOR dsPIC33EV64GM00X/10X DEVICES[1]**



| | Address |
|---|---|
| GOTO Instruction | 0x000000 |
| Reset Address | 0x000002 |
| Interrupt Vector Table | 0x000004 / 0x0001FE |
| User Program Flash Memory (21696 instructions) | 0x000200 ... 0x00AB7E |
| Device Configuration | 0x00AB80 ... 0x00ABFE |
| Unimplemented (Read '0's) | 0x00AC00 ... 0x7FFFFE |
| Executive Code Memory | 0x800000 ... 0x800BFE |
| Reserved | 0x800C00 ... 0x800F80 |
| User OTP Memory | 0x800FFE |
| Reserved | 0x801000 ... 0xF9FFFE |
| Write Latches | 0xFA0000 / 0xFA0002 |
| Reserved | 0xFA0004 ... 0xFEFFFE |
| DEVID | 0xFF0000 / 0xFF0002 |
| Reserved | 0xFF0004 ... 0xFFFFFE |

User Memory Space / Configuration Memory Space

**Note 1:** Memory areas are not shown to scale.

**FIGURE 4-8:** **DATA MEMORY MAP FOR 256-Kbyte DEVICES[1]**



**Note 1:** Memory areas are not shown to scale.
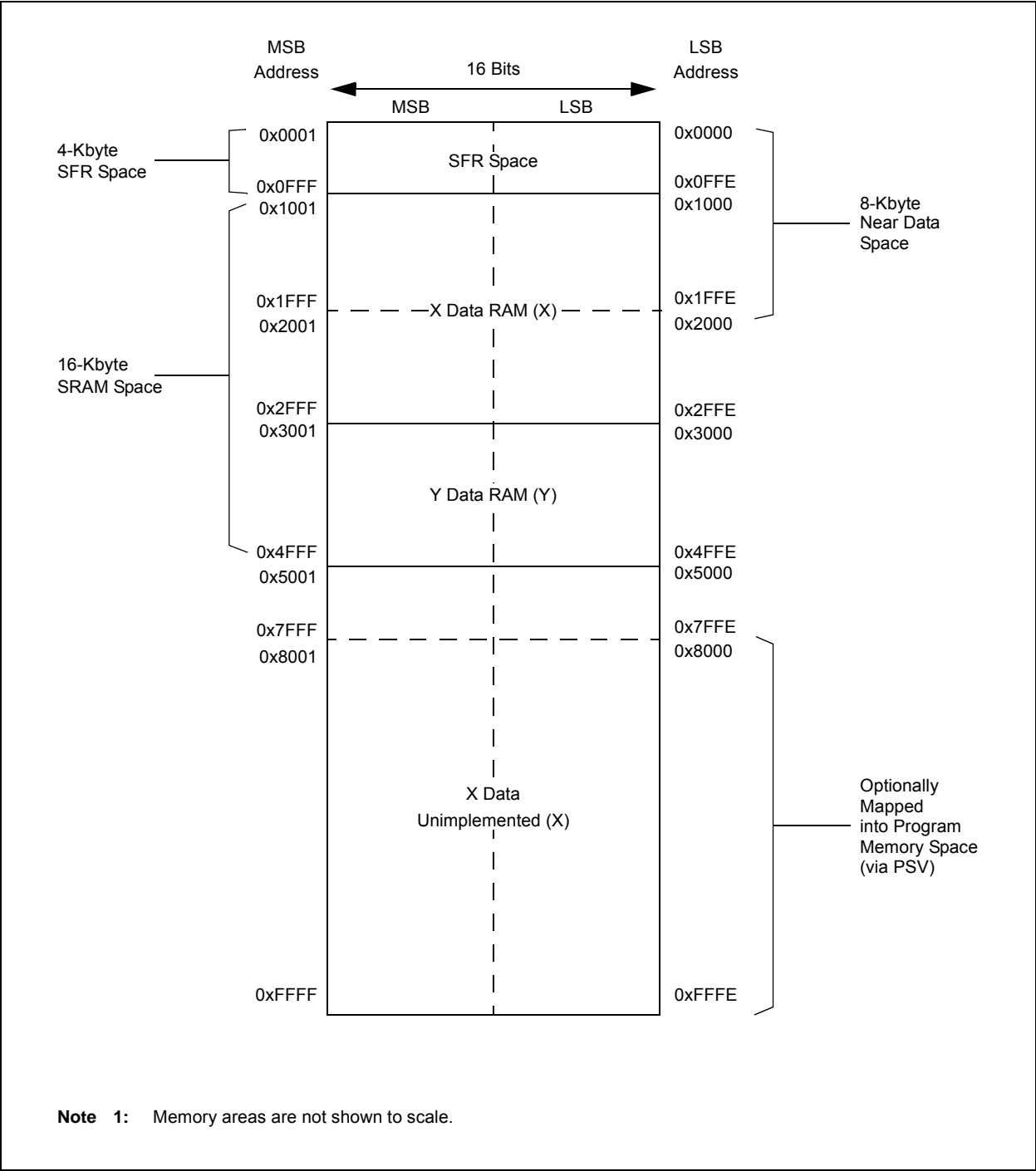
**dsPIC33EVXXXGM00X/10X FAMILY**

## TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | | | | | | | See definition when WIN = x | | | | | | | | | | |
| C1BUFPNT1 | 0420 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 | 0000 |
| C1BUFPNT2 | 0422 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C1BUFPNT3 | 0424 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C1BUFPNT4 | 0426 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C1RXM0SID | 0430 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM0EID | 0432 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM1EID | 0436 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM2EID | 043A | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF0EID | 0442 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF1EID | 0446 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF2EID | 044A | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF3EID | 044E | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF4EID | 0452 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF5EID | 0456 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF6EID | 045A | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF7EID | 045E | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF8EID | 0462 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF9EID | 0466 | | | | | | | EID<15:0> | | | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF10EID | 046A | | | | | | | EID<15:0> | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-3:  INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)**

bit 3          **ADDRERR:** Address Error Trap Status bit

1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2          **STKERR:** Stack Error Trap Status bit

1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1          **OSCFAIL:** Oscillator Failure Trap Status bit

1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0          **Unimplemented:** Read as '0'

**REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER**

| R/S-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|-------|-----|-----|-----|-----|-----|-----|-----|
| FORCE[(1)] | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| | S = Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FORCE:** Force DMA Transfer bit[(1)]

1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits

01000110 = TX data request (CAN1)[(2)]
00100110 = Input Capture 4 (IC4)
00100101 = Input Capture 3 (IC3)
00100010 = RX data ready (CAN1)
00100001 = SPI2 transfer done (SPI2)
00011111 = UART2 Transmitter (UART2TX)
00011110 = UART2 Receiver (UART2RX)
00011100 = Timer5 (TMR5)
00011011 = Timer4 (TMR4)
00011010 = Output Compare 4 (OC4)
00011001 = Output Compare 3 (OC3)
00001101 = ADC1 convert done (ADC1)
00001100 = UART1 Transmitter (UART1TX)
00001011 = UART1 Receiver (UART1RX)
00001010 = SPI1 transfer done (SPI1)
00001000 = Timer3 (TMR3)
00000111 = Timer2 (TMR2)
00000110 = Output Compare 2 (OC2)
00000101 = Input Capture 2 (IC2)
00000010 = Output Compare 1 (OC1)
00000001 = Input Capture 1 (IC1)
00000000 = External Interrupt 0 (INT0)

**Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

**2:** This select bit is only available on dsPIC33EVXXXGM10X devices.

**REGISTER 8-7:** **DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER**[1]

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PAD<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PAD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0      **PAD<15:0>:** DMA Peripheral Address Register bits

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**REGISTER 8-8:** **DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER**[1]

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-------|-------|-------|-------|-------|-------|
| — | — | CNT<13:8>[2] | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CNT<7:0>[2] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14      **Unimplemented:** Read as '0'

bit 13-0      **CNT<13:0>:** DMA Transfer Count Register bits[2]

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

   **2:** The number of DMA transfers = CNT<13:0> + 1.

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## 11.0 I/O PORTS

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports"** (DS70000598) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. All the pins in the device are 5V tolerant pins.

### 11.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch; writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means that the corresponding LATx and TRISx registers, and the port pin are read as zeros.
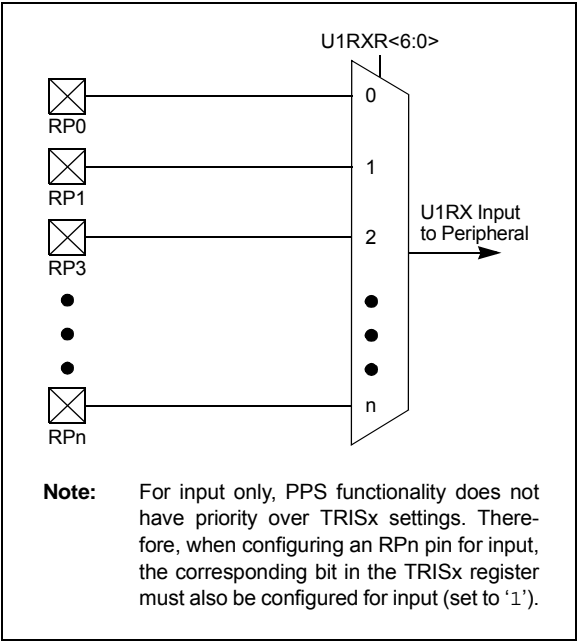
When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port, because there is no other competing source of output.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**
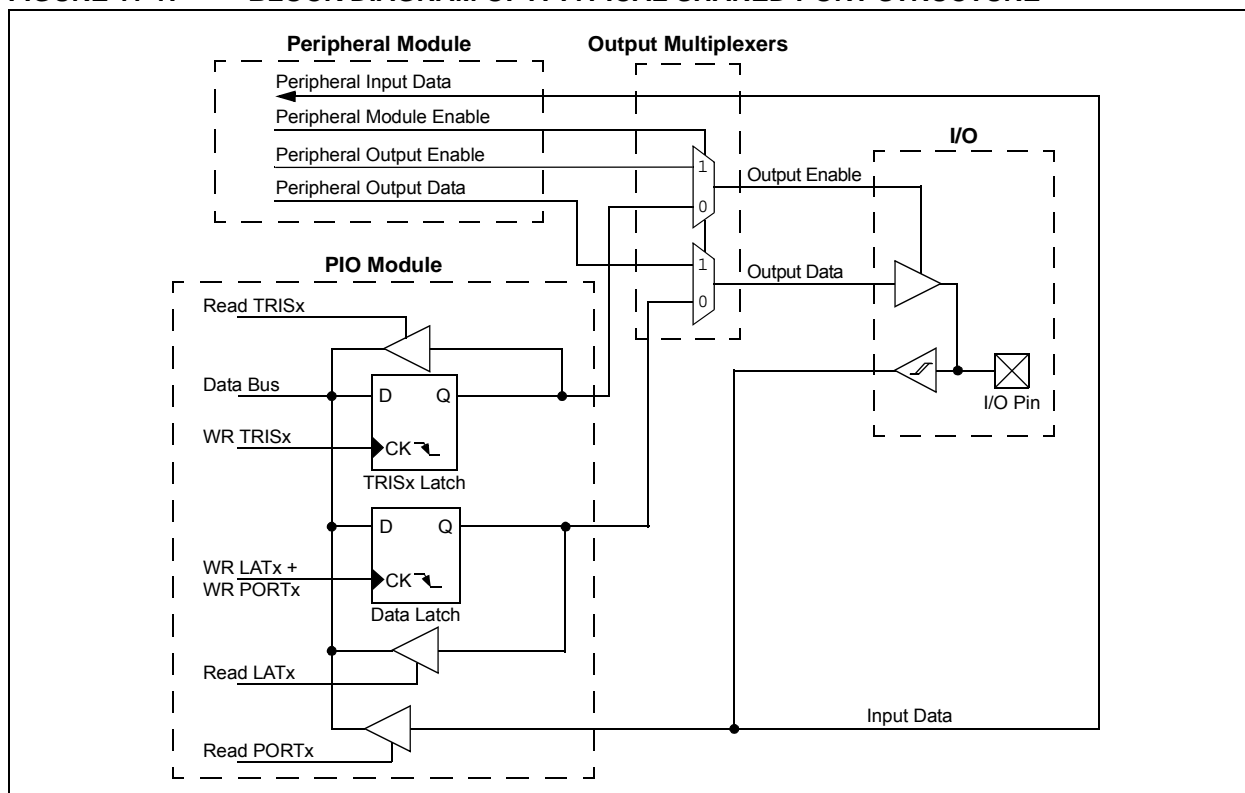
For example, Figure 11-2 shows the remappable pin selection for the U1RX input.

**FIGURE 11-2:** **REMAPPABLE INPUT FOR U1RX**



**Note:** For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

### 11.5.4.1 Virtual Connections

dsPIC33EVXXXGM00X/10X family devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 "Op Amp/Comparator Module"**).

These devices provide six virtual output pins (RPV0-RPV5) that correspond to the outputs of six peripheral pin output remapper blocks (RP176-RP181). The six virtual remapper outputs (RP176-RP181) are not connected to actual pins. The six virtual pins may be read by any of the input remappers as inputs, RPI176-RPI181. These virtual pins can be used to connect the internal peripherals, whose signals are of significant use to the other peripherals, but these output signals are not present on the device pin.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<7:0> bits of the RPINR12 register to the value of 'b0000001', the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

## 13.0 TIMER2/3 AND TIMER4/5

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

> **Note:** For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

> **Note:** Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

## REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|-------|-------|-------|-----|-----|-----|-----|-----|
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-----|-----|-----|-------|-------|
| — | — | — | — | — | — | FRMDLY | SPIBEN |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FRMEN:** Framed SPIx Support bit

1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as the Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** SPIx Frame Sync Pulse Direction Control bit

1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit

1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit

1 = Frame Sync pulse coincides with the first bit clock
0 = Frame Sync pulse precedes the first bit clock

bit 0 **SPIBEN:** SPIx Enhanced Buffer Enable bit

1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Standard mode)

**REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R/C-0 | R-0 | R/W-0, HC |
|---|---|---|---|---|---|---|---|
| PAUSE | NIB2 | NIB1 | NIB0 | CRCERR | FRMERR | RXIDLE | SYNCTXEN[1] |
| bit 7 | | | | | | | bit 0 |

| Legend: | C = Clearable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PAUSE:** Pause Period Status bit

1 = The module is transmitting/receiving a pause period
0 = The module is not transmitting/receiving a pause period

bit 6-4 **NIB<2:0>:** Nibble Status bit

Module in Transmit Mode (RCVEN = 0):
111 = Module is transmitting a CRC nibble
110 = Module is transmitting Data Nibble 6
101 = Module is transmitting Data Nibble 5
100 = Module is transmitting Data Nibble 4
011 = Module is transmitting Data Nibble 3
010 = Module is transmitting Data Nibble 2
001 = Module is transmitting Data Nibble 1
000 = Module is transmitting a status nibble or pause period, or is not transmitting

Module in Receive Mode (RCVEN = 1):
111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred
110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
000 = Module is receiving a status nibble or waiting for Sync

bit 3 **CRCERR:** CRC Status bit (Receive mode only)

1 = A CRC error occurred for the 1-6 data nibbles in SENTxDATH/L
0 = A CRC error has not occurred

bit 2 **FRMERR:** Framing Error Status bit (Receive mode only)

1 = A data nibble was received with less than 12 tick periods or greater than 27 tick periods
0 = Framing error has not occurred

bit 1 **RXIDLE:** SENTx Receiver Idle Status bit (Receive mode only)

1 = The SENTx data bus has been Idle (high) for a period of SYNCMAX<15:0> or greater
0 = The SENTx data bus is not Idle

**Note 1:** In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

## 24.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Analog-to-Digital (ADC) module in the dsPIC33EVXXXGM00X/10X family devices supports up to 36 analog input channels.

The ADC module can be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

> **Note:** The ADC module needs to be disabled before modifying the AD12B bit.

### 24.1 Key Features

#### 24.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) Conversion
- Conversion Speeds of up to 1.1 Msps
- Up to 36 Analog Input Pins
- Connections to Four Internal Op Amps
- Connections to the Charge Time Measurement Unit (CTMU) and Temperature Measurement Diode
- Simultaneous Sampling of:
  - Up to four analog input pins
  - Four op amp outputs
- Combinations of Analog Inputs and Op Amp Outputs
- Automatic Channel Scan mode
- Selectable Conversion Trigger Source
- Selectable Buffer Fill modes
- Four Result Alignment Options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle Modes

#### 24.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed previously, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration. Therefore, simultaneous sampling of multiple channels is not supported.

The ADC has up to 36 analog inputs. The analog inputs, AN32 through AN63, are multiplexed, thus providing flexibility in using any of these analog inputs in addition to the analog inputs, AN0 through AN31. Since AN32 through AN63 are multiplexed, do not use two channels simultaneously, since it may result in erroneous output from the module. These analog inputs are shared with op amp inputs and outputs, comparator inputs and external voltage references. When op amp/comparator functionality is enabled, the analog input that shares that pin is no longer available. The actual number of analog input pins and op amps depends on the specific device.

A block diagram of the ADC module with connection options is shown in Figure 24-1. Figure 24-2 shows a block diagram of the ADC conversion clock period.

## 24.3 ADC Control Registers

### REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-------|-------|-----|-------|-------|-------|
| ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC, HS | R/C-0, HC, HS |
|-------|-------|-------|-------|-------|-------|---------------|---------------|
| SSRC2 | SSRC1 | SSRC0 | SSRCG | SIMSAM | ASAM | SAMP | DONE[1] |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| | C = Clearable bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | W = Writable bit | HS = Hardware Settable bit   HC = Hardware Clearable bit |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared   x = Bit is unknown |

bit 15    **ADON:** ADCx Operating Mode bit
1 = ADCx module is operating
0 = ADCx is off

bit 14    **Unimplemented:** Read as '0'

bit 13    **ADSIDL:** ADCx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12    **ADDMABM:** ADCx DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather mode address to the DMA channel based on the index of the analog input and the size of the DMA buffer

bit 11    **Unimplemented:** Read as '0'

bit 10    **AD12B:** ADCx 10-Bit or 12-Bit Operation Mode bit
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8    **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional ($D_{OUT}$ = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional ($D_{OUT}$ = dddd dddd dd00 0000)
01 = Signed integer ($D_{OUT}$ = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer ($D_{OUT}$ = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional ($D_{OUT}$ = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional ($D_{OUT}$ = dddd dddd dddd 0000)
01 = Signed integer ($D_{OUT}$ = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer ($D_{OUT}$ = 0000 dddd dddd dddd)

**Note 1:** Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

## 26.2 Comparator Voltage Reference Registers

### REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|-------|-------|-----|-----|-------|--------|-----|-----|
| CVREN | CVROE | — | — | CVRSS | VREFSEL | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-------|-------|-------|-------|-------|-------|-------|
| — | CVR6 | CVR5 | CVR4 | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CVREN:** Comparator Voltage Reference Enable bit

1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF1O Pin) bit

1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from the CVREF1O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit

1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit

1 = CVREFIN = CVREF+
0 = CVREFIN is generated by the resistor network

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits

1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

**TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial  -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param. | Symbol | Characteristic[1] | Min. | Typ.[2] | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-25:** SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS
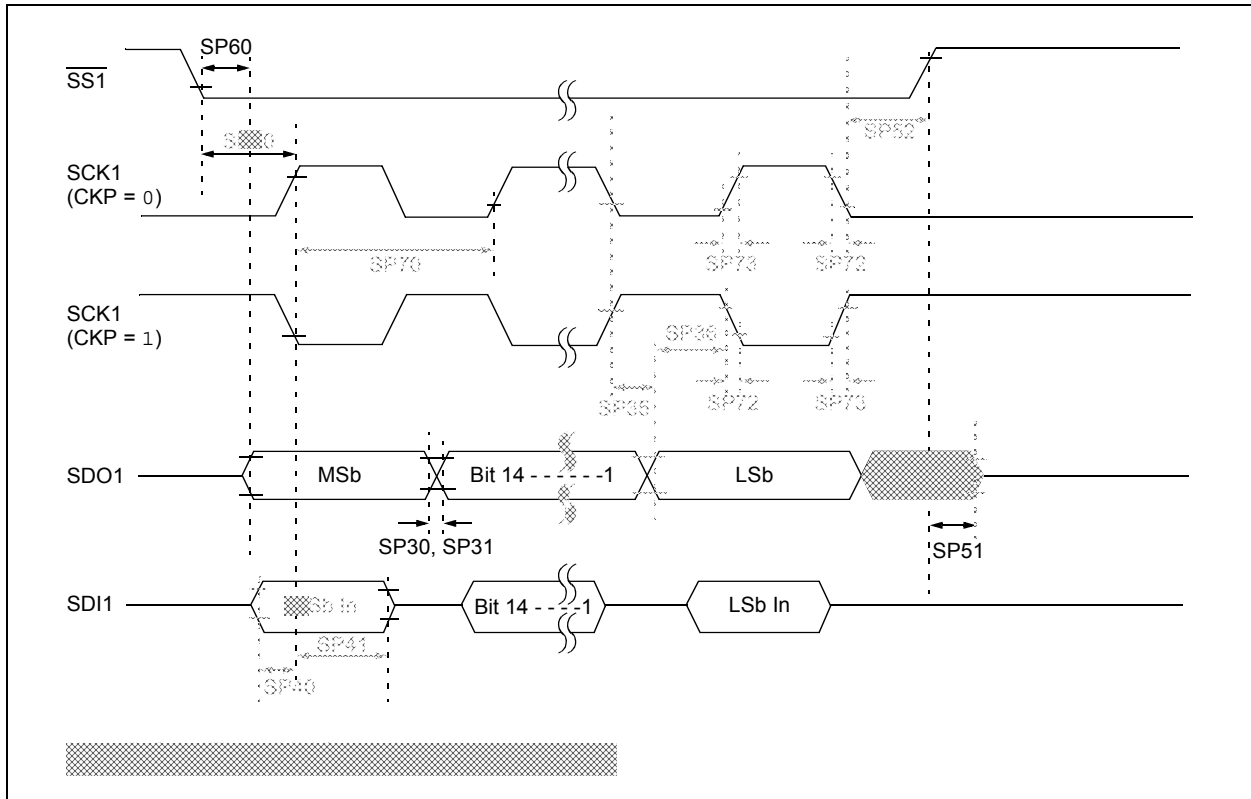
## 32.18 ADC INL

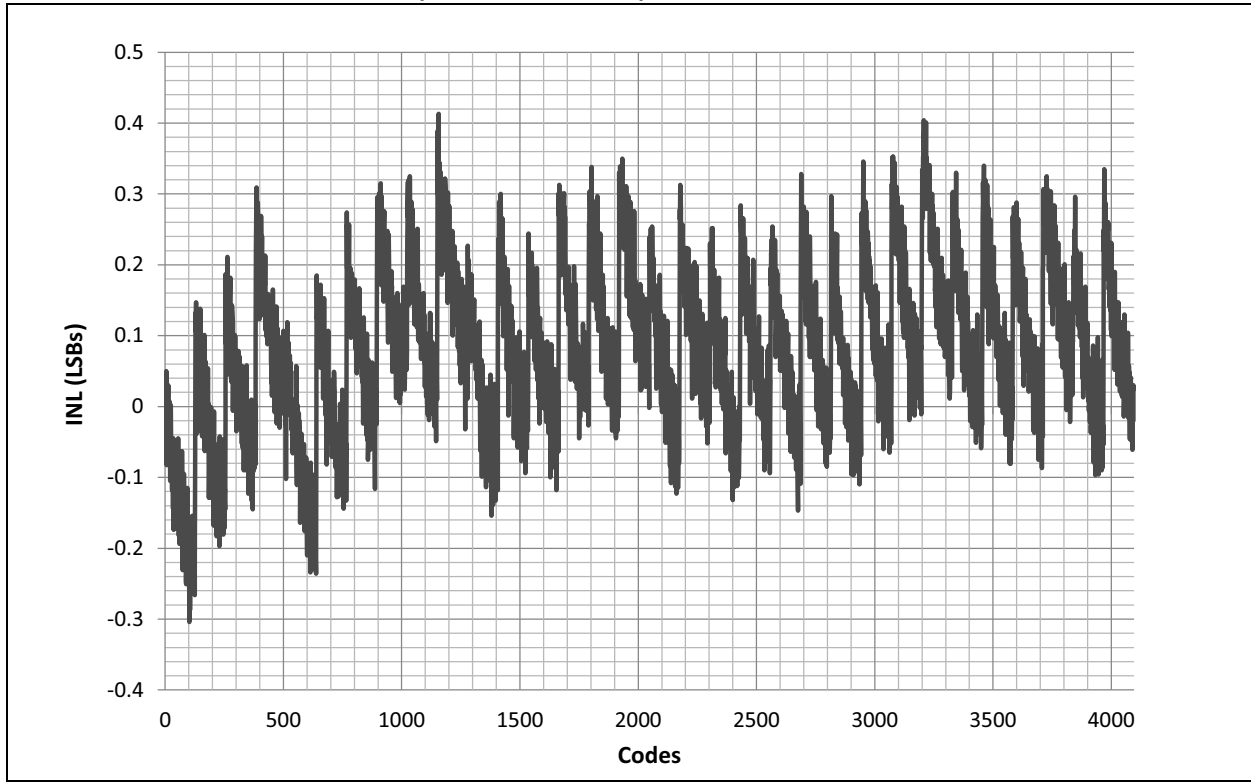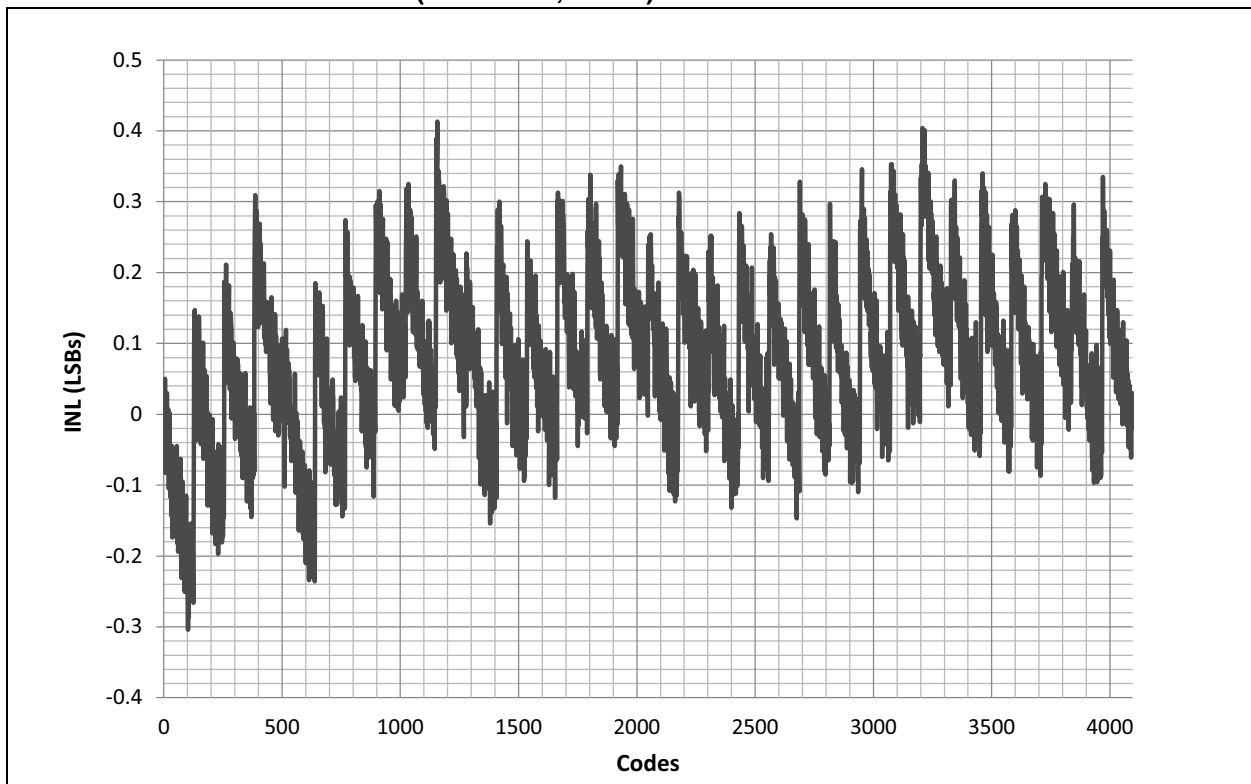**FIGURE 32-45:** **TYPICAL INL (V$_{DD}$ = 5.5V, -40°C)**



**FIGURE 32-46:** **TYPICAL INL (V$_{DD}$ = 5.5V, +25°C)**

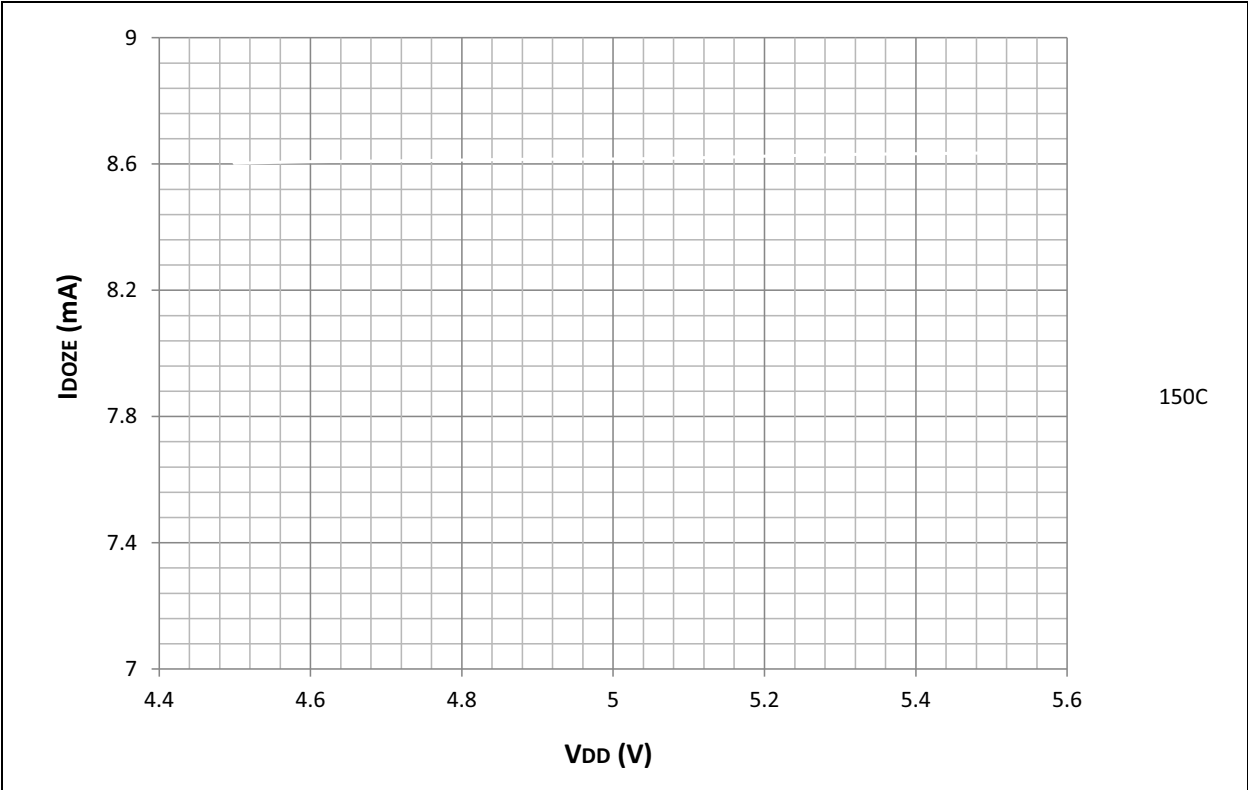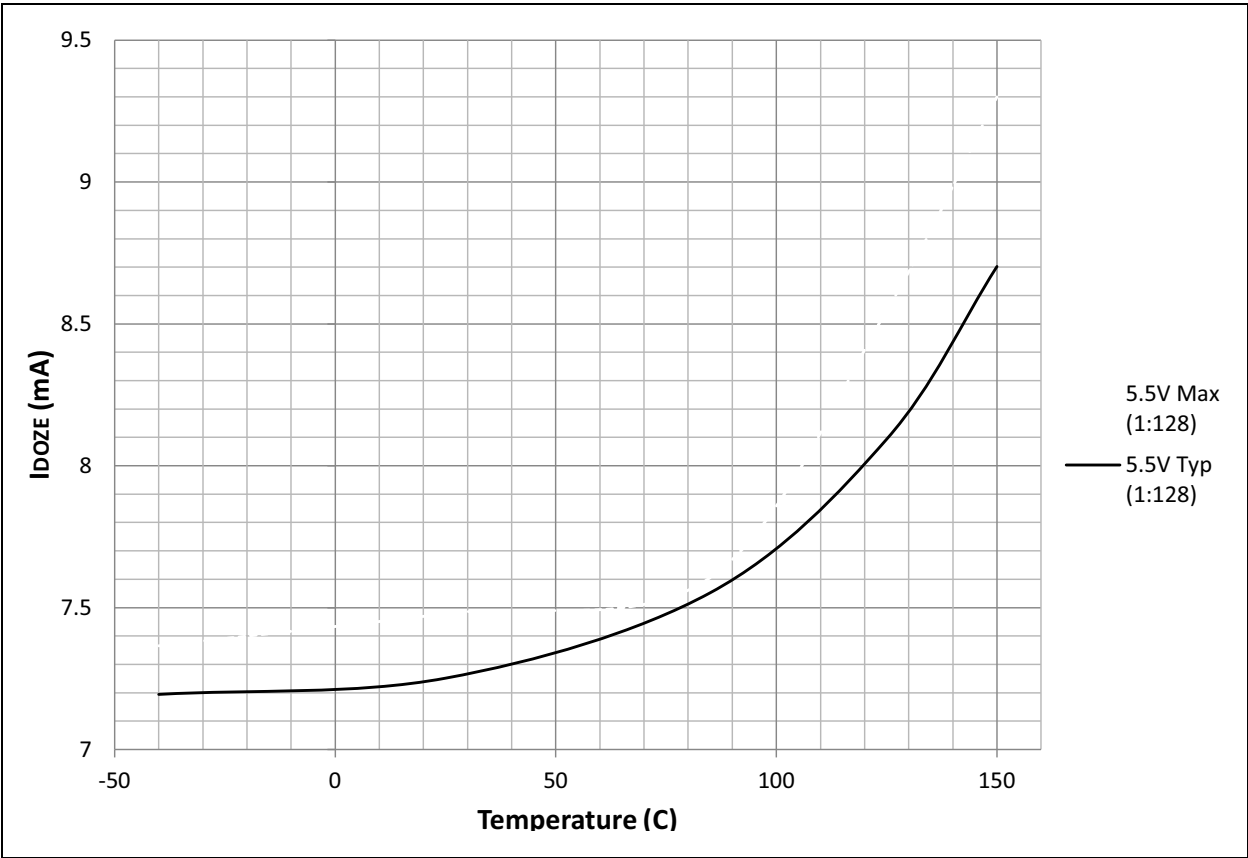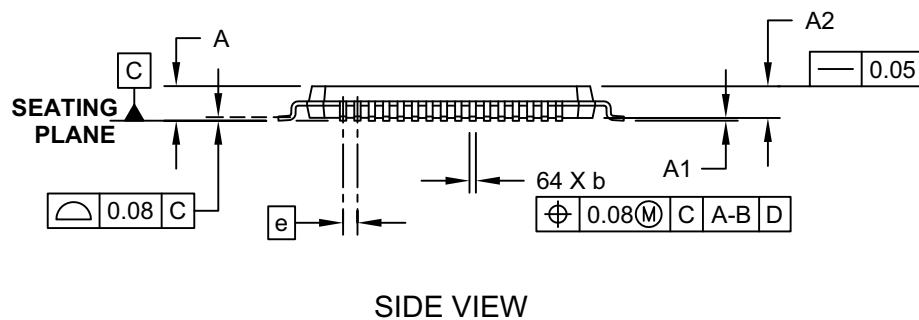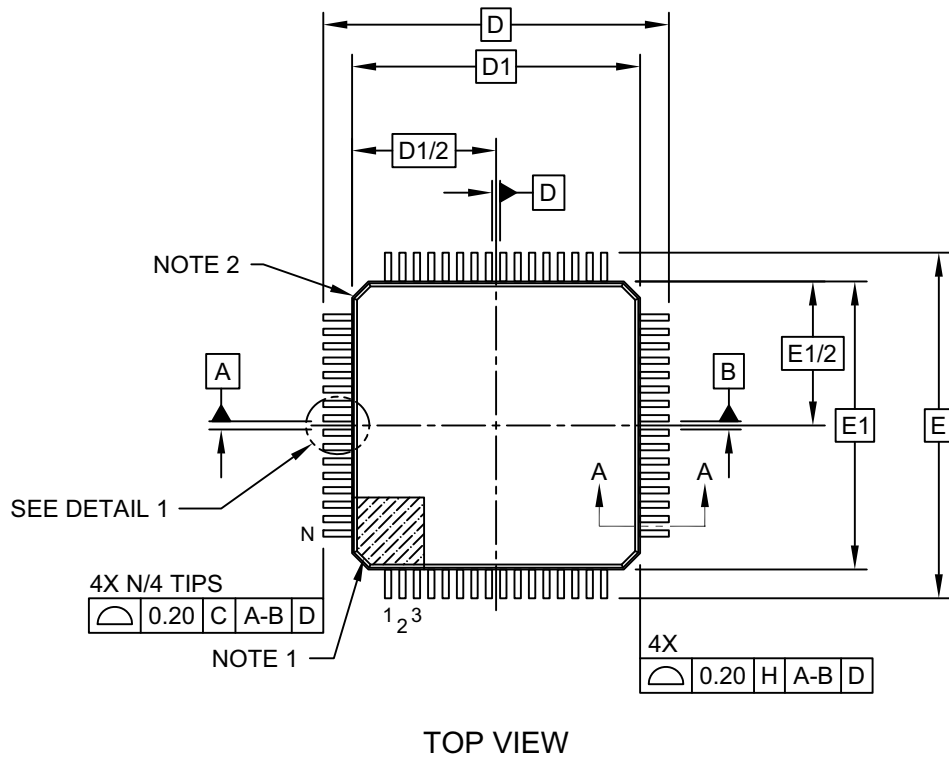**FIGURE 33-11:** TYPICAL I$_{DOZE}$ vs. V$_{DD}$ (DOZE 1:128, 70 MIPS)



**FIGURE 33-12:** TYPICAL/MAXIMUM I$_{DOZE}$ vs. TEMPERATURE (DOZE 1:128, 70 MIPS)

**64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2