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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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| Details | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I ² C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm004t-i-ml |
| | |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-------------|-------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|--------|-------|-------|-------|--------|---------------|
| TRISA | 0E00 | _ | — | — | | | TRISA< | 12:7> | | | — | — | TRISA4 | — | _ | TRISA | <1:0> | 1F93 |
| PORTA | 0E02 | _ | — | — | | | RA<12 | 2:7> | | | | — | RA4 | — | - | RA< | 1:0> | 0000 |
| LATA | 0E04 | _ | — | — | | | LATA<1 | 2:7> | | | | — | LATA4 | — | - | LATA | <1:0> | 0000 |
| ODCA | 0E06 | — | — | — | | | ODCA< | 12:7> | | | | _ | ODCA4 | — | - | ODCA | <1:0> | 0000 |
| CNENA | 0E08 | _ | _ | _ | | | CNIEA< | 12:7> | | | _ | _ | CNIEA4 | _ | _ | CNIEA | <1:0> | 0000 |
| CNPUA | 0E0A | — | — | — | | | CNPUA< | :12:7> | | | | _ | CNPUA4 | — | - | CNPU | ۹<1:0> | 0000 |
| CNPDA | 0E0C | _ | _ | _ | | | CNPDA< | :12:7> | | | _ | _ | CNPDA4 | _ | _ | CNPD | A<1:0> | 0000 |
| ANSELA | 0E0E | _ | — | — | | ANSA< | <12:9> | | | ANSA7 | | — | ANSA4 | — | - | ANSA | <1:0> | 1E93 |
| SR1A | 0E10 | _ | — | — | | — | _ | SR1A9 | | | | — | SR1A4 | — | - | | | 0000 |
| SR0A | 0E12 | _ | _ | — | | _ | _ | SR0A9 | | | | — | SR0A4 | — | _ | | _ | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-------------|-------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|------------|-------|------------|-----------|-------|---------------|
| TRISA | 0E00 | _ | _ | _ | _ | _ | | TRISA | <10:7> | | — | — | | - | TRISA<4:0> | > | | DF9F |
| PORTA | 0E02 | _ | _ | _ | _ | _ | | RA<1 | 0:7> | | — | — | | | RA<4:0> | | | 0000 |
| LATA | 0E04 | — | _ | _ | _ | _ | | LATA< | 10:7> | | | — | | | LATA<4:0> | | | 0000 |
| ODCA | 0E06 | — | _ | _ | _ | _ | | ODCA< | <10:7> | | | — | | (| ODCA<4:0> | > | | 0000 |
| CNENA | 0E08 | — | — | _ | _ | | | CNIEA | <10:7> | | | — | | (| CNIEA<4:0 | > | | 0000 |
| CNPUA | 0E0A | — | — | _ | _ | | | CNPUA | <10:7> | | | — | | C | NPUA<4:0 | > | | 0000 |
| CNPDA | 0E0C | — | — | _ | _ | | | CNPDA | <10:7> | | | — | CNPDA<4:0> | | | 0000 | | |
| ANSELA | 0E0E | — | — | _ | _ | | ANSA< | :10:9> | _ | ANSA7 | | — | ANSA4 | — | | ANSA<2:0> | • | 1813 |
| SR1A | 0E10 | — | — | _ | _ | | | SR1A9 | _ | _ | | — | SR1A4 | — | — | | | 0000 |
| SR0A | 0E12 | — | — | _ | _ | | | SR0A9 | _ | _ | | — | SR0A4 | — | — | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.0 RESETS

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Uninitialized W Register Reset
 - Security Reset
 - Illegal Address Mode Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 4.0 "Memory Organization" of this device data sheet for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in the other sections of this device data sheet.

Note: The status bits in the RCON register should be cleared after they are read. Therefore, the next RCON register value after a device Reset is meaningful.

Note: In all types of Resets, to select the device clock source, the contents of OSCCON are initialized from the FNOSCx Configuration bits in the FOSCSEL Configuration register.

| REGISTER | | CON: DMA C | | | | | |
|---------------|----------------------|--|---------------------|-------------------|-----------------|-----------------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| CHEN | SIZE | DIR | HALF | NULLW | — | — | _ |
| bit 15 | | | | • | | | bit 8 |
| | | | | | | | |
| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | AMODE1 | AMODE0 | — | _ | MODE1 | MODE0 |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable | e bit | W = Writable | bit | U = Unimplen | nented bit, rea | d as '0' | |
| -n = Value at | POR | '1' = Bit is set | | '0' = Bit is clea | ared | x = Bit is unkn | own |
| | | | | | | | |
| bit 15 | CHEN: DMA | Channel Enabl | le bit | | | | |
| | 1 = Channel | | | | | | |
| | 0 = Channel | is disabled | | | | | |
| bit 14 | SIZE: DMA D | ata Transfer S | ize bit | | | | |
| | 1 = Byte 0 = Word | | | | | | |
| L:1 1 0 | | anafar Direction | a hit (a a ura a /d | activation bus | a a la at) | | |
| bit 13 | | ansfer Directior om RAM addre | - | | - | | |
| | | om peripheral a | | | | | |
| bit 12 | | Block Transfer | | | | | |
| | | nterrupt when | - | | ved | | |
| | | nterrupt when | | | | | |
| bit 11 | NULLW: Null | Data Peripher | al Write Mode | Select bit | | | |
| | | write to periph | eral in addition | n to RAM write | (DIR bit must | also be clear) | |
| | 0 = Normal c | peration | | | | | |
| bit 10-6 | - | ted: Read as ' | | | | | |
| bit 5-4 | | >: DMA Chann | el Addressing | Mode Select b | its | | |
| | 11 = Reserve | | 1. | | | | |
| | | ral Indirect moon Indirect without read without read without the second second second second second second second second second s | | ent mode | | | |
| | • | Indirect with F | | | | | |
| bit 3-2 | • | ted: Read as ' | | | | | |
| bit 1-0 | - | DMA Channel | | de Select bits | | | |
| | | | | | transfer from | /to each DMA bu | (ffer) |
| | | ous Ping-Pong | modes are en | abled | | | |
| | | | | | | | |
| | | ot Ping-Pong n ous Ping-Pong | nodes are disa | bled | | | |

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----------------------------------|-------|------------------|-------|------------------|-----------------|-----------------|-------|
| | | | PAD | <15:8> | | | |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | | | PAI |)<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit W = Writable bit | | | | U = Unimpler | mented bit, rea | d as '0' | |
| -n = Value at P | POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unkr | nown |

bit 15-0 PAD<15:0>: DMA Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|-----|-------|-------|-------|------------------|-------|-------|
| — | — | | | CNT< | 13:8> (2) | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-----------------|-------|-------|-------|
| | | | CNT< | 7:0> (2) | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|-------------------|------------------|------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, | , read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 Unimplemented: Read as '0'

bit 13-0 CNT<13:0>: DMA Transfer Count Register bits⁽²⁾

- **Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.
 - **2:** The number of DMA transfers = CNT<13:0> + 1.

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- · Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|--------------------------------|------------------------------|---|-------|------------------|-----------------|-----------------|-------|
| _ | _ | FBP5 | FBP4 | FBP3 | FBP2 | FBP1 | FBP0 |
| bit 15 | · | · | | | | · | bit |
| | | | | | | | |
| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | FNRB5 | FNRB4 | FNRB3 | FNRB2 | FNRB1 | FNRB0 |
| bit 7 | | | | | | | bit |
| Legend: | | | | | | | |
| R = Readable | e bit | W = Writable | bit | U = Unimpler | nented bit, rea | id as '0' | |
| -n = Value at | POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unki | nown |
| bit 13-8 bit 7-6 bit 5-0 | - | B30 buffer RB1 buffer RB0 buffer nted: Read as ' : FIFO Next Rea B31 buffer | | ter bits | | | |
| | 0000001 = TI 0000000 = TI | | | | | | |

REGISTER 22-5: CxFIFO: CANx FIFO STATUS REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---------------|-------------------------------|----------------------------------|----------------|-------------------|------------------|-----------------|----------|
| EDG1MOD | EDG1POL | EDG1SEL3 | EDG1SEL2 | EDG1SEL1 | EDG1SEL0 | EDG2STAT | EDG1STAT |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| EDG2MOD | EDG2POL | EDG2SEL3 | EDG2SEL2 | EDG2SEL1 | EDG2SEL0 | _ | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable | e bit | W = Writable | bit | U = Unimplen | nented bit, read | l as '0' | |
| -n = Value at | POR | '1' = Bit is set | | '0' = Bit is clea | ared | x = Bit is unkr | nown |
| | | | | | | | |
| bit 15 | | Edge 1 Edge Sa | | Selection bit | | | |
| | • | s edge-sensitive | | | | | |
| hit 11 | - | s level-sensitive | | | | | |
| bit 14 | | dge 1 Polarity | | dae response | | | |
| | Ų | s programmed f | | v . | | | |
| bit 13-10 | - | :0>: Edge 1 So | - | • | | | |
| | 1111 = Fosc | • | | | | | |
| | 1110 = OSCI | pin | | | | | |
| | 1101 = FRC (| | | | | | |
| | 1100 = BFRC | COSCIIIator | otor | | | | |
| | 1011 - Intern 1010 = Reser | | aloi | | | | |
| | 1001 = Reser | | | | | | |
| | 1000 = Rese r | | | | | | |
| | 0111 = Reser | | | | | | |
| | 0110 = Reser | | | | | | |
| | 0100 = Resei | | | | | | |
| | 0011 = CTED | 01 pin | | | | | |
| | 0010 = CTED | • | | | | | |
| | 0001 = OC1 I 0000 = TMR1 | | | | | | |
| bit 9 | | Edge 2 Status b | .i+ | | | | |
| bit 9 | | - | | vritten to contro | ol the edge sour | rce | |
| | 1 = Edge 2 h | | | | ine eage soul | | |
| | | as not occurred | ł | | | | |
| bit 8 | EDG1STAT: E | Edge 1 Status b | it | | | | |
| | | | 1 and can be v | vritten to contro | ol the edge sour | rce. | |
| | 1 = Edge 1 h | | J | | | | |
| hit 7 | - | as not occurred | | Coloction hit | | | |
| bit 7 | | Edge 2 Edge Sa edge-sensitive | | Selection Dit | | | |
| | • | level-sensitive | | | | | |
| bit 6 | - | dge 2 Polarity | | | | | |
| | | s programmed f | | dge response | | | |
| | | programmed f | | | | | |
| | | | | | | | |

REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5) (CONTINUED)

- bit 7-6 EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits⁽³⁾
 - 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
 - 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

 $\frac{\text{If CPOL} = 1 \text{ (inverted polarity):}}{\text{Low-to-high transition of the comparator output.}}$ $\frac{\text{If CPOL} = 0 \text{ (non-inverted polarity):}}{\text{High-to-low transition of the comparator output.}}$

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):

High-to-low transition of the comparator output.

- If CPOL = 0 (non-inverted polarity):
- Low-to-high transition of the comparator output.
- 00 = Trigger/event/interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator x Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to the internal CVREFIN voltage
 - 0 = VIN+ input connects to the CxIN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Op Amp/Comparator x Channel Select bits⁽¹⁾
 - 11 = Inverting input of op amp/comparator connects to the CxIN4- pin
 - 10 = Inverting input of op amp/comparator connects to the CxIN3- pin
 - 01 = Inverting input of op amp/comparator connects to the CxIN2- pin
 - 00 = Inverting input of op amp/comparator connects to the CxIN1- pin
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.
 - **2:** The op amp and the comparator can be used simultaneously in these devices. The OPAEN bit only enables the op amp while the comparator is still functional.
 - 3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator x Event bit, CEVT (CMxCON<9>), and the Comparator Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

| bit 7-6 | EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits ⁽²⁾ |
|---------|---|
| | 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0) 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0) |
| | If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output. |
| | If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output. |
| | 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0) |
| | If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output. |
| | If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output. |
| | 00 = Trigger/event/interrupt generation is disabled |
| bit 5 | Unimplemented: Read as '0' |
| bit 4 | CREF: Comparator 4 Reference Select bit (VIN+ input) ⁽¹⁾ |
| | 1 = VIN+ input connects to the internal CVREFIN voltage 0 = VIN+ input connects to the C4IN1+ pin |
| bit 3-2 | Unimplemented: Read as '0' |
| bit 1-0 | CCH<1:0>: Comparator 4 Channel Select bits ⁽¹⁾ |
| | 11 = VIN- input of comparator connects to the C4IN4- pin 10 = VIN- input of comparator connects to the C4IN3- pin 01 = VIN- input of comparator connects to the C4IN2- pin 00 = VIN- input of comparator connects to the C4IN1- pin |
| Note 1: | Inputs that are selected and not available will be tied to Vss. See the " Pin Diagrams " section for available inputs for each package. |

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

26.2 Comparator Voltage Reference Registers

REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|--------|-------|-------|-------|-------|---------|-------|-------|
| CVREN | CVROE | — | _ | CVRSS | VREFSEL | — | _ |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| _ | CVR6 | CVR5 | CVR4 | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|-------------------|------------------|-----------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit | t, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

| bit 15 | CVREN: Comparator Voltage Reference Enable bit |
|-----------|---|
| | 1 = Comparator voltage reference circuit is powered on |
| | 0 = Comparator voltage reference circuit is powered down |
| bit 14 | CVROE: Comparator Voltage Reference Output Enable (CVREF10 Pin) bit |
| | 1 = Voltage level is output on the CVREF10 pin |
| | 0 = Voltage level is disconnected from the CVREF10 pin |
| bit 13-12 | Unimplemented: Read as '0' |
| bit 11 | CVRSS: Comparator Voltage Reference Source Selection bit |
| | 1 = Comparator reference source, CVRsRC = CVREF+ – AVss |
| | 0 = Comparator reference source, CVRSRC = AVDD – AVSS |
| bit 10 | VREFSEL: Voltage Reference Select bit |
| | 1 = CVREFIN = CVREF+ |
| | 0 = CVREFIN is generated by the resistor network |
| bit 9-7 | Unimplemented: Read as '0' |
| bit 6-0 | CVR<6:0>: Comparator Voltage Reference Value Selection bits |
| | 1111111 = 127/128 x VREF input voltage |
| | • |
| | • |
| | • |
| | 0000000 = 0.0 volts |

| Bit Field | Register | Description |
|---------------|-----------|---|
| OSCIOFNC | FOSC | OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin |
| IOL1WAY | FOSC | Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations |
| FCKSM<1:0> | FOSC | Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| PLLKEN | FOSC | PLL Lock Wait Enable bit 1 = Clock switches to the PLL source; will wait until the PLL lock signal is valid 0 = Clock switch will not wait for PLL lock |
| WDTPS<3:0> | FWDT | Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • • • • • • • • • • • |
| WDTPRE | FWDT | Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32 |
| FWDTEN<1:0> | FWDT | Watchdog Timer Enable bits 11 = WDT is enabled in hardware 10 = WDT is controlled through the SWDTEN bit 01 = WDT is enabled only while device is active and disabled in Sleep; the SWDTEN bit is disabled 00 = WDT and the SWDTEN bit are disabled |
| WINDIS | FWDT | Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode |
| WDTWIN<1:0> | FWDT | Watchdog Timer Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period |
| BOREN | FPOR | Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled |
| ICS<1:0> | FICD | ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use |
| DMTIVT<15:0> | FDMTINTVL | Lower 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits |
| DMTIVT<31:16> | FDMTINTVH | Upper 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits |
| DMTCNT<15:0> | FDMTCNTL | Lower 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits |

| TABLE 27-2: | dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED) |
|-------------|--|
|-------------|--|

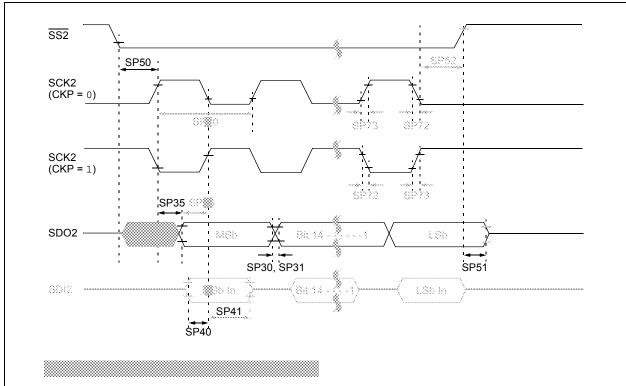


FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

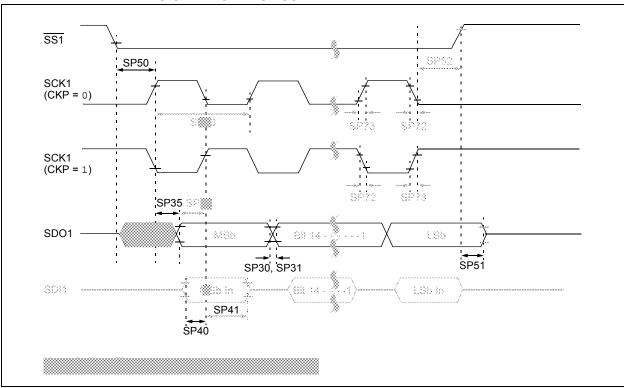


FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

dsPIC33EVXXXGM00X/10X FAMILY

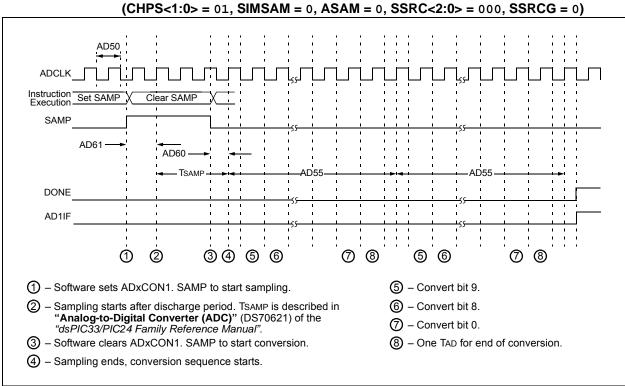


FIGURE 30-35: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS

FIGURE 30-36: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)

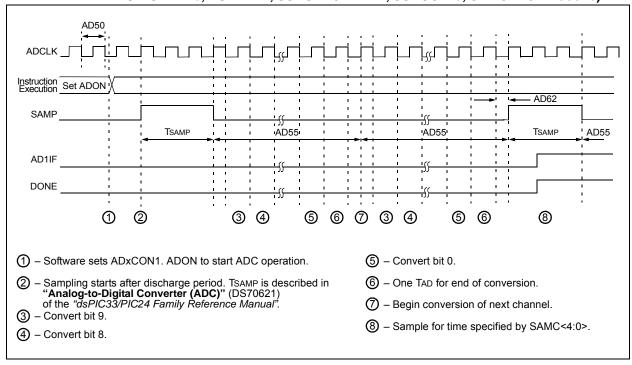
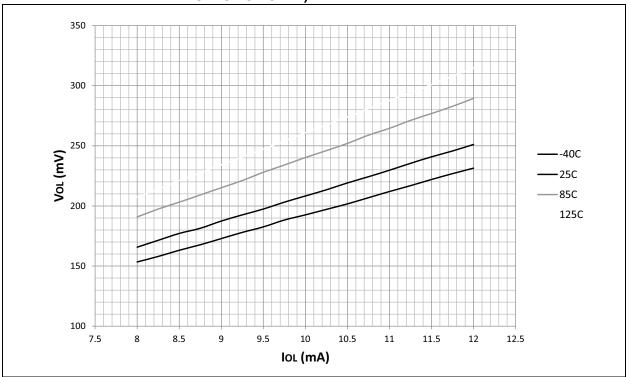
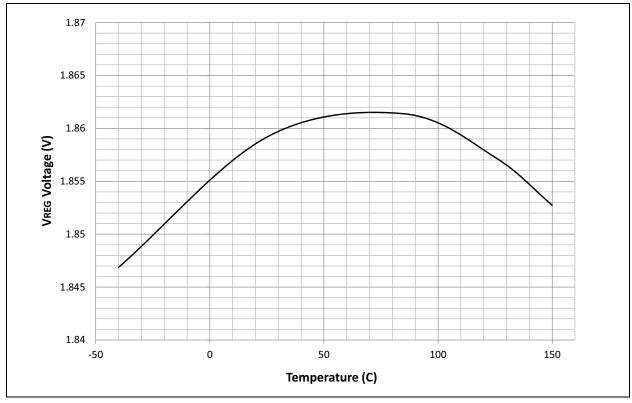


FIGURE 32-33: TYPICAL Vol 4x DRIVER PINS vs. Iol (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

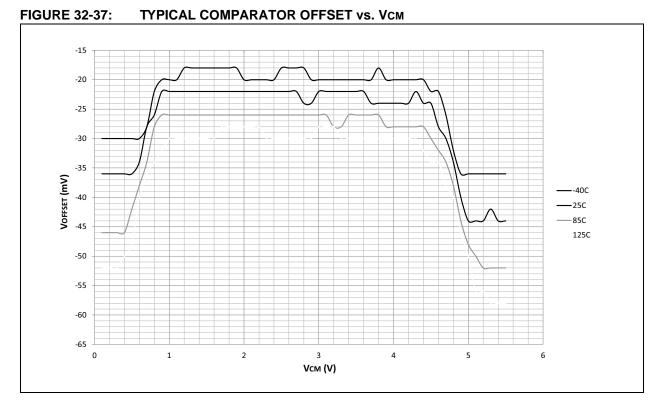


32.11 VREG

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE

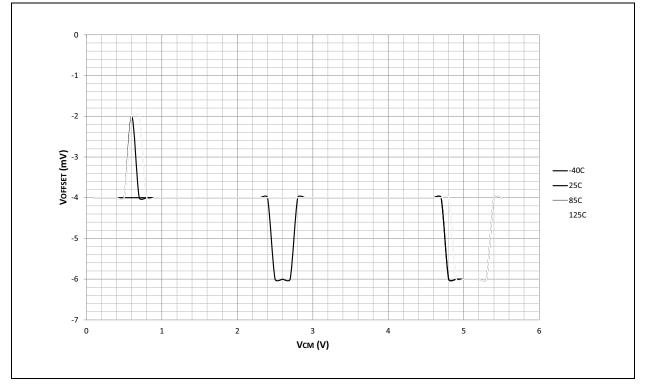


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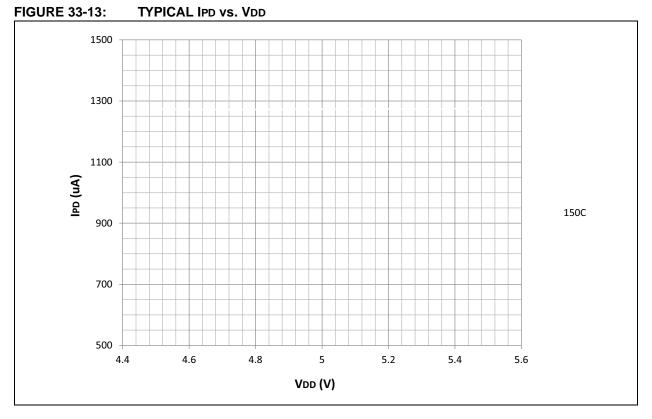
32.14 Comparator Op Amp Offset



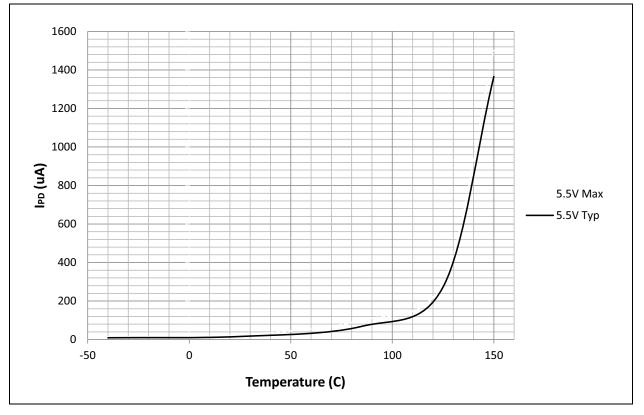


dsPIC33EVXXXGM00X/10X FAMILY

33.4 IPD

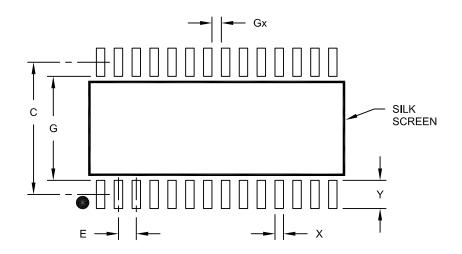






28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| | Units MILLIMETERS | | S | |
|--------------------------|-------------------|----------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | С | | 9.40 | |
| Contact Pad Width (X28) | Х | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

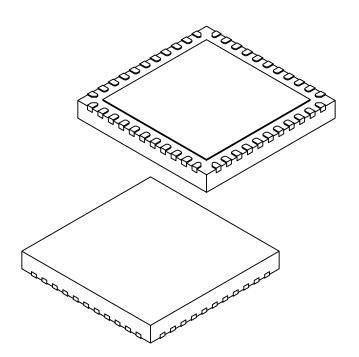
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| | Units MILLIMETERS | | | S |
|-------------------------|-------------------|----------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 44 | | |
| Pitch | е | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 8.00 BSC | | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | 8.00 BSC | | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2

| Peripheral Pin Select (PPS) | |
|---|---|
| Control Registers 1 | 53 |
| Input Sources, Maps Input to Function1 | |
| Output Selection for Remappable Pins 1 | |
| Pinout I/O Descriptions (table) | |
| Power-Saving Features1 | |
| Clock Frequency and Switching1 | |
| Instruction-Based Modes1 | |
| Idle1 | |
| Sleep1 | 34 |
| Interrupts Coincident with Power Save | 24 |
| Instructions1 | |
| Program Address Space Construction | |
| Data Access from Program Memory Using | 19 |
| Table Instructions | 81 |
| Memory Map for dsPIC33EV128GM00X/10X | 01 |
| Devices | 33 |
| Memory Map for dsPIC33EV256GM00X/10X | 00 |
| Devices | 34 |
| Memory Map for dsPIC33EV32GM00X/10X | |
| Devices | 31 |
| Memory Map for dsPIC33EV64GM00X/10X | |
| Devices | 32 |
| Table Read Instructions | |
| TBLRDH | 81 |
| TBLRDL | 81 |
| Program Memory | |
| Interrupt/Trap Vectors | |
| Organization | |
| Reset Vector | 35 |
| Programmer's Model | |
| Register Descriptions | 23 |
| | |
| R | |
| | |
| Referenced Sources | |
| Referenced Sources Register Maps | 12 |
| Referenced Sources Register Maps ADC1 | 12 46 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) | 12 46 47 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) | 12 46 47 47 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) | 12 46 47 47 48 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) | 12 46 47 47 48 18 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 47 48 18 41 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 18 41 46 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 47 48 18 41 46 59 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 18 41 46 59 52 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 18 41 46 59 52 44 |
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| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 18 41 46 59 52 44 45 53 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator | 12 46 47 48 18 41 46 59 52 44 45 53 53 53 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 41 46 59 52 44 45 53 55 53 57 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words | 12 46 47 48 18 41 46 59 52 44 45 53 58 57 52 |
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| Referenced Sources | 12 46 47 48 8 41 46 52 44 45 53 85 52 53 85 52 46 |
| Referenced Sources | 12 46 47 48 8 41 46 55 53 57 52 44 55 58 57 52 46 63 62 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXXGMX04 Devices | 12 46 47 48 8 41 46 55 53 55 55 55 55 63 62 62 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices | 12 46 47 48 18 46 52 44 45 53 57 52 46 62 62 64 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTA for dsPIC33EVXXXGMX02 Devices PORTB for dsPIC33EVXXXGMX02 Devices | 12 46 47 48 18 46 52 44 45 53 57 52 43 62 62 64 64 |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ |
| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ |
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| Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices PORTD for dsPIC33EVXXXGMX06 Devices PORTC for dsPIC33EVXXXGMX06 Devices PORTC for dsPIC33EVXXXGMX06 Devices PORTD for dsPIC33EVXXXGMX06 Devices PORTD for dsPIC33EVXXXGMX06 Devices | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ |

| Devices 50 PPS Output for dsPIC33EVXXXGM004/104 50 PPS Output for dsPIC33EVXXXGM006/106 51 Devices 51 PVM Generator 1 60 PVM Generator 3 61 PVM Generator 3 61 PWM Generator 3 61 PWM Generator 3 61 PWM Generator 3 61 PWT Receiver 49 SENT1 Receiver 49 SENT2 Receiver 49 SP11 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCCN3 (ADCx Control 1) 289 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON3 (ADCx Input Scan Select Liow) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 ADxCON2 (PWMx Alternate Dead-Time) 211 ADxCON3 (ADCx Control 3) 293 ADxCON | PPS Output for dsPIC33EVXXXGM002/102 | |
|--|---|-----|
| Devices 50 PPS Output for dsPIC33EVXXXGM006/106 51 Devices 51 PWM 60 PWM Generator 1 60 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCCN3 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 1) 289 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Input Scan Select Ligh) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON (Comparator 4 Control) 306 CMACON (Comparator X Control) 306 CMXTON (Comparator x Control) 307 CLKDIV (Clock Divisor) 28 | Devices | 50 |
| Devices 51 PVMM 60 PVMM Generator 1 60 PVMM Generator 2 61 PVMM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPH1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCX control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON2 (ADCx Control 3) 293 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 AUXCONK (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 | | 50 |
| PWM 60 PWM Generator 1 60 PWM Generator 2 61 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCX Input Channel 0 Select) 296 ADXCHS123 (ADCx Input 295 ADXCON1 (ADCX Control 1) 289 ADXCON3 (ADCx Control 3) 293 ADXCON3 (ADCx Control 3) 293 ADXCON4 (ADCx Control 4) 294 ADXCSSL (ADCx Input Scan Select High) 298 ADXCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Status) 303 CMXCON (Comparator X Mask Source Select Control) Select Control) 308 CO | | - 4 |
| PWM Generator 1 60 PWM Generator 2 61 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCx Input Channel 0 Select) 296 ADXCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCx Control 2) 291 ADXCON3 (ADCx Control 3) 293 ADXCON4 (ADCx Control 4) 294 ADXCSSH (ADCx Input Scan Select High) 298 ADXCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Atuxiliary Control) 219 CM4CON (Comparator 2 Control) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Filter Control) 310 CMxKCON (Comparator x Mask Gating Control) 312 CMMKON (Comparator x Kliter Sold 308 CORCON (Core Control) 271 </td <td></td> <td></td> | | |
| PWM Generator 2. 61 PWM Generator 3. 61 Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADXCSSL (ADCX Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Atternate Dead-Time) 211 AUXCON4 (Comparator X Control) 206 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Mask Source | | |
| PWM Generator 3. 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers. 43 UART1 and UART2 45 Registers ADXCHS0 (ADCX Input Channel 0 Select) 296 ADXCHS123 (ADCx Input Channel 0 Select) 296 ADXCON2 (ADCX Control 1) 289 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCX Control 3) 293 ADXCON3 (ADCx Control 4) 294 ADXCSSH (ADCx Input Scan Select High) 298 ADXCSS (ADCX Input Scan Select Low) 300 ALTDTSK (PWMx Atternate Dead-Time) 211 AUXCON1 (Comparator 4 Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Comparator x Control) 303 CMXCON (Comparator X Control) 312 CMMCON (Comparator x Filter Control) 312 CMMSKSCO (Comparator x Mask Source Select Control) Select Control) 308 CORCON (Core Control) 271 C | | |
| Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SP11 and SP12 45 System Control 53 Timers 43 UART1 and UART2 45 Registers 43 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCONS (ADCx Control 1) 289 ADxCON1 (ADCx Control 2) 291 ADxCON2 (ADCx Control 1) 289 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSL (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON4 (CMC Comparator X Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 306 CMXCON (Comparator X Mask 310 CMXMSKSCN (Comparator X Mask 310 CMxMSKSRC (Comparator X Mask 308 | PWM Generator 2 | 61 |
| SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCx Input Channels 1, 2, 3 Select) 296 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCx Control 2) 291 ADXCON3 (ADCx Control 2) 291 ADXCON4 (ADCx Control 2) 293 ADXCON4 (ADCx Control 3) 293 ADXCOSSH (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Autiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) CMXCKSCON (Comparator x Control, x = 1, 2, 3 or 5) CMXMSKCON (Comparator x Mask 303 Gating Control) 310 CMXMSKSCN (Comparator x Mask 308 CORCON (Core Control) 27 CTMU | PWM Generator 3 | 61 |
| SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Control) 304 CMxLETR (Comparator X Filter Control) 312 CMXMSKCON (Comparator X Mask Gating Control) X = 1, 2, 3 or 5) 304 CMxCON (Core Control) 310 CMxCON (Core Control) 312 CMMMSKS | Reference Clock | 53 |
| SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channel 0 Select) 296 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 1) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHACON (Comparator Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHACON (Comparator X Control) 218 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Control) 312 CMxMSKSRC (Comparator x Mask 303 Gating Control) 308 CORCON (Core Control) 27 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 | SENT1 Receiver | 49 |
| System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Aiternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CMACON (Comparator 4 Control) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMXFLTR (Comparator x Klask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON2 (CTMU Control 2) 282 CTMUCON3 (COMparator Voltage Refere | SENT2 Receiver | 49 |
| System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Aiternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CMACON (Comparator 4 Control) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMXFLTR (Comparator x Klask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON2 (CTMU Control 2) 282 CTMUCON3 (COMparator Voltage Refere | SPI1 and SPI2 | 45 |
| Timers. 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Input Scan Select High) 298 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) X = 1, 2, 3 or 5) 304 CMxMSKSRC (Comparator x Mask Gating Control) MXMSKSRC (Comparator x Mask Source Select Control) X = 1, 2, 3 or 5) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Current Control) 284 CTMUCON2 (CTMU Control 1) 281 CTMUC | | |
| UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) CMXCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 310 CMXMSKSCO (Comparator x Mask Source 388 Gating Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 1) 282 CTMUCON1 (CTMU Control 1) 281 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) <td></td> <td></td> | | |
| Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxMSKCON (Comparator x Mask Gating Control) CMXMSKSRC (Comparator x Mask Source Select Control) Select Control) 308 CORCON (Core Control 1) 281 CTMUCON1 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Vo | | |
| ADxCHS0 (ADCx Input 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSL (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON4 (Conparator Select Low) 300 ALTDTRx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) 304 CMXMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control | | |
| ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 4) 294 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON2 (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMTACON (Comparator X Control) 303 CMXCON (Comparator X Control) 303 CMXCON (Comparator x Control) 312 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Comparator x Mask 310 CMXMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 27 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 | | 200 |
| ADxCON1 (ADCx Control 1) | ADxCHS123 (ADCx Input | |
| ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 311 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Corparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 271 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 8-11 | Channels 1, 2, 3 Select) | 295 |
| ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 311 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Corparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 271 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 8-11 | ADxCON1 (ADCx Control 1) | 289 |
| ADxCON3 (ADCx Control 3) | | |
| ADxCON4 (ADCx Control 4) | ADxCON3 (ADCx Control 3) | 293 |
| ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 310 CMXMSKCON (Comparator x Mask 310 CMXMSKSRC (Comparator x Mask Source Select Control) Select Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 1) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) CONTOl 2) 316 CXBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 2) 265 CXBUFPNT3 (CANx Filters 4-7 Buffer Pointer 3) Buffer Pointer 3) 266 CxSUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) Buffer Pointer 4) 267 | | |
| ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Control) 312 CMxMSKCON (Comparator x Mask Gating Control) Gating Control) 310 CMXMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Control 2) 282 CTMUICON (CTMU Control 2) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 1) 264 CXBUFPNT3 (CANx Filters 8-11 < | | |
| ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxKLTR (Comparator x Kliter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) Gating Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON1 (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) Control 2) 316 CxBUFPNT2 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 3) 266 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) Buffer Pointer 4) 267 CxCFG1 (CANx Ba | | |
| AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Kontrol) 312 CMxMSKCON (Comparator x Mask Gating Control) CMxMSKSRC (Comparator x Mask Saling Control) Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 3) 266 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) Buffer Pointer 4) 267 CxCFG1 (CANx Bau | | |
| CHOP (PWMx Chop Clock Generator)207CLKDIV (Clock Divisor)128CM4CON (Comparator 4 Control)306CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKCON (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15316Buffer Pointer 3)266CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL2 (CANx Control 1)255CxCTRL2 (CANx FIFO Control)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) CMxMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON1 (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 30 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 30 Buffer Pointer 4) 267 | | 219 |
| CM4CON (Comparator 4 Control)306CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKSRC (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 3)266CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKSRC (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 3)266CxCFG2 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| CMxCON (Comparator x Control, x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFEN1 (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | | |
| x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source 308 Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 316 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 316 CxCFG2 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 < | | 303 |
| CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 316 CxBUFPNT3 (CANx Filters 8-11 316 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 316 CxCFG2 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262< | | |
| CMxMSKCON (Comparator x Mask Gating Control) 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG2 (CANx Baud Rate Configuration 1) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | x = 1, 2, 3 or 5) | 304 |
| Gating Control)310CMxMSKSRC (Comparator x Mask Source Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | CMxFLTR (Comparator x Filter Control) | 312 |
| Gating Control)310CMxMSKSRC (Comparator x Mask Source Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | CMxMSKCON (Comparator x Mask | |
| CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG2 (CANx Baud Rate Configuration 1) 263 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | | 310 |
| Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-38Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265CxBUFPNT3 (CANx Filters 8-118Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | 308 |
| CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 316 CxBUFPNT1 (CANx Filters 0-3 8 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 8 Buffer Pointer 2) 265 CxBUFPNT4 (CANx Filters 12-15 8 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 8 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 1) 255 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | , | |
| CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 265 CxBUFPNT4 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | | |
| CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 315 CVR2CON (Comparator Voltage Reference 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | | |
| CTXTSTAT (CPU W Register Context Status) | | |
| CVR1CON (Comparator Voltage Reference Control 1) | | |
| Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| Control 2)316CxBUFPNT1 (CANx Filters 0-39Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | Control 1) | 315 |
| CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | |
| CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | CxBUFPNT1 (CANx Filters 0-3 | |
| Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | 264 |
| CxBUFPNT3 (CANx Filters 8-11Buffer Pointer 3)CxBUFPNT4 (CANx Filters 12-15Buffer Pointer 4)CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1) | | |
| Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | 265 |
| CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264 | CxBUFPNT3 (CANx Filters 8-11 | |
| Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264 | | 266 |
| CxCFG1 (CANx Baud Rate Configuration 1) | CxBUFPNT4 (CANx Filters 12-15 | |
| CxCFG1 (CANx Baud Rate Configuration 1) | Buffer Pointer 4) | 267 |
| CxCFG2 (CANx Baud Rate Configuration 2) | CxCFG1 (CANx Baud Rate Configuration 1) | 262 |
| CxCTRL1 (CANx Control 1) | | |
| CxCTRL2 (CANx Control 2) | | |
| CxEC (CANx Transmit/Receive Error Count) | CxCTRI 2 (CANx Control 2) | 256 |
| CxFCTRL (CANx FIFO Control) | | |
| CxFEN1 (CANx Acceptance Filter Enable 1) | | |
| | | |
| CXFIFU (CANX FIFU STATUS) | | |
| | GARTIFU (GAINA FIFU STATUS) | 259 |