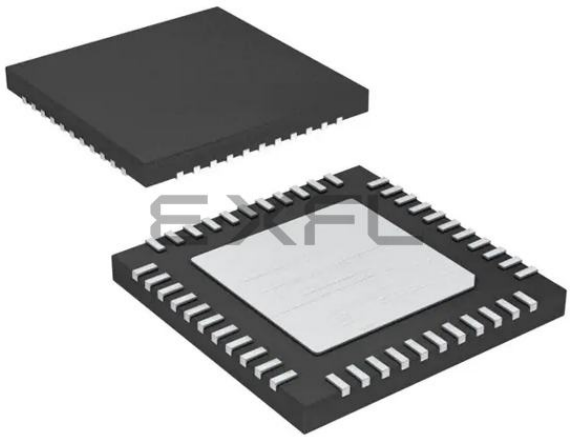
Microchip Technology - DSPIC33EV128GM004T-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm004t-i-ml

TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA<12:7>						—	—	TRISA4	—	—	TRISA<1:0>		1F93
PORTA	0E02	—	—	—	RA<12:7>						—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	—	—	—	LATA<12:7>						—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	—	—	—	ODCA<12:7>						—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	—	—	—	CNIEA<12:7>						—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	—	—	—	CNPUA<12:7>						—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	—	—	—	CNPDA<12:7>						—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	—	—	—	ANSA<12:9>				—	ANSA7	—	—	ANSA4	—	—	ANSA<1:0>		1E93
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA<10:7>				—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	RA<10:7>				—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	LATA<10:7>				—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	ODCA<10:7>				—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	CNIEA<10:7>				—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	CNPUA<10:7>				—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	CNPDA<10:7>				—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	ANSA<10:9>		—	ANSA7	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Reset"** (DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset
  - Illegal Address Mode Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 "Memory Organization"** of this device data sheet for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in the other sections of this device data sheet.

Note: The status bits in the RCON register should be cleared after they are read. Therefore, the next RCON register value after a device Reset is meaningful.

Note: In all types of Resets, to select the device clock source, the contents of OSCCON are initialized from the FNOSCx Configuration bits in the FOSCSEL Configuration register.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
11 = One-Shot Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous Ping-Pong modes are enabled
01 = One-Shot Ping-Pong modes are disabled
00 = Continuous Ping-Pong modes are disabled

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PAD<15:0>:** DMA Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT<13:8>(2)					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT<13:0>:** DMA Transfer Count Register bits(2)

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

REGISTER 22-5: CxFIFO: CANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit
1 = Edge 1 is edge-sensitive
0 = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = FOSC
1110 = OSCI pin
1101 = FRC Oscillator
1100 = BFRC Oscillator
1011 = Internal LPRC Oscillator
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = Reserved
0100 = Reserved
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1 module
0000 = TMR1 module

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the edge source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the edge source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit
1 = Edge 2 is edge-sensitive
0 = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge response
0 = Edge 2 is programmed for a negative edge response

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(3)

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator x Reference Select bit (VIN+ input)(1)

1 = VIN+ input connects to the internal CVREFIN voltage
0 = VIN+ input connects to the CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Op Amp/Comparator x Channel Select bits(1)

11 = Inverting input of op amp/comparator connects to the CxIN4- pin
10 = Inverting input of op amp/comparator connects to the CxIN3- pin
01 = Inverting input of op amp/comparator connects to the CxIN2- pin
00 = Inverting input of op amp/comparator connects to the CxIN1- pin

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

2: The op amp and the comparator can be used simultaneously in these devices. The OPAEN bit only enables the op amp while the comparator is still functional.

3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator x Event bit, CEVT (CMxCON<9>), and the Comparator Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(2)

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator 4 Reference Select bit (VIN+ input)(1)

1 = VIN+ input connects to the internal CVREFIN voltage
0 = VIN+ input connects to the C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator 4 Channel Select bits(1)

11 = VIN- input of comparator connects to the C4IN4- pin
10 = VIN- input of comparator connects to the C4IN3- pin
01 = VIN- input of comparator connects to the C4IN2- pin
00 = VIN- input of comparator connects to the C4IN1- pin

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

26.2 Comparator Voltage Reference Registers

REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF1O Pin) bit
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from the CVREF1O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = CVREFIN = CVREF+
0 = CVREFIN is generated by the resistor network

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	Description
OSCIOFNC	FOSC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
IOL1WAY	FOSC	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
FCKSM<1:0>	FOSC	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
PLLKEN	FOSC	PLL Lock Wait Enable bit 1 = Clock switches to the PLL source; will wait until the PLL lock signal is valid 0 = Clock switch will not wait for PLL lock
WDTPS<3:0>	FWDT	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
WDTPRE	FWDT	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
FWDTEN<1:0>	FWDT	Watchdog Timer Enable bits 11 = WDT is enabled in hardware 10 = WDT is controlled through the SWDTEN bit 01 = WDT is enabled only while device is active and disabled in Sleep; the SWDTEN bit is disabled 00 = WDT and the SWDTEN bit are disabled
WINDIS	FWDT	Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode
WDTWIN<1:0>	FWDT	Watchdog Timer Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
BOREN	FPOR	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
ICS<1:0>	FICD	ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use
DMTIVT<15:0>	FDMTINTVL	Lower 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits
DMTIVT<31:16>	FDMTINTVH	Upper 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits
DMTCNT<15:0>	FDMTCNTL	Lower 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits

FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

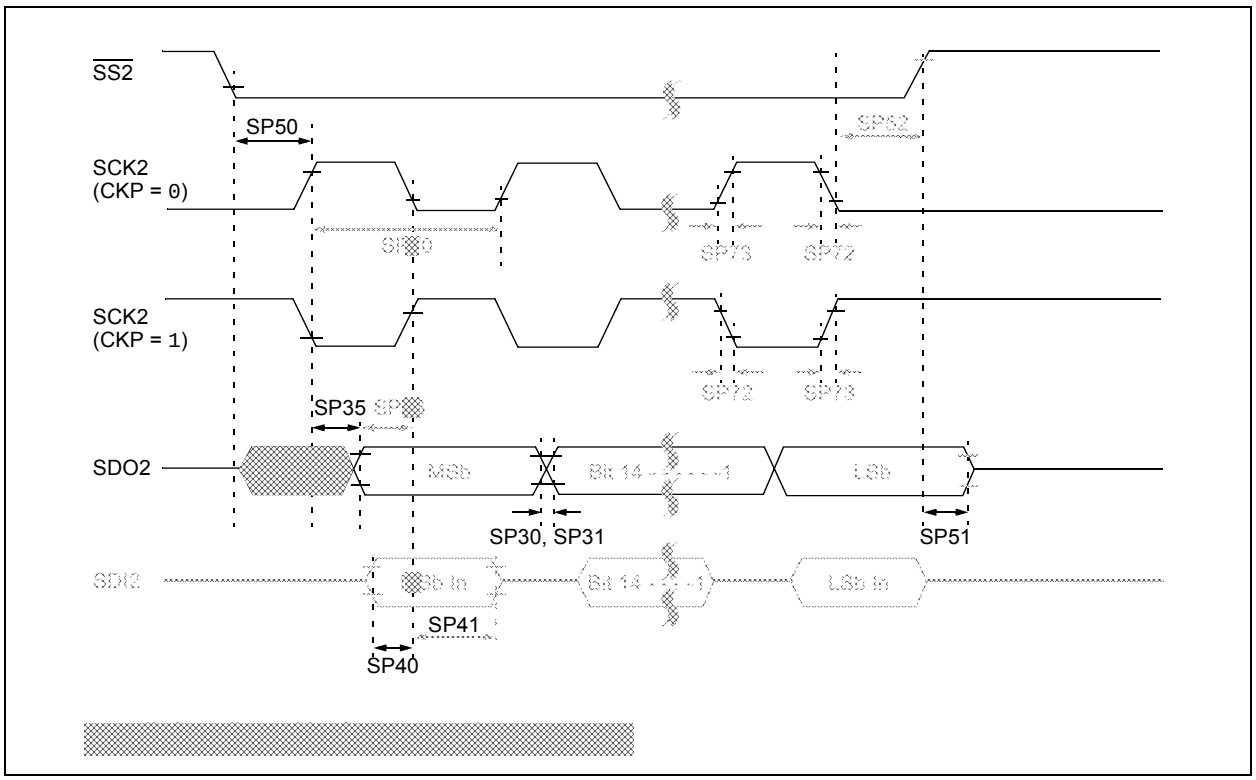


FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

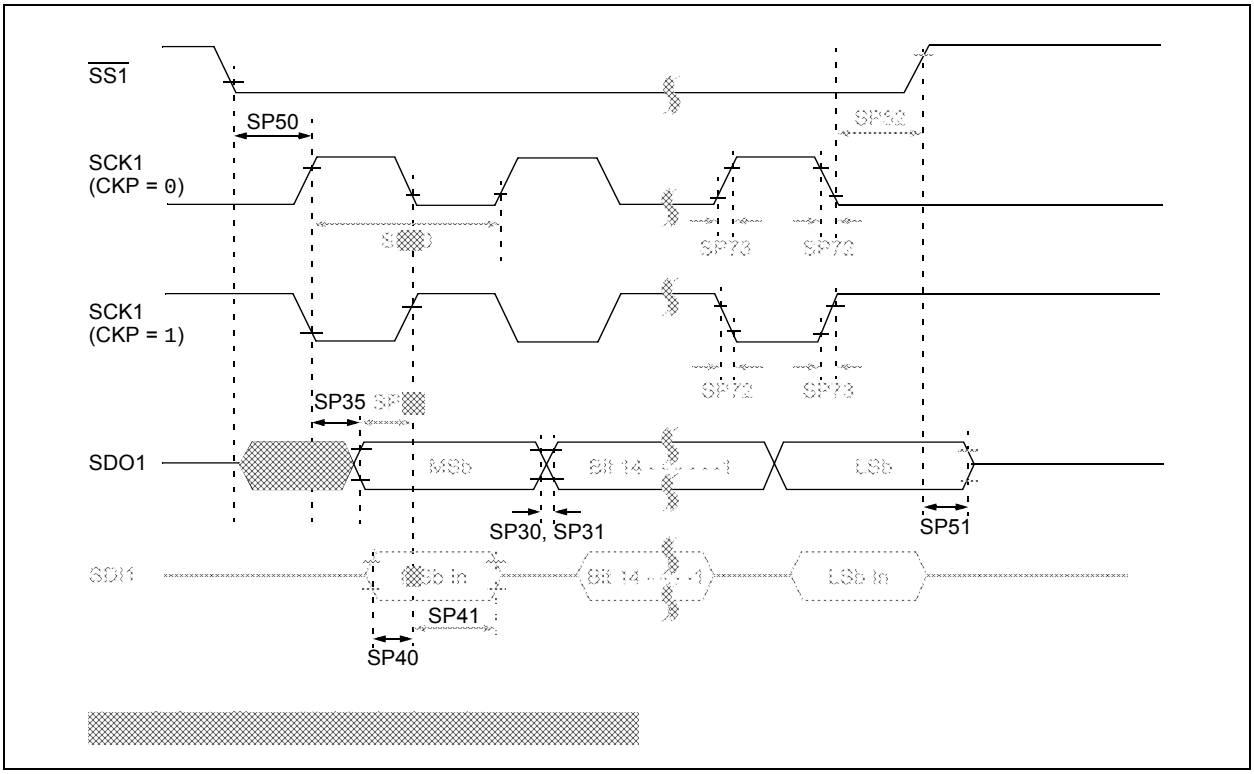
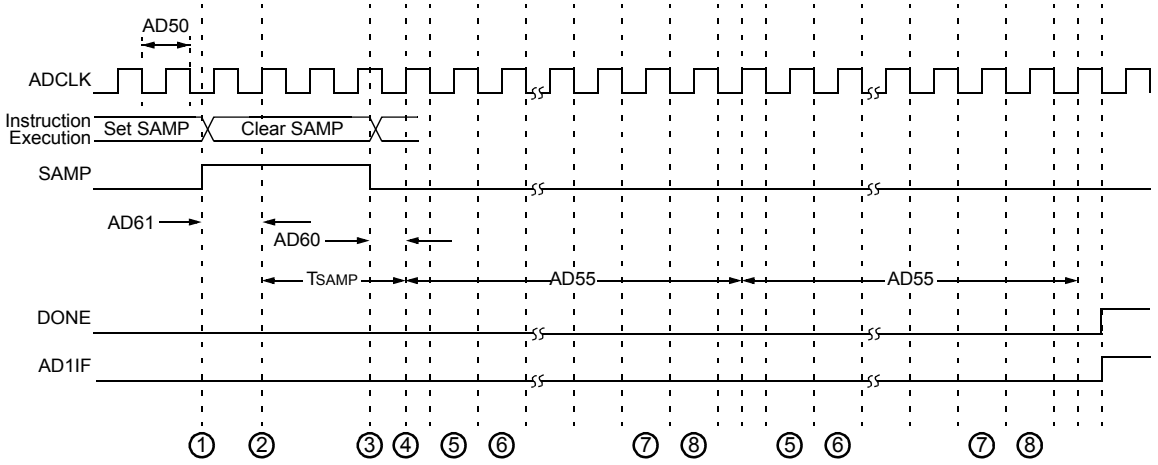


FIGURE 30-35: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



① – Software sets ADxCON1. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Software clears ADxCON1. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

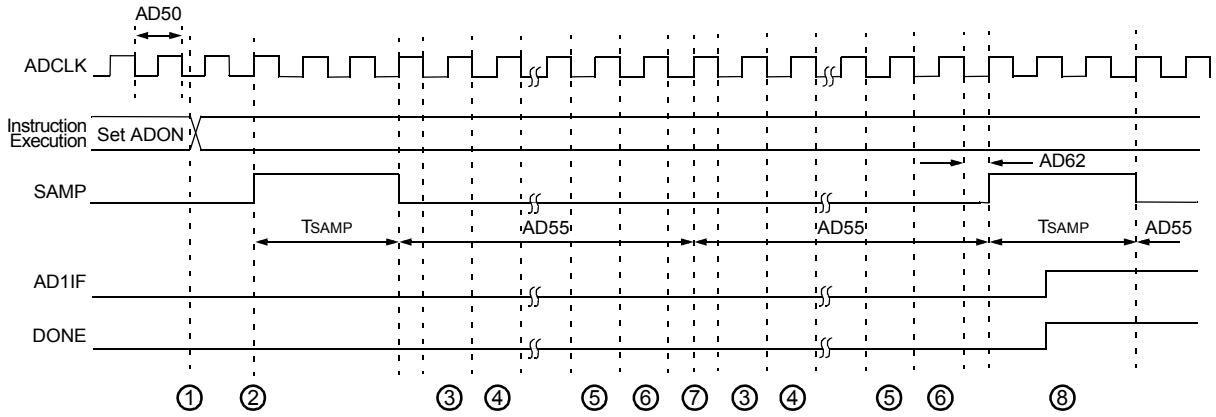
⑤ – Convert bit 9.

⑥ – Convert bit 8.

⑦ – Convert bit 0.

⑧ – One TAD for end of conversion.

FIGURE 30-36: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



① – Software sets ADxCON1. ADON to start ADC operation.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Convert bit 9.

④ – Convert bit 8.

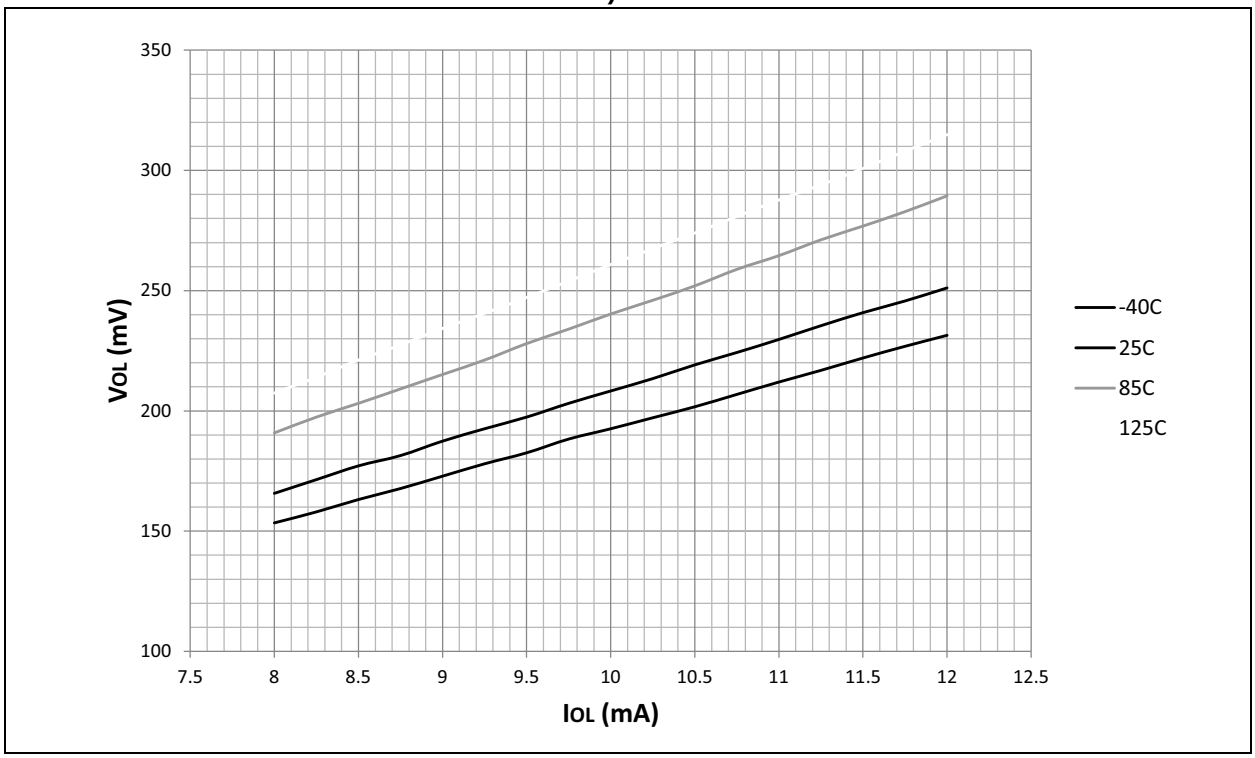
⑤ – Convert bit 0.

⑥ – One TAD for end of conversion.

⑦ – Begin conversion of next channel.

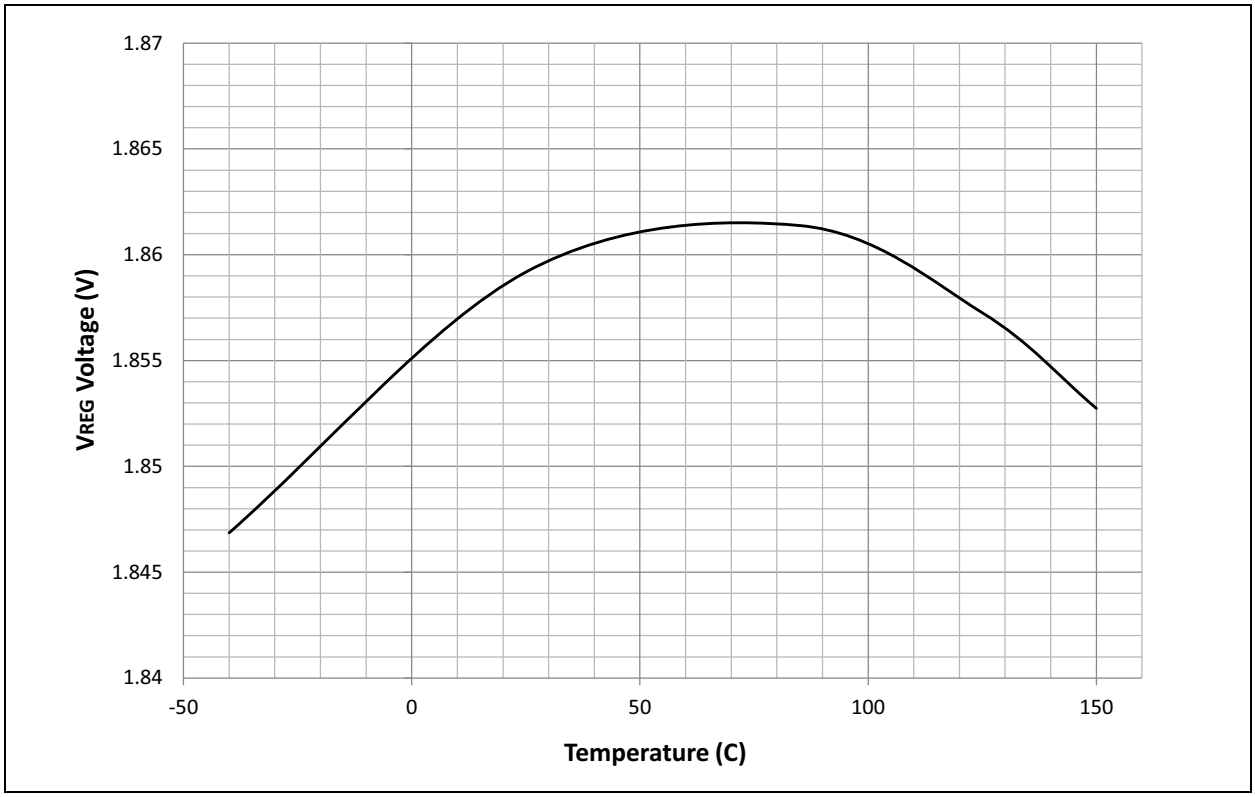
⑧ – Sample for time specified by SAMC<4:0>.

FIGURE 32-33: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



32.11 VREG

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE



32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. VCM

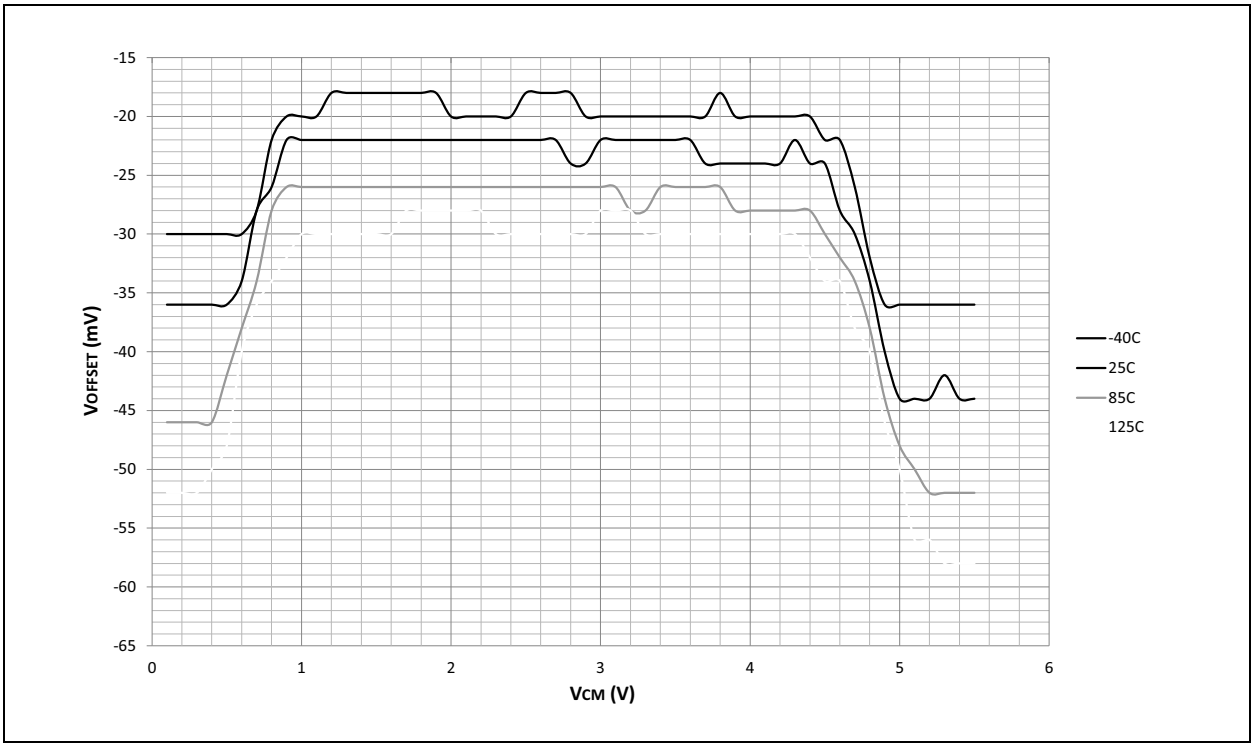
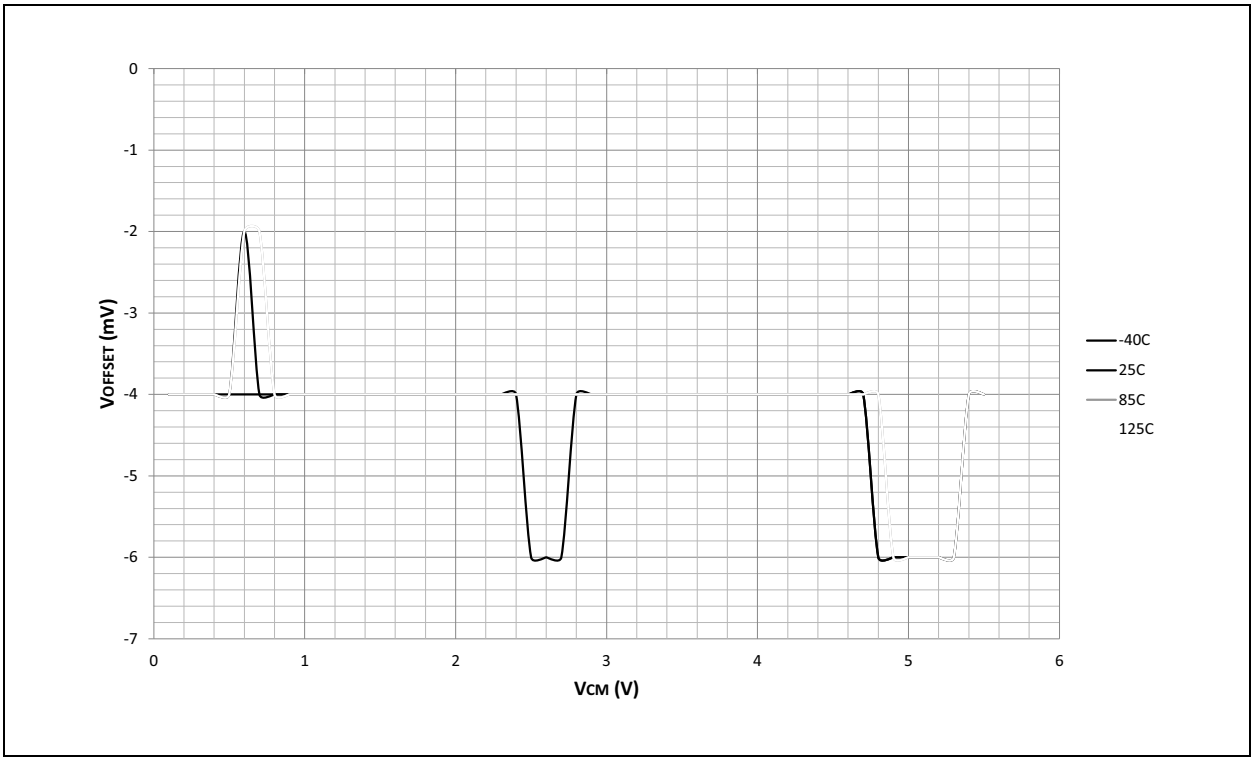


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. VCM OP AMP OFFSET



33.4 IPD

FIGURE 33-13: TYPICAL IPD vs. VDD

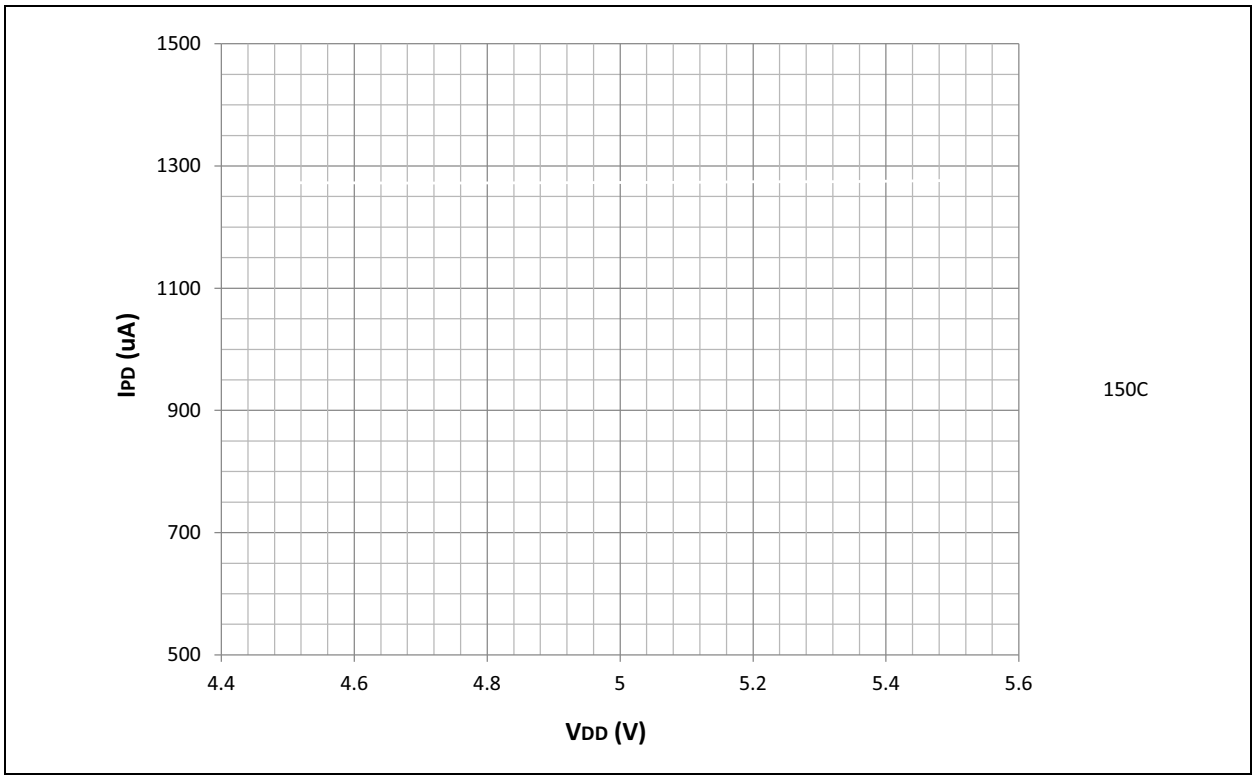
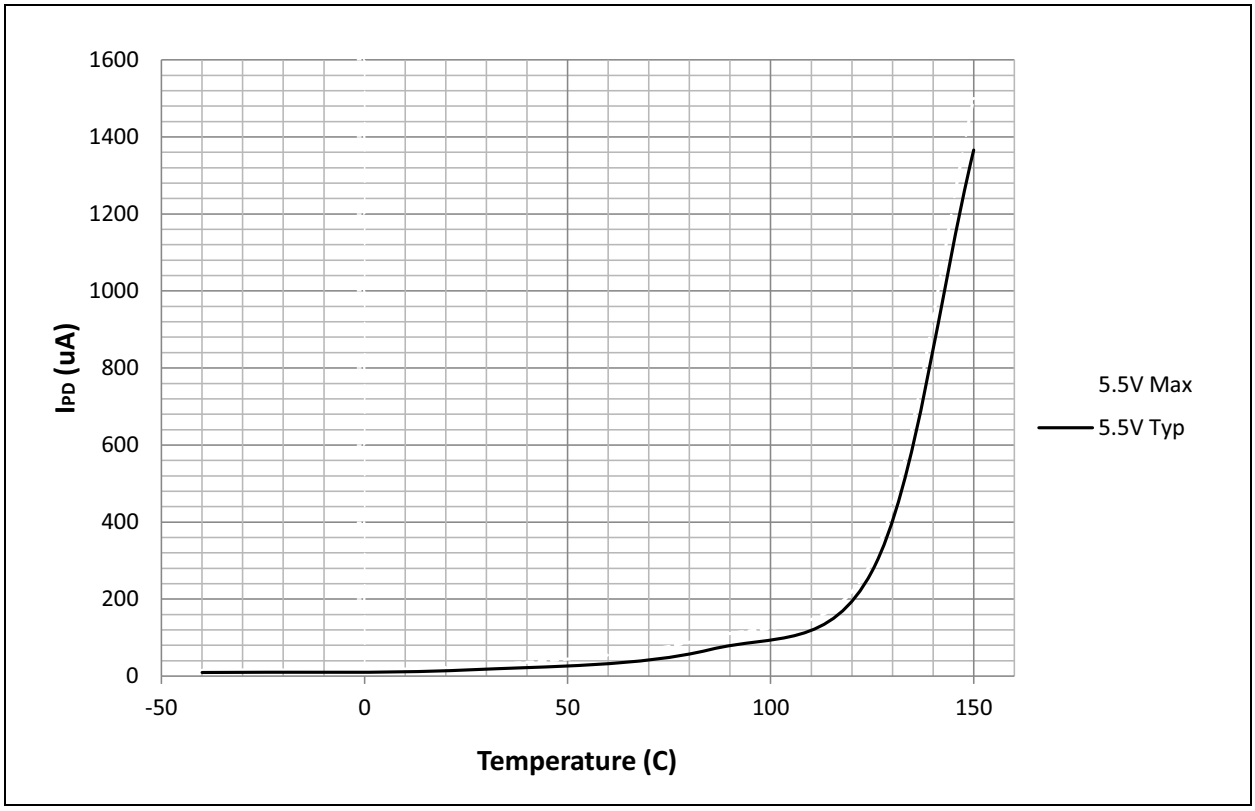
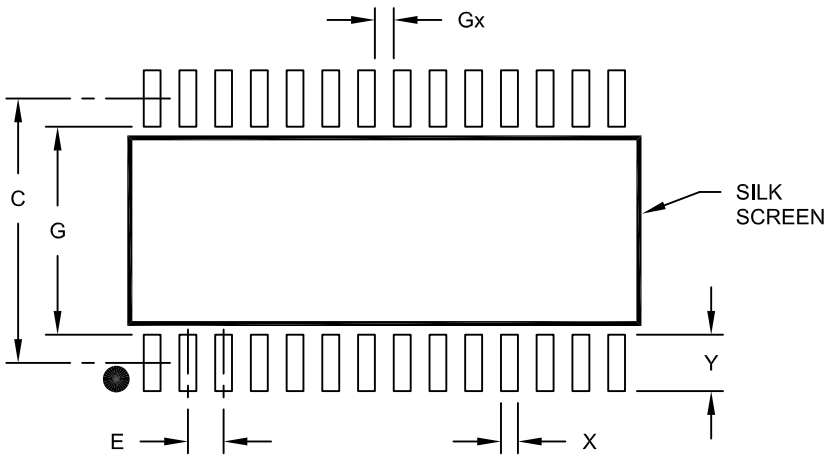


FIGURE 33-14: TYPICAL/MAXIMUM IPD vs. TEMPERATURE



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

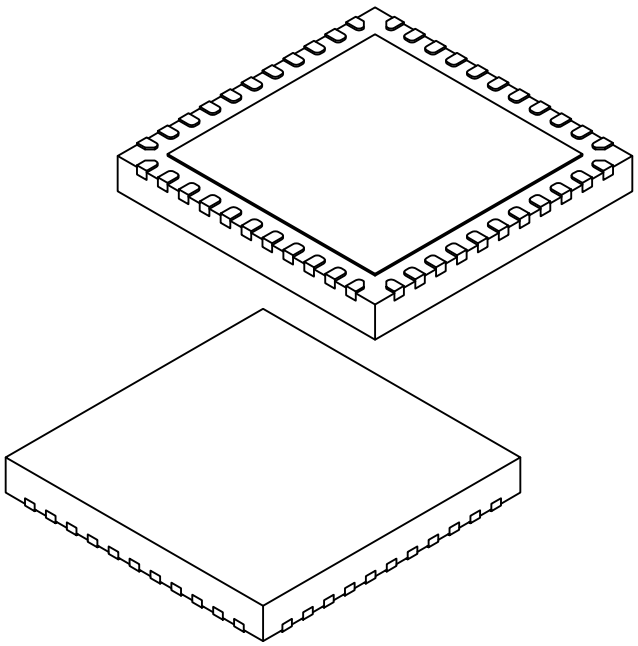
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2

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