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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm102-i-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

### 2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16-bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)
- (see Section 2.2 "Decoupling Capacitors")
   VCAP
- (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

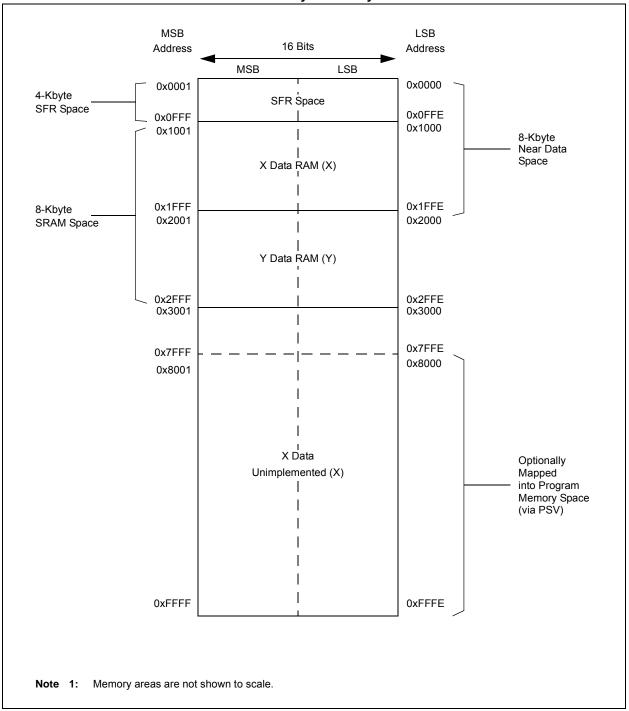
Note: The AVDD and AVSS pins must be connected, regardless of the ADC voltage reference source.

## 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of 0.1  $\mu$ F (100 nF), 10V-20V is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the Printed Circuit Board (PCB): The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of  $0.01 \ \mu\text{F}$  to  $0.001 \ \mu\text{F}$ . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example,  $0.1 \ \mu\text{F}$  in parallel with  $0.001 \ \mu\text{F}$ .
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.



## FIGURE 4-7: DATA MEMORY MAP FOR 64-Kbyte/128-Kbyte DEVICES<sup>(1)</sup>

## 4.3 Special Function Register Maps

#### TABLE 4-1: CPU CORE REGISTER MAP

IADLL 4	- • •			LOISIL														
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Reset s
W0	0000								W0 (W	REG)								0000
W1	0002								Ŵ									0000
W2	0004								W	2								0000
W3	0006								W	3								0000
W4	0008								W	4								0000
W5	000A								W	5								0000
W6	000C								We	6								0000
W7	000E		W7 0000											0000				
W8	0010		W8 0000											0000				
W9	0012								W	9								0000
W10	0014								W1	0								0000
W11	0016								W1	1								0000
W12	0018								W1	2								0000
W13	001A								W1	3								0000
W14	001C								W1	4								0000
W15	001E								W1	5								0800
SPLIM	0020								SPL	IM								xxxx
ACCAL	0022								ACC	AL								xxxx
ACCAH	0024								ACC	AH								xxxx
ACCAU	0026			Sig	n Extension	of ACCA<3	9>						ACC	CAU				xxxx
ACCBL	0028								ACC	BL								xxxx
ACCBH	002A								ACC	BH								xxxx
ACCBU	002C			Sig	n Extension	of ACCB<3	9>						ACC	CBU				xxxx
PCL	002E						Pro	ogram Cou	nter Low We	ord Register	r						_	0000
PCH	0030	_	_	_	_	_	_	_	_	_		F	Program Cou	inter High W	ord Registe	r		0000
DSRPAG	0032	_	_	_	_	_	_				Dat	a Space Re	ad Page Reg	gister				0001
DSWPAG	0034	—	_			—	_	_				Data Spa	ce Write Pag	e Register				0001
RCOUNT	0036							REPEAT LC	op Counter	Register							0	xxxx
DCOUNT	0038							DC	OUNT<15:1	>							0	xxxx
DOSTARTL	003A							DOS	TARTL<15	:1>							0	xxxx
DOSTARTH	003C	_	_		_	_		_	_	_	_			DOSTART	H<5:0>			00xx
DOENDL	003E							DO	ENDL<15:1	>							—	xxxx
Lanandi				- unimalar														

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### REGISTER 5-5: NVMSRCADRH: NVM DATA MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	_	_	—	_	—	—
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMSRCAD	)R<23:16>			
bit 7							bit 0
Legend:							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

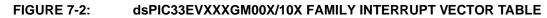
bit 7-0 NVMSRCADRH<23:16>: Data Memory Upper Address bits

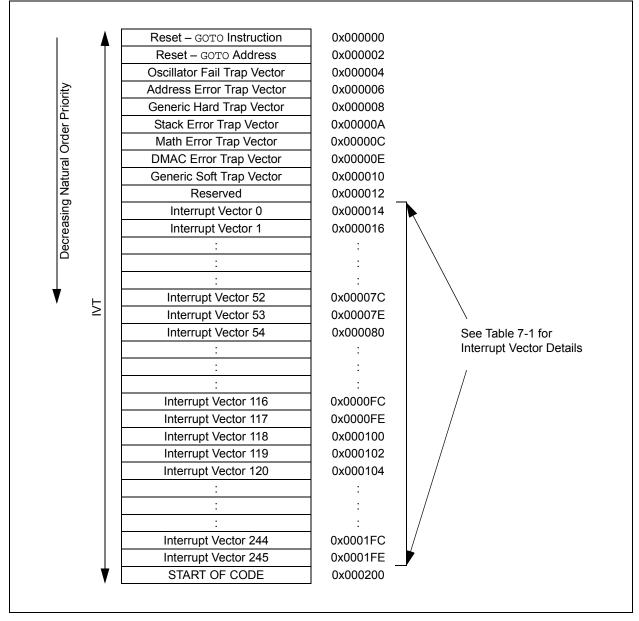
#### REGISTER 5-6: NVMSRCADRL: NVM DATA MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMSRC	CADR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	r-0
		NV	MSRCADR<	7:1>			—
bit 7							bit C
Legend:		r = Reserved	bit				
R = Readable b	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-1 NVMSRCADRL<15:1>: Data Memory Lower Address bits

bit 0 Reserved: Maintain as '0'





## 9.1 CPU Clocking System

The dsPIC33EVXXXGM00X/10X family of devices provides the following six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

For instruction execution speed or device operating frequency, FCY, see Equation 9-1.

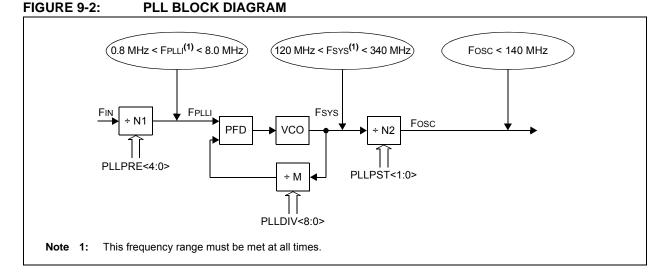
# EQUATION 9-1: DEVICE OPERATING FREQUENCY

#### FCY = FOSC/2

Figure 9-2 provides the block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FSYS).



## EQUATION 9-2: Fosc CALCULATION

$$FOSC = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV < 8:0 > + 2)}{(PLLPRE < 4:0 > + 2) \times 2(PLLPOST < 1:0 > + 1)}\right)$$

Where: *N*1 = *PLLPRE*<4:0> + 2 *N*2 = 2 x (*PLLPOST*<1:0> + 1) *M* = *PLLDIV*<8:0> + 2

## EQUATION 9-3: Fvco CALCULATION

$$FSYS = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV < 8:0 > + 2)}{(PLLPRE < 4:0 > + 2)}\right)$$

## 11.6 High-Voltage Detect (HVD)

dsPIC33EVXXXGM00X/10X devices contain High-Voltage Detection (HVD) which monitors the VCAP voltage. The HVD is used to monitor the VCAP supply voltage to ensure that an external connection does not raise the value above a safe level (~2.4V). If high core voltage is detected, all I/Os are disabled and put in a tristate condition. The device remains in this I/O tri-state condition as long as the high-voltage condition is present.

## 11.7 I/O Helpful Tips

- 1. In some cases, certain pins, as defined in Table 30-10 under "Injection Current", have internal protection diodes to VDD and Vss. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention; for example, AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
- 5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specifications. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

VOH = 4.4V at IOH = -8 mA and VDD = 5V

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current, <12 mA, is technically permitted. For more information, refer to the VOH/ IOH specifications in **Section 30.0 "Electrical Characteristics"**.

#### REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	_	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			T2CK	R<7:0>			
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	<b>d as</b> '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 15-8 Unimplemented: Read as '0'

bit 7-0 **T2CKR<7:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers) 10110101 = Input tied to RPI181 •

• 00000001 = Input tied to CMP1 00000000 = Input tied to Vss

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SENT	1R<7:0>			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—		—	—	—	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, rea	<b>d as</b> '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	(see Table 1	<b>0&gt;:</b> Assign SEN 1-2 for input pin Input tied to RF	selection nui		esponding RP	n Pin bits	
		Input tied to Cl Input tied to Vs					

### REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

#### REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0							
0-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	_	—	—
bit 15							bit 8
DANO	DAMO	DAMO					D/M/ O
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SENT2	2R<7:0>			
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	<b>as</b> '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-8	Unimplemer	tod. Dood on "	<u>,</u>				
	e inipierier	neau as	J				
bit 7-0	SENT2R<7:0 (see Table 11 10110101 = 00000001 =	<ul> <li>Input tied to CN</li> <li>Input tied to CN</li> <li>Input tied to CN</li> </ul>	T Module Inp selection num P181 /IP1		esponding RPn	Pin bits	

### REGISTER 17-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPE	R<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
			PTPE	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	<b>d as</b> '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

#### REGISTER 17-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		SEVTC	MP<15:8>			
						bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		SEVTO	CMP<7:0>			
						bit 0
t	W = Writable bi	t	U = Unimpler	nented bit, rea	<b>d as</b> '0'	
R	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
		R/W-0 R/W-0 t W = Writable bi	SEVTC R/W-0 R/W-0 R/W-0 SEVTC	SEVTCMP<15:8>           R/W-0         R/W-0         R/W-0           SEVTCMP<7:0>         SEVTCMP<7:0>	SEVTCMP<15:8>           R/W-0         R/W-0         R/W-0           SEVTCMP<7:0>         SEVTCMP<7:0>	SEVTCMP<15:8>           R/W-0         R/W-0         R/W-0         R/W-0           SEVTCMP<7:0>         SEVTCMP<7:0>

bit 15-0 SEVTCMP<15:0>: Special Event Compare Count Value bits

### REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	_			DTRx	<13:8>				
bit 15							bit		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			DTR	x<7:0>					
bit 7							bit		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		

bit 15-14Unimplemented: Read as '0'bit 13-0DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

#### REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—		ALTDTRx<13:8>							
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
ALTDTRx<7:0>									
bit 7							bit 0		

Legend:					
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
	_	_	_	_	_	—	_				
bit 15							bit 8				
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN				
bit 7							bit 0				
Legend:											
R = Readal	ble bit	W = Writable	oit	U = Unimplem	nented bit, read	<b>l as</b> '0'					
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea		x = Bit is unkn	own				
bit 15-7	Unimplemen	ted: Read as 'o	)'								
bit 6	PCIE: Stop C	ondition Interru	pt Enable bit (	I <sup>2</sup> C Slave mode	only).						
	1 = Enables interrupt on detection of Stop condition										
bit 5	<ul> <li>0 = Stop detection interrupts are disabled</li> <li>SCIE: Start Condition Interrupt Enable bit (I<sup>2</sup>C Slave mode only)</li> </ul>										
DIL D			• •	or Restart condi	• ·						
		ction interrupts									
bit 4			•	ave mode only)							
				and an ACK is g		received addre	ess/data byte,				
				/ if the RBF bit = ted when I2CO							
bit 3		x Hold Time Se									
				after the falling							
				after the falling	-						
bit 2				Enable bit (I <sup>2</sup> C		• ·					
		• •		mpled low whe Detection mode			•				
	sequences.	C				in ing the circ					
		collision interr									
bit 1		ess Hold Enable	•								
bit i			•	x for a matchir	na received ad	ldress byte: the	e SCLREL bit				
	(I2CxCO	N1<12>) will be	e cleared and t	he SCLx will be							
		holding is disat									
bit 0		Hold Enable bit		ode only) for a received da	ata huto: clava	hardwara clear					
		CON1<12>) and			aia Dyle, Slave	naruware ciears	SUIC SOLKEL				
		ding is disabled									

#### REGISTER 19-2: I2CxCON2: I2Cx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT		
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0		
EDG2MOD	2MOD EDG2POL EDG2SEL3 EDG2SEL2 EDG2SEL1 EDG2SEL0 —								
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15		Edge 1 Edge Sa		Selection bit					
	•	s edge-sensitive							
hit 11	-	s level-sensitive							
bit 14		dge 1 Polarity		dae response					
	Ų	s programmed f		<b>v</b> .					
bit 13-10	-	:0>: Edge 1 So	-	•					
	1111 = Fosc	•							
	1110 <b>= OSCI</b>	pin							
	1101 <b>= FRC</b> (								
	1100 = BFRC	COSCIIIator	otor						
	1011 - Intern 1010 = Reser		aloi						
	1001 = Reser								
	1000 <b>= Rese</b> r								
	0111 = Reser								
	0110 = Reser								
	0100 = Resei								
	0011 = CTED	01 pin							
	0010 = CTED								
	0001 = OC1 I 0000 = TMR1								
bit 9		Edge 2 Status b	.i+						
bit 9		-		vritten to contro	ol the edge sour	rce			
	1 = Edge 2 h				ine eage soul				
		as not occurred	ł						
bit 8	EDG1STAT: E	Edge 1 Status b	it						
			1 and can be v	vritten to contro	ol the edge sour	rce.			
	1 = Edge 1 h		J						
hit 7	-	as not occurred		Coloction hit					
bit 7		Edge 2 Edge Sa edge-sensitive		Selection Dit					
	•	level-sensitive							
bit 6	-	dge 2 Polarity							
		s programmed f		dge response					
		programmed f							

## REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2

## **REGISTER 24-7:** ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH<sup>(2)</sup> (CONTINUED)

- bit 1 CSS17: ADCx Input Scan Selection bit 1 = Selects ANx for input scan
  - 0 = Skips ANx for input scan
- bit 0 CSS16: ADCx Input Scan Selection bit
  - 1 = Selects ANx for input scan
    - 0 = Skips ANx for input scan
- **Note 1:** If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.
  - 2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

#### TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

Standard Operating Conditions: 4.5V to 5.5V

AC CH	AC CHARACTERISTICS			(unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Charac	Characteristic <sup>(1)</sup>		Тур.	Max.	Units	Conditions	
TB10	T⊤xH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N		_	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)	
TB11	ΤτxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N		_	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)	
TB15	ΤτχΡ	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_	_	ns	N = Prescaler Value (1, 8, 64, 256)	
TB20	TCKEXT- MRL	Delay from I Clock Edge Increment	External TxCK to Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

#### TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 4.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Chara	cteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
TC10	ТтхН	TxCK High Time	Synchronous	Tcy + 20	—	_	ns	Must also meet Parameter TC15
TC11	ΤτxL	TxCK Low Time	Synchronous	Tcy + 20	_	—	ns	Must also meet Parameter TC15
TC15	ΤτχΡ	TxCK Input Period	Synchronous, with Prescaler	2 Tcy + 40	_	—	ns	N = Prescaler Value (1, 8, 64, 256)
TC20	TCKEXT- MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1:	These parameters are characterized but not tested in manufacturing.

# TABLE 30-44:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHA	AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions		
SP70	FscP	Maximum SCK1 Input Frequency		_	25	MHz	See Note 3		
SP72	TscF	SCK1 Input Fall Time	—			ns	See Parameter DO32 and <b>Note 4</b>		
SP73	TscR	SCK1 Input Rise Time	_			ns	See Parameter DO31 and <b>Note 4</b>		
SP30	TdoF	SDO1 Data Output Fall Time	—	_	_	ns	See Parameter DO32 and <b>Note 4</b>		
SP31	TdoR	SDO1 Data Output Rise Time	—			ns	See Parameter DO31 and <b>Note 4</b>		
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns			
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	_	_	ns			
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20			ns			
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	_	_	ns			
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	_	ns			
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	_	50	ns	See Note 4		
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40		_	ns	See Note 4		

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min. <sup>(1)</sup>	Тур.	Max.	Units	Conditions	
HDO16	Vol	Output Low Voltage 4x Sink Driver Pins <sup>(2)</sup>			0.4	V	Iol = 8.8 mA, VDD = 5.0V	
HDO10	Vol	Output Low Voltage 8x Sink Driver Pins <sup>(3)</sup>	_		0.4	V	IOL = 10.8 mA, VDD = 5.0V	
HDO26	Vон	Output High Voltage 4x Sink Driver Pins <sup>(2)</sup>	Vdd - 0.6		_	V	Іон = -8.3 mA, Vdd = 5.0V	
HDO20	Vон	Output High Voltage 8x Sink Driver Pins	Vdd - 0.6	_	_	V	Іон = -12.3 mA, Vdd = 5.0V	

#### TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x sink driver pins (see below).

**3:** Includes the pins, such as RA3, RA4 and RB<15:10> for 28-pin devices, RA3, RA4, RA9 and RB<15:10> for 44-pin devices, and RA4, RA7, RA9, RB<15:10> and RC15 for 64-pin devices.

#### TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR

DC CHA	DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature				
Param No.	Symbol	Characteristic	Min. <sup>(1)</sup>	Тур.	Max.	Units	Conditions	
HBO10	VBOR	BOR Event on VDD Transition High-to-Low	4.15	4.285	4.4	V	VDD (see Note 2, Note 3 and Note 4)	

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

- **2:** The VBOR specification is relative to the VDD.
- **3:** The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but is not characterized.
- 4: The start-up VDD must rise above 4.6V.

#### TABLE 31-11: DC CHARACTERISTICS: PROGRAM MEMORY

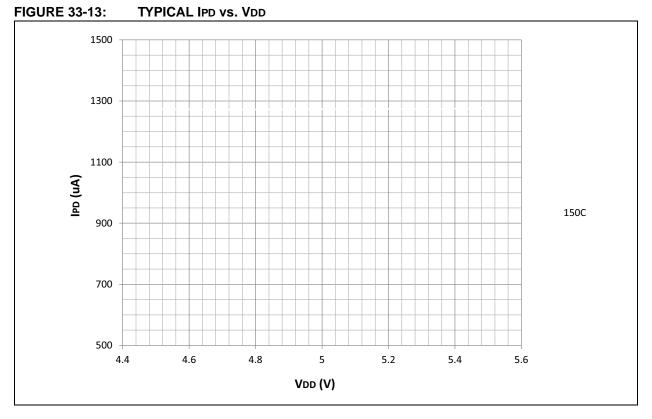
DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature					
Param No.	Symbol	ol Characteristic <sup>(1)</sup> Min. Typ. Max. Units		Conditions				
		Program Flash Memory						
HD130	Eр	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C <sup>(2)</sup>	
HD134	Tretd	Characteristic Retention	20		—	Year	1000 E/W cycles or less and no other specifications are violated	

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

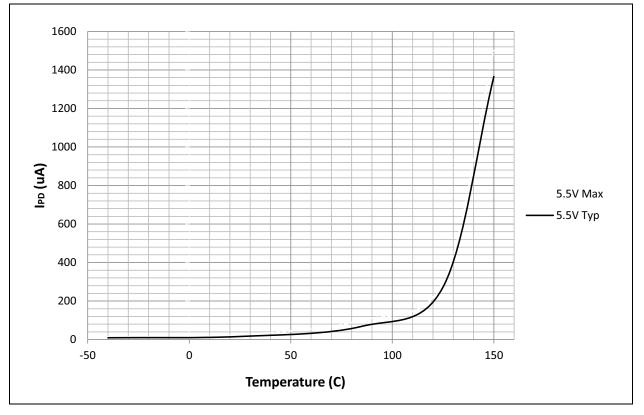
**2:** Programming of the Flash memory is allowed up to +150°C.

## dsPIC33EVXXXGM00X/10X FAMILY

#### 33.4 IPD

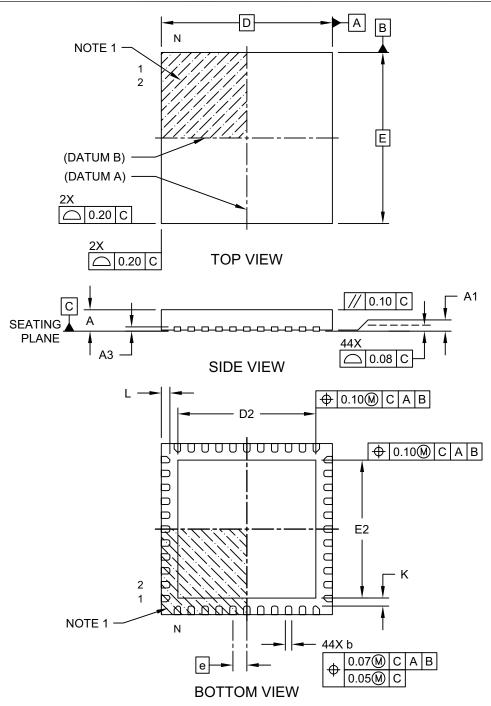






## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





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Referenced Sources           Register Maps           ADC1           CAN1 (WIN (C1CTRL) = 0 or 1)           CAN1 (WIN (C1CTRL) = 0)           CAN1 (WIN (C1CTRL) = 1)           CAN1 (WIN (C1CTRL) = 1)           Configuration Words           CPU Core           CTMU           DMAC           DMT           I2C1	46 47 48 318 41 46 59 52 44
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core CTMU DMAC DMAC DMT I2C1 Input Capture 1 through Input Capture 4	46 47 48 318 41 46 59 52 44 44
Referenced Sources           Register Maps           ADC1           CAN1 (WIN (C1CTRL) = 0 or 1)           CAN1 (WIN (C1CTRL) = 0)           CAN1 (WIN (C1CTRL) = 1)           CAN1 (WIN (C1CTRL) = 1)           Configuration Words           CPU Core           CTMU           DMAC           DMT           I2C1	46 47 48 318 41 46 59 52 44 44 55
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller	46 47 48 41 46 59 52 44 44 55 53
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core. CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM	46 47 48 41 46 59 52 44 44 45 55 53 58
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Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core. CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator. Output Compare Peripheral Input Remap	46 47 48 318 41 46 59 52 44 44 44 55 53 58 57 52 54
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Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX06 Devices	46 47 48 318 41 46 59 52 44 44 45 53 53 53 52 54 52 54 62 62
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTA for dsPIC33EVXXXGMX04 Devices	46 47 48 318 41 46 59 52 44 44 55 53 53 57 52 54 63 62 62 64
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices	46 47 48 318 41 46 59 52 44 44 44 55 53 53 52 54 52 54 63 62 64 64
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices	46 47 48 318 41 46 59 52 44 44 45 53 53 57 52 54 63 62 64 64 63
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices	46 47 48 318 41 46 59 52 44 44 55 53 53 52 54 52 54 63 62 64 63 65
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX04 Devices	46 47 48 318 41 46 59 52 44 45 53 53 53 57 52 54 63 62 64 63 65
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX06 Devices         PORTD for dsPIC33EVXXXGMX06 Devices	46 47 48 318 41 46 59 52 44 44 55 53 53 57 52 54 63 62 64 63 65 65 66
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX06 Devices         PORTD for dsPIC33EVXXXGMX06 Devices         PORTD for dsPIC33EVXXXGMX06 Devices	46 47 48 318 41 46 59 52 44 44 55 53 53 57 52 54 63 62 64 64 65 66 66
Referenced Sources         Register Maps         ADC1         CAN1 (WIN (C1CTRL) = 0 or 1)         CAN1 (WIN (C1CTRL) = 0)         CAN1 (WIN (C1CTRL) = 1)         Configuration Words         CPU Core         CTMU         DMAC         DMT         I2C1         Input Capture 1 through Input Capture 4         Interrupt Controller         NVM         Op Amp/Comparator         Output Compare         Peripheral Input Remap         PMD         PORTA for dsPIC33EVXXXGMX02 Devices         PORTA for dsPIC33EVXXXGMX04 Devices         PORTB for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX04 Devices         PORTC for dsPIC33EVXXXGMX06 Devices         PORTD for dsPIC33EVXXXGMX06 Devices	46 47 48 318 41 46 59 52 44 44 55 53 53 57 52 54 63 62 64 63 65 66 66 66

Devices         50           PPS Output for dsPIC33EVXXXGM004/104         50           PPS Output for dsPIC33EVXXXGM006/106         51           Devices         51           PVM Generator 1         60           PVM Generator 3         61           PVM Generator 3         61           PWM Generator 3         61           PWM Generator 3         61           PWR Generator 3         61           PWR TReceiver         49           SENT1 Receiver         49           SENT2 Receiver         49           SP11 and SPI2         45           System Control         53           Timers         43           UART1 and UART2         45           ADxCHS0 (ADCx Input Channel 0 Select)         296           ADxCCN3 (ADCx Control 1)         289           ADxCON3 (ADCx Control 2)         291           ADxCON4 (ADCx Control 3)         293           ADxCON3 (ADCx Input Scan Select Liow)         300           ALTDTRx (PWMx Alternate Dead-Time)         211           ADxCON3 (ADCx Input Scan Select Low)         301           ALTDTRx (PWMx Alternate Dead-Time)         211           ADxCON3 (ADCx Control 3)         298	PPS Output for dsPIC33EVXXXGM002/102	
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Devices         51           PVMM         60           PVMM Generator 1         60           PVMM Generator 2         61           PVMM Generator 3         61           Reference Clock         53           SENT1 Receiver         49           SPH1 and SPI2         45           System Control         53           Timers         43           UART1 and UART2         45           Registers         ADxCHS0 (ADCx Input Channel 0 Select)         296           ADxCHS123 (ADCX control 1)         289           ADxCON2 (ADCx Control 2)         291           ADxCON2 (ADCx Control 3)         293           ADxCON4 (ADCx Control 3)         293           ADxCON4 (ADCx Input Scan Select Low)         300           ALTDTRx (PMMx Alternate Dead-Time)         211           ADxCON4 (ADCx Input Scan Select Low)         300           ALTDTRx (PMMx Alternate Dead-Time)         211           ADxCON4 (ADCx Input Scan Select Low)         300           ALTDTRx (PMMx Alternate Dead-Time)         211           AUXCONK (PWMx Auxiliary Control)         219           CHOP (PWMx Chop Clock Generator)         207           CLKDIV (Clock Divisor)         128		50
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PWM Generator 2.         61           PWM Generator 3.         61           Reference Clock         53           SENT1 Receiver         49           SENT2 Receiver         49           SPI1 and SPI2         45           System Control         53           Timers         43           UART1 and UART2         45           Registers         ADxCHS0 (ADCx Input Channel 0 Select)         296           ADxCON1 (ADCx Control 1)         289           ADxCON2 (ADCx Control 2)         291           ADxCON3 (ADCx Control 2)         291           ADxCON4 (ADCx Control 3)         293           ADxCON4 (ADCx Control 4)         294           ADXCSSL (ADCx Input Scan Select High)         298           ADxCSSL (ADCX Input Scan Select Low)         300           ALTDTRx (PWMx Atternate Dead-Time)         211           AUXCON4 (Comparator X Control)         206           CM4CON (Comparator 4 Control)         306           CMSTAT (Op Amp/Comparator Status)         303           CMxCON (Comparator x Filter Control)         312           CMxMSKCON (Comparator x Mask         Gating Control)           x = 1, 2, 3 or 5)         304           CMxFLTR (Comparator x Mask Source		
PWM Generator 3.         61           Reference Clock         53           SENT1 Receiver         49           SPI1 and SPI2         45           System Control         53           Timers.         43           UART1 and UART2         45           Registers         ADXCHS0 (ADCx Input Channel 0 Select)         296           ADXCHS123 (ADCx Input Channel 0 Select)         296           ADXCON2 (ADCx Control 1)         289           ADXCON1 (ADCx Control 1)         289           ADXCON2 (ADCx Control 3)         293           ADXCON3 (ADCx Control 4)         294           ADXCSSH (ADCx Input Scan Select High)         298           ADXCSS (ADCx Input Scan Select Low)         300           ALTDTSk (PWMx Atternate Dead-Time)         211           AUXCON1 (Comparator 4 Control)         219           CHOP (PWMx Chop Clock Generator)         207           CLKDIV (Comparator x Control)         303           CMXCON (Comparator X Control)         312           CMMCON (Comparator x Filter Control)         312           CMMSKSCO (Comparator x Mask Source         Select Control)           Select Control)         308           CORCON (Core Control)         271           C		
Reference Clock         53           SENT1 Receiver         49           SENT2 Receiver         49           SP11 and SP12         45           System Control         53           Timers         43           UART1 and UART2         45           Registers         43           ADxCHS0 (ADCx Input Channel 0 Select)         296           ADxCONS (ADCx Control 1)         289           ADxCON1 (ADCx Control 1)         289           ADxCON3 (ADCx Control 2)         291           ADxCON4 (ADCx Control 2)         293           ADxCON4 (ADCx Control 3)         293           ADxCON4 (ADCx Control 4)         294           ADxCSSL (ADCx Input Scan Select High)         298           ADxCSSL (ADCx Input Scan Select Low)         300           ALTDTRx (PWMx Alternate Dead-Time)         211           AUXCON4 (CMC Comparator X Control)         219           CHOP (PWMx Chop Clock Generator)         207           CLKDIV (Clock Divisor)         128           CM4CON (Comparator X Control)         306           CMXCON (Comparator X Mask         310           CMXMSKSCN (Comparator X Mask         310           CMxMSKSRC (Comparator X Mask Source         308	PWM Generator 2	61
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