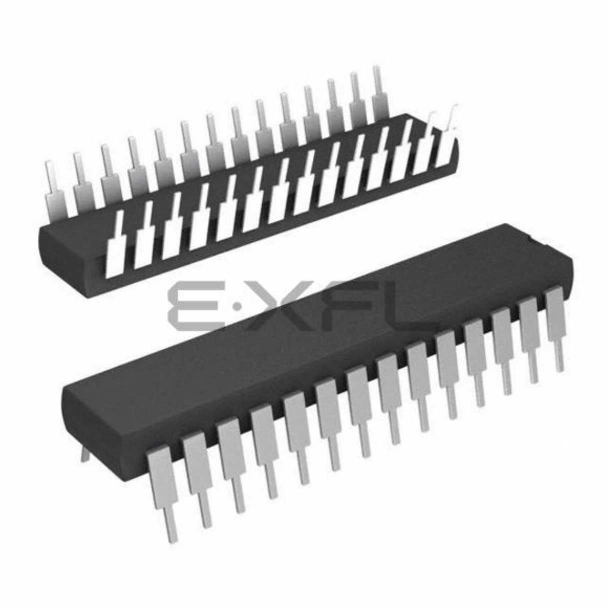

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm102-i-sp

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16-bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

> **Note:** The AVDD and AVSS pins must be connected, regardless of the ADC voltage reference source.

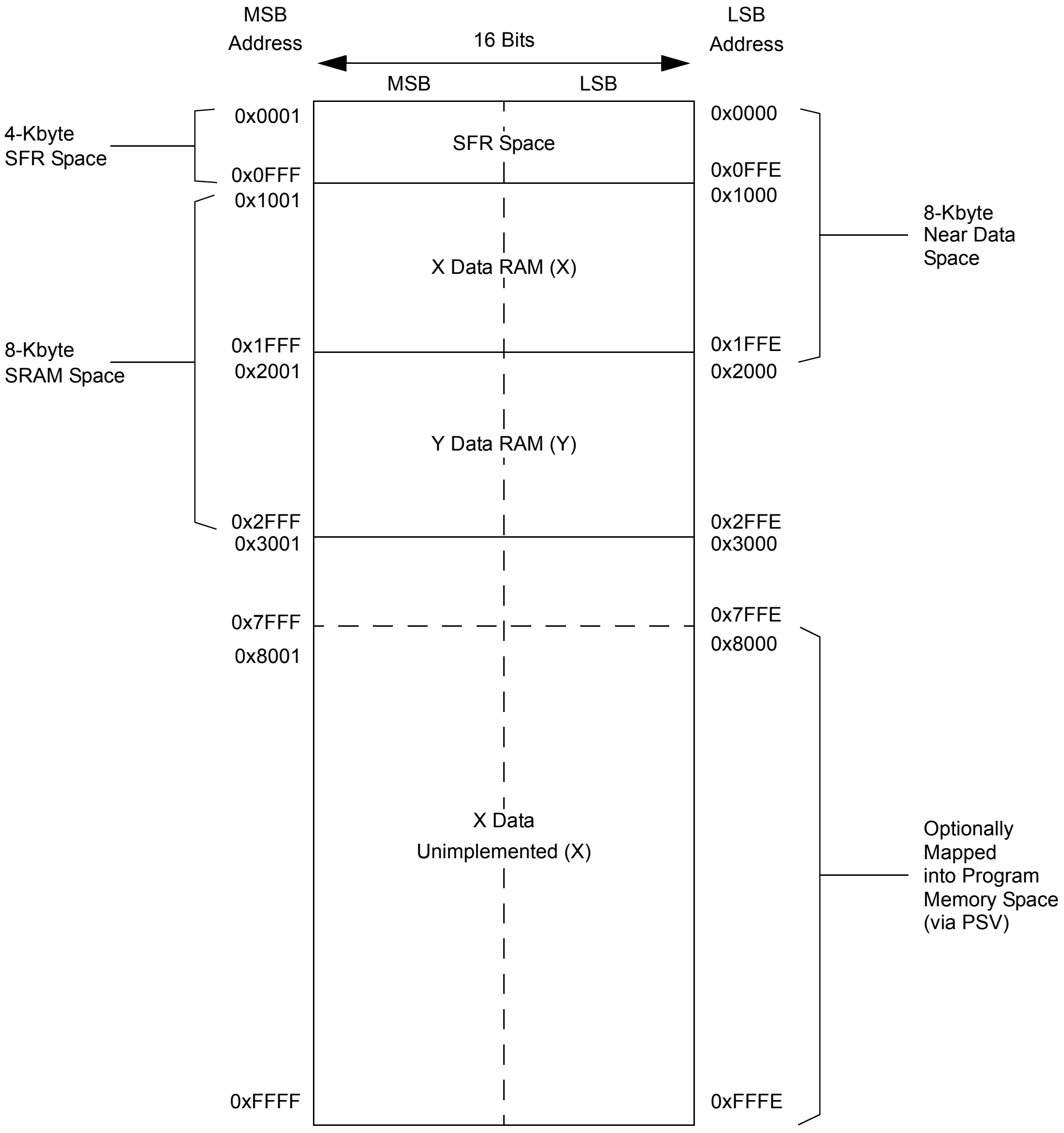
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10V-20V is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the Printed Circuit Board (PCB):** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.

FIGURE 4-7: DATA MEMORY MAP FOR 64-Kbyte/128-Kbyte DEVICES[1]



Note 1: Memory areas are not shown to scale.

4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																`0000`
W1	0002	W1																`0000`
W2	0004	W2																`0000`
W3	0006	W3																`0000`
W4	0008	W4																`0000`
W5	000A	W5																`0000`
W6	000C	W6																`0000`
W7	000E	W7																`0000`
W8	0010	W8																`0000`
W9	0012	W9																`0000`
W10	0014	W10																`0000`
W11	0016	W11																`0000`
W12	0018	W12																`0000`
W13	001A	W13																`0000`
W14	001C	W14																`0000`
W15	001E	W15																`0800`
SPLIM	0020	SPLIM																`xxxx`
ACCAL	0022	ACCAL																`xxxx`
ACCAH	0024	ACCAH																`xxxx`
ACCAU	0026	Sign Extension of ACCA<39>								ACCAU								`xxxx`
ACCBL	0028	ACCBL																`xxxx`
ACCBH	002A	ACCBH																`xxxx`
ACCBU	002C	Sign Extension of ACCB<39>								ACCBU								`xxxx`
PCL	002E	Program Counter Low Word Register															—	`0000`
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register							`0000`
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										`0001`
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register									`0001`
RCOUNT	0036	`REPEAT` Loop Counter Register															`0`	`xxxx`
DCOUNT	0038	DCOUNT<15:1>															`0`	`xxxx`
DOSTARTL	003A	DOSTARTL<15:1>															`0`	`xxxx`
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						`00xx`
DOENDL	003E	DOENDL<15:1>															—	`xxxx`

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

REGISTER 5-5: NVMSRCADRH: NVM DATA MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8	**Unimplemented:** Read as ‘0’
bit 7-0	**NVMSRCADRH<23:16>:** Data Memory Upper Address bits

REGISTER 5-6: NVMSRCADRL: NVM DATA MEMORY LOWER ADDRESS REGISTER

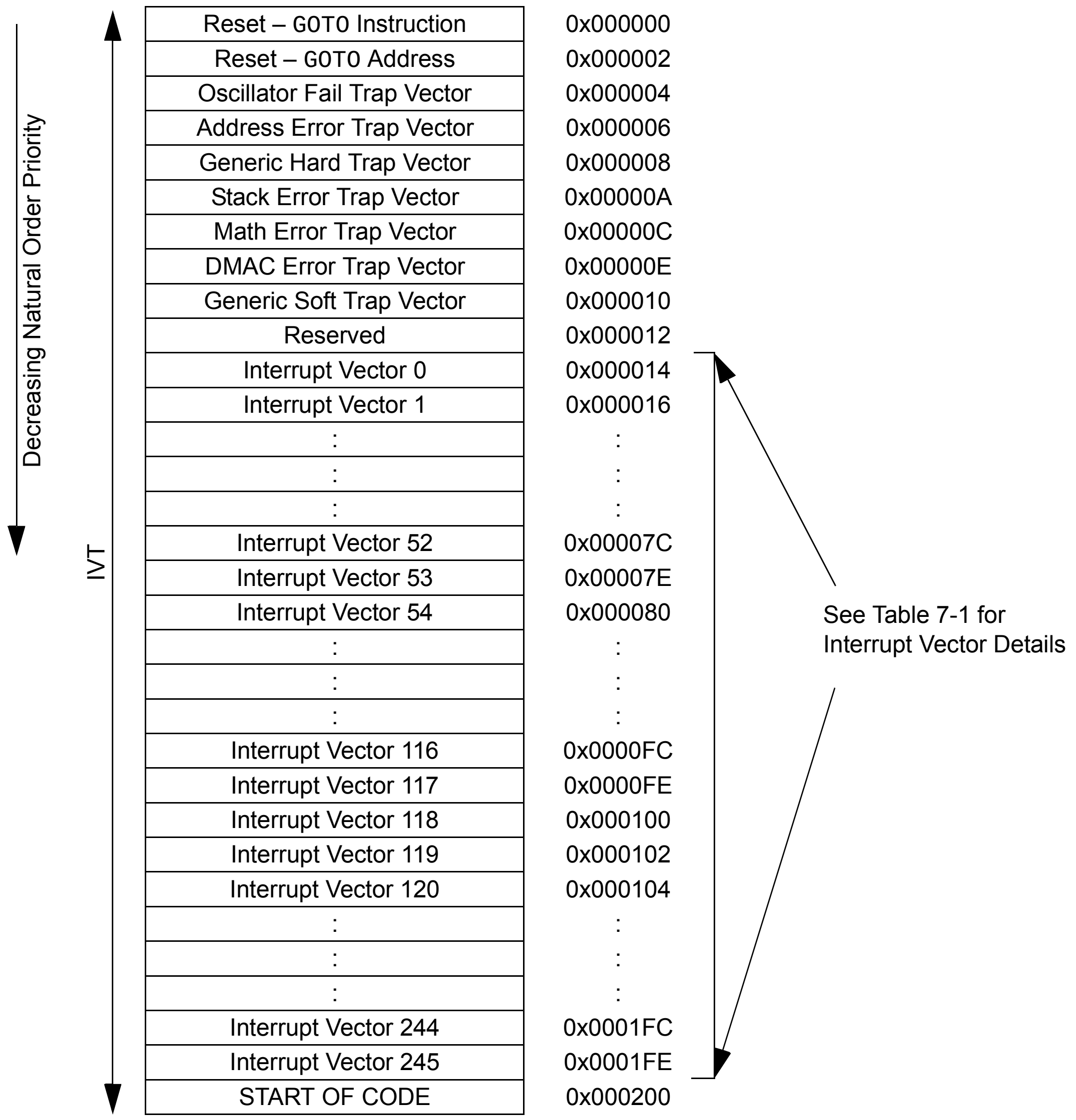
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	r-0
NVMSRCADR<7:1>							—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1	**NVMSRCADRL<15:1>:** Data Memory Lower Address bits
bit 0	**Reserved:** Maintain as ‘0’

FIGURE 7-2: dsPIC33EVXXXGM00X/10X FAMILY INTERRUPT VECTOR TABLE



Reset – `GOTO` Instruction	0x000000
Reset – `GOTO` Address	0x000002
Oscillator Fail Trap Vector	0x000004
Address Error Trap Vector	0x000006
Generic Hard Trap Vector	0x000008
Stack Error Trap Vector	0x00000A
Math Error Trap Vector	0x00000C
DMAC Error Trap Vector	0x00000E
Generic Soft Trap Vector	0x000010
Reserved	0x000012
Interrupt Vector 0	0x000014
Interrupt Vector 1	0x000016
:	:
:	:
:	:
Interrupt Vector 52	0x00007C
Interrupt Vector 53	0x00007E
Interrupt Vector 54	0x000080
:	:
:	:
:	:
Interrupt Vector 116	0x0000FC
Interrupt Vector 117	0x0000FE
Interrupt Vector 118	0x000100
Interrupt Vector 119	0x000102
Interrupt Vector 120	0x000104
:	:
:	:
:	:
Interrupt Vector 244	0x0001FC
Interrupt Vector 245	0x0001FE
START OF CODE	0x000200

9.1 CPU Clocking System

The dsPIC33EVXXXGM00X/10X family of devices provides the following six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

For instruction execution speed or device operating frequency, F_{CY}, see Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

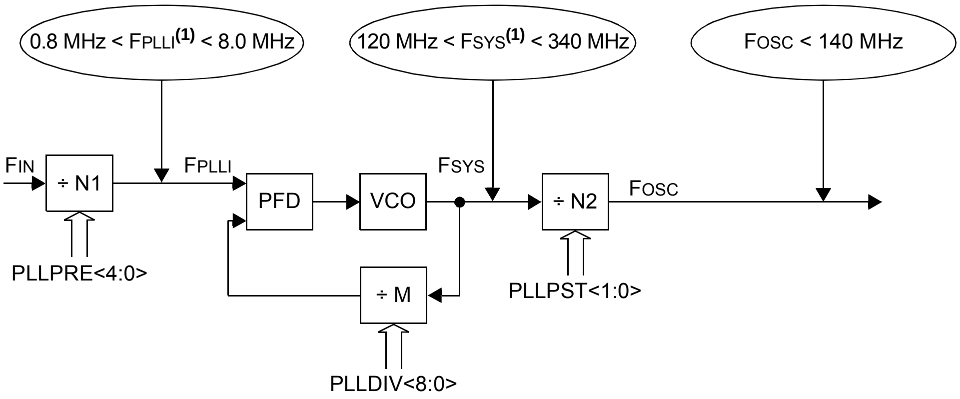
$$F_{CY} = F_{OSC}/2$$

Figure 9-2 provides the block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{OSC}).

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{SYS}).

FIGURE 9-2: PLL BLOCK DIAGRAM



Note 1: This frequency range must be met at all times.

EQUATION 9-2: FOSC CALCULATION

$$F_{OSC} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV\text{<8:0>} + 2)}{(PLLPRE\text{<4:0>} + 2) \times 2(PLLPOST\text{<1:0>} + 1)}\right)$$

Where:

$N1 = PLLPRE\text{<4:0>} + 2$

$N2 = 2 \text{ x } (PLLPOST\text{<1:0>} + 1)$

$M = PLLDIV\text{<8:0>} + 2$

EQUATION 9-3: FVCO CALCULATION

$$F_{SYS} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV\text{<8:0>} + 2)}{(PLLPRE\text{<4:0>} + 2)}\right)$$

11.6 High-Voltage Detect (HVD)

dsPIC33EVXXXGM00X/10X devices contain High-Voltage Detection (HVD) which monitors the VCAP voltage. The HVD is used to monitor the VCAP supply voltage to ensure that an external connection does not raise the value above a safe level (~2.4V). If high core voltage is detected, all I/Os are disabled and put in a tri-state condition. The device remains in this I/O tri-state condition as long as the high-voltage condition is present.

11.7 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-10 under "Injection Current", have internal protection diodes to VDD and VSS. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '`0`', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '`0`'.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = `0x0`, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention; for example, AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specifications. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

   VOH = 4.4V at IOH = -8 mA and VDD = 5V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current, <12 mA, is technically permitted. For more information, refer to the VOH/IOH specifications in **Section 30.0 "Electrical Characteristics"**.

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2CKR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘`0`’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8	**Unimplemented:** Read as ‘`0`’
bit 7-0	**T2CKR<7:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers) `10110101` = Input tied to RPI181 • • • `00000001` = Input tied to CMP1 `00000000` = Input tied to VSS

REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT1R<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘`0`’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 15-8 **SENT1R<7:0>:** Assign SENT Module Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

`10110101` = Input tied to RPI181
•
•
•
`00000001` = Input tied to CMP1
`00000000` = Input tied to V_{SS}

bit 7-0 **Unimplemented:** Read as ‘`0`’

REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT2R<7:0>							
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘`0`’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘`0`’

bit 7-0 **SENT2R<7:0>:** Assign SENT Module Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

`10110101` = Input tied to RPI181
•
•
•
`00000001` = Input tied to CMP1
`00000000`= Input tied to V_{SS}

REGISTER 17-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

REGISTER 17-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits

REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-0	**DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-0	**ALTDTRx<13:0>:** Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 19-2: I2CxCON2: I2Cx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘`0`’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7	**Unimplemented:** Read as ‘`0`’
bit 6	**PCIE:** Stop Condition Interrupt Enable bit (I^{2}C Slave mode only). `1` = Enables interrupt on detection of Stop condition `0` = Stop detection interrupts are disabled
bit 5	**SCIE:** Start Condition Interrupt Enable bit (I^{2}C Slave mode only) `1` = Enables interrupt on detection of Start or Restart conditions `0` = Start detection interrupts are disabled
bit 4	**BOEN:** Buffer Overwrite Enable bit (I^{2}C Slave mode only) `1` = The I2CxRCV register bit is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit = `0` `0` = The I2CxRCV register bit is only updated when I2COV is clear
bit 3	**SDAHT:** SDAx Hold Time Selection bit `1` = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx `0` = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx
bit 2	**SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^{2}C Slave mode only) If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences. `1` = Slave bus collision interrupts are enabled `0` = Slave bus collision interrupts are disabled
bit 1	**AHEN:** Address Hold Enable bit (I^{2}C Slave mode only) `1` = Following the 8th falling edge of SCLx for a matching received address byte; the SCLREL bit (I2CxCON1<12>) will be cleared and the SCLx will be held low `0` = Address holding is disabled
bit 0	**DHEN:** Data Hold Enable bit (I^{2}C Slave mode only) `1` = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCON1<12>) and the SCLx is held low `0` = Data holding is disabled

REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit

`1` = Edge 1 is edge-sensitive
`0` = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit

`1` = Edge 1 is programmed for a positive edge response
`0` = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits

`1111` = FOSC
`1110` = OSCI pin
`1101` = FRC Oscillator
`1100` = BFRC Oscillator
`1011` = Internal LPRC Oscillator
`1010` = Reserved
`1001` = Reserved
`1000` = Reserved
`0111` = Reserved
`0110` = Reserved
`0101` = Reserved
`0100` = Reserved
`0011` = CTED1 pin
`0010` = CTED2 pin
`0001` = OC1 module
`0000` = TMR1 module

bit 9 **EDG2STAT:** Edge 2 Status bit

Indicates the status of Edge 2 and can be written to control the edge source.
`1` = Edge 2 has occurred
`0` = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit

Indicates the status of Edge 1 and can be written to control the edge source.
`1` = Edge 1 has occurred
`0` = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit

`1` = Edge 2 is edge-sensitive
`0` = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit

`1` = Edge 2 is programmed for a positive edge response
`0` = Edge 2 is programmed for a negative edge response

REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2) (CONTINUED)

bit 1	**CSS17:** ADCx Input Scan Selection bit `1` = Selects ANx for input scan `0` = Skips ANx for input scan
bit 0	**CSS16:** ADCx Input Scan Selection bit `1` = Selects ANx for input scan `0` = Skips ANx for input scan

Note 1: If the op amp is selected (OPAEN bit (CMxCON<10>) = `1`), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TB10	TTXH	TxCK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB15	TTXP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TB20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TC10	TTXH	TxCK High Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTXL	TxCK Low Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTXP	TxCK Input Period	Synchronous, with Prescaler	2 TCY + 40	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TC20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = `0`, CKP = `1`, SMP = `0`) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SS1}}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SS1}}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{\text{SS1}}$ ↑ after SCK1 Edge	1.5 T_{CY} + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
HDO16	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	IOL = 8.8 mA, VDD = 5.0V
HDO10	VOL	**Output Low Voltage** 8x Sink Driver Pins(3)	—	—	0.4	V	IOL = 10.8 mA, VDD = 5.0V
HDO26	VOH	**Output High Voltage** 4x Sink Driver Pins(2)	VDD – 0.6	—	—	V	IOH = -8.3 mA, VDD = 5.0V
HDO20	VOH	**Output High Voltage** 8x Sink Driver Pins	VDD – 0.6	—	—	V	IOH = -12.3 mA, VDD = 5.0V

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x sink driver pins (see below).

3: Includes the pins, such as RA3, RA4 and RB<15:10> for 28-pin devices, RA3, RA4, RA9 and RB<15:10> for 44-pin devices, and RA4, RA7, RA9, RB<15:10> and RC15 for 64-pin devices.

TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
HBO10	VBOR	BOR Event on VDD Transition High-to-Low	4.15	4.285	4.4	V	VDD (see **Note 2, Note 3** and **Note 4**)

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The VBOR specification is relative to the VDD.

3: The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but is not characterized.

4: The start-up VDD must rise above 4.6V.

TABLE 31-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
HD130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C(2)
HD134	TRETD	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

33.4 IPD

FIGURE 33-13: TYPICAL IPD vs. VDD

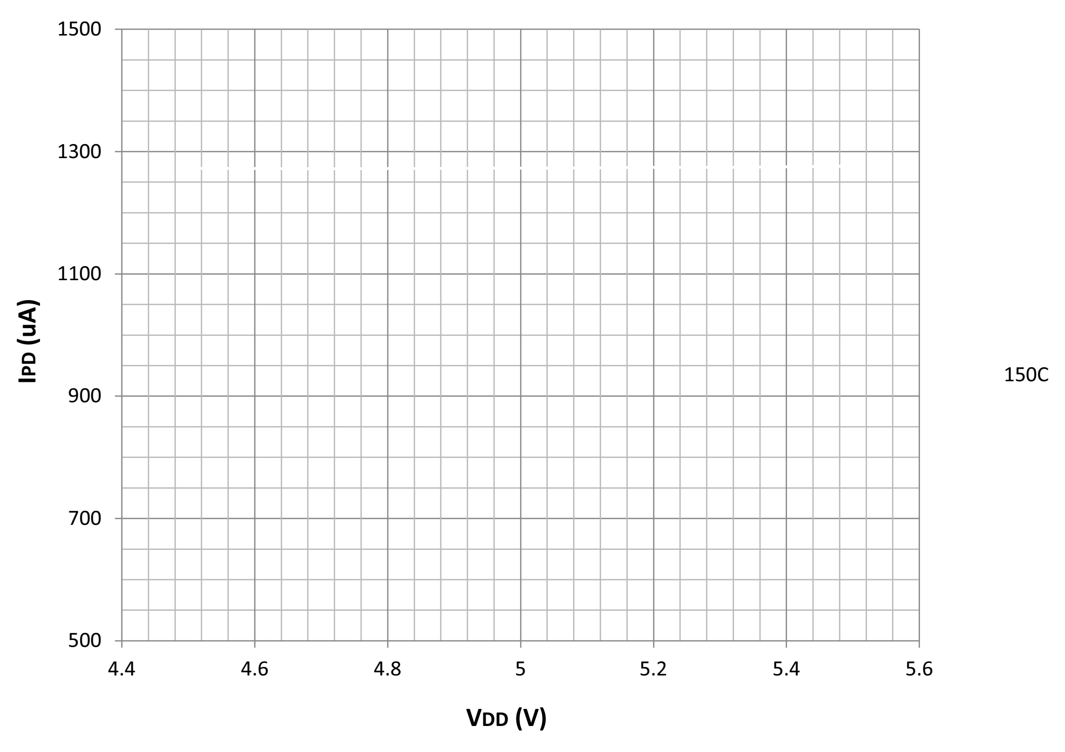
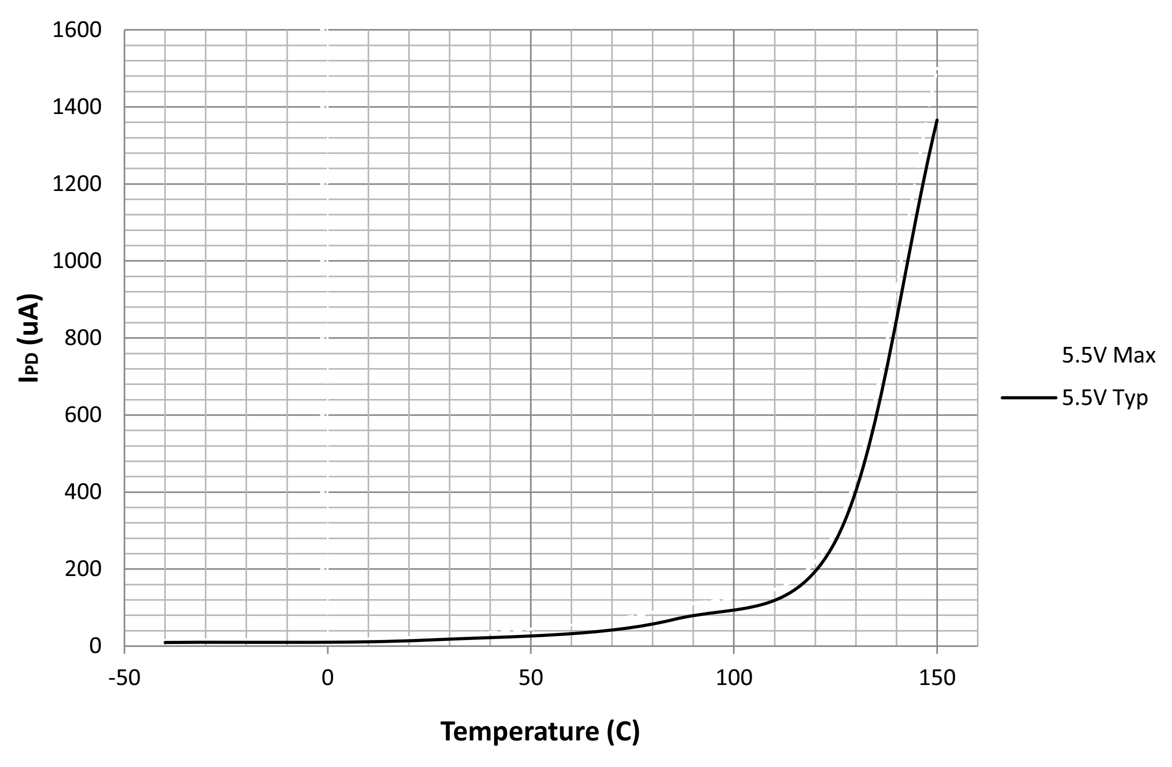
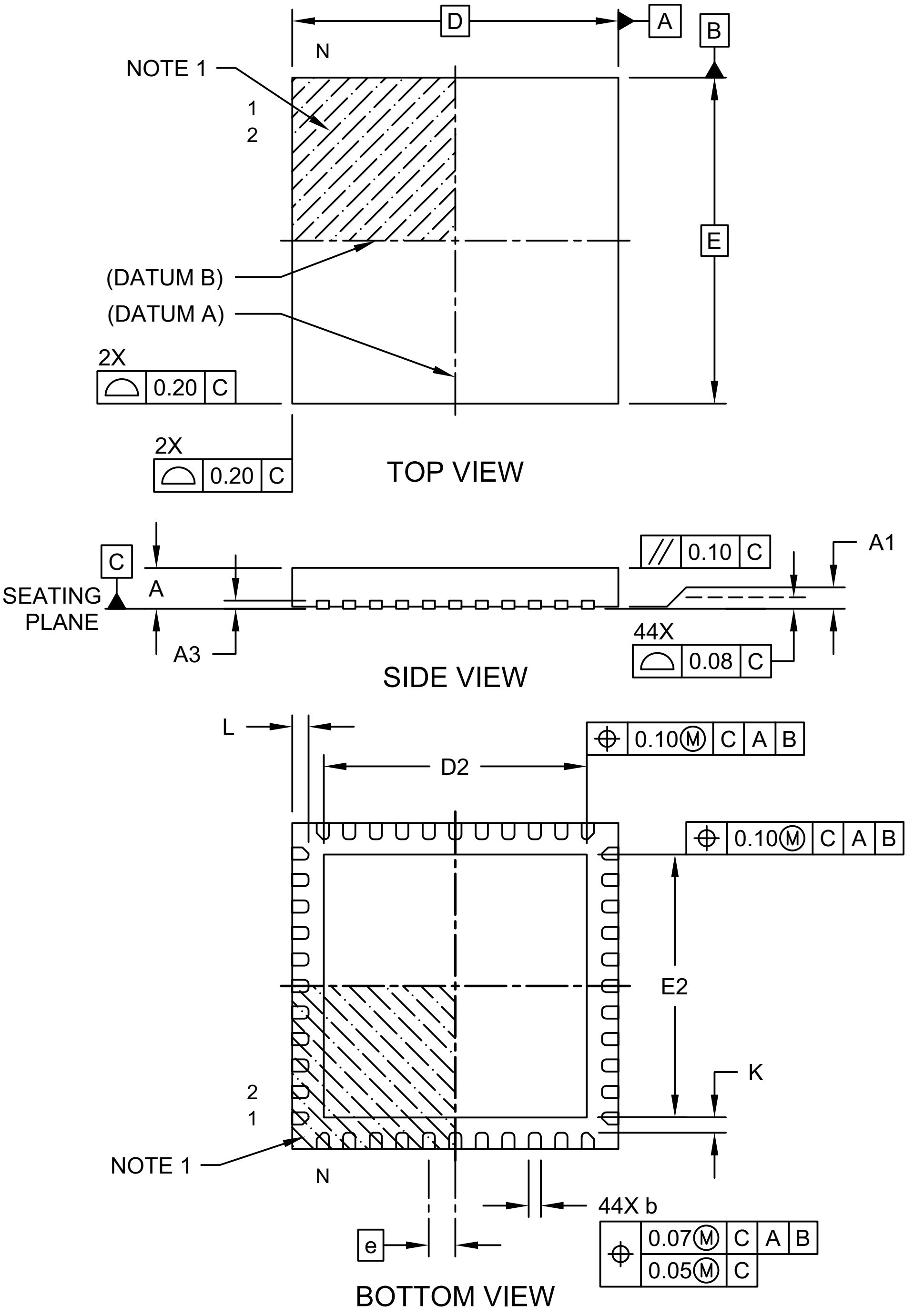


FIGURE 33-14: TYPICAL/MAXIMUM IPD vs. TEMPERATURE



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103D Sheet 1 of 2