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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm102-i-ss

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1,2)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit

1 = REPEAT loop is in progress
0 = REPEAT loop is not in progress

bit 3 **N:** MCU ALU Negative bit

1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = Overflow has not occurred for signed arithmetic

bit 1 **Z:** MCU ALU Zero bit

1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit

1 = A carry-out from the Most Significant bit (MSb) of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT(1)	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminates executing the DO loop at the end of the current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-24: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in the data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configure the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or a PSV page.
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing.

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using the Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-43 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when an overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-43: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS AND PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last Page	DSRPAG = 0x1FF	0	See **Note 1**
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw Page	DSRPAG = 0x300	1	PSV: First MSB Page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB Page	DSRPAG = 0x3FF	0	See **Note 1**
O, Write		DSWPAG = 0x1FF	1	EDS: Last Page	DSWPAG = 0x1FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	PSV Page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw Page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB Page	DSRPAG = 0x2FF	1	PSV: Last lsw Page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudolinear Addressing is not supported for large offsets.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain outputs. This is controlled by the Open-Drain Control x register (ODCx) associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See Table 30-10 in **Section 30.0 "Electrical Characteristics"** for the maximum VIH specification of each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx registers control the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UARTs, etc., the corresponding ANSELx bits must be cleared.

The ANSELx register has a default value of 0xFFFF. Therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions table (see Table 1-1 in **Section 1.0 "Device Overview"**).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function (ICN) of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States, even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the ICN functionality of each I/O port. The CNENx registers contain the ICN interrupt enable control bits for each of the input pins. Setting any of these bits enables an ICN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	The pull-ups and pull-downs on ICN pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0   ; Configure PORTB<15:8>
                   ; as inputs
MOV   W0, TRISB    ; and PORTB<7:0>
                   ; as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

11.8 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1R<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **INT1R<7:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2R<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **INT2R<7:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-15: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTCMP3R7	DTCMP3R6	DTCMP3R5	DTCMP3R4	DTCMP3R3	DTCMP3R2	DTCMP3R1	DTCMP3R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTCMP2R7	DTCMP2R6	DTCMP2R5	DTCMP2R4	DTCMP2R3	DTCMP2R2	DTCMP2R1	DTCMP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **DTCMP3R<7:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **DTCMP2R<7:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 14-11: DMTHOLDREG: DMT HOLD REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **UPRCNT<15:0>:** Value of the DMTCNTH register when DMTCNTL and DMTCNTH were Last Read bits

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits(1)
111 = Reserved
•
•
•
100 = Reserved
011 = Reserved
010 = Reserved
001 = Reserved
000 = SYNCI1 input from PPS

bit 3-0 **SEVTPS<3:0>:** Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 postscaler generates a Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 postscaler generates a Special Event Trigger on every second compare match event
0000 = 1:1 postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 17-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER(2) (CONTINUED)

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pin; PWMxL output signal is connected to the PWMxH pin
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides through the OVRDAT<1:0> bits are synchronized to the PWMx time base
0 = Output overrides through the OVRDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TRGCMP<15:0>:** Trigger Control Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN(2)	CKP	MSTEN	SPRE2(3)	SPRE1(3)	SPRE0(3)	PPRE1(3)	PPRE0(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled, pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit
1 = SDOx pin is not used by the module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** Clock Edge Select bit(1)
1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
2: This bit must be cleared when FRMEN = 1.
3: Do not set both primary and secondary prescalers to the value of 1:1.

21.1 UART Helpful Tips

1. In multi-node direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin, depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on wake-up from Sleep mode, caused by activity on the UxRX pin of the UART module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid. This is to be expected.

REGISTER 22-22: CxRXFUL1: CANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<15:8>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<7:0>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

REGISTER 22-23: CxRXFUL2: CANx RECEIVE BUFFER FULL REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<31:24>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<23:16>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

23.1 CTMU Control Registers

REGISTER 23-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN(2)	EDGEN	EDGSEQEN	IDISSEN(1)	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(2)
1 = Edge delay generation is enabled
0 = Edge delay generation is disabled

bit 11 **EDGEN:** Edge Enable bit
1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(1)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** ADC Trigger Control bit
1 = CTMU triggers the ADC start of conversion
0 = CTMU does not trigger the ADC start of conversion

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold (S&H) capacitor is not automatically discharged between sample/conversion cycles. Any software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

2: If the TGEN bit is set to '1', then the CMP1 module should be selected as the Edge 2 source in the EDG2SELx bits field; otherwise, the module will not function.

30.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**.

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

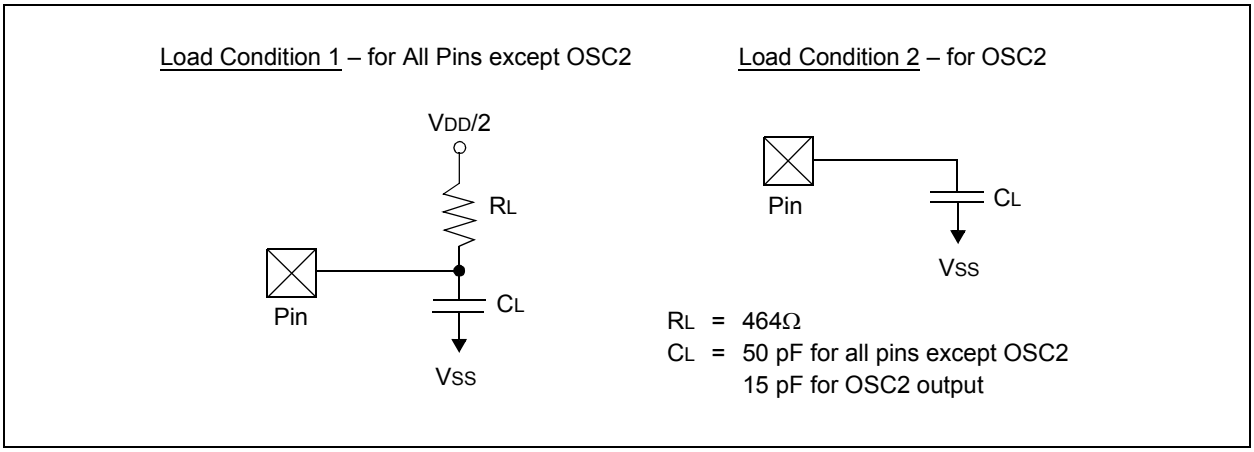


TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

TABLE 30-50: OP AMP/COMPARATOR x SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Comparator AC Characteristics							
CM10	TRESP	Response Time	—	19	80	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
Comparator DC Characteristics							
CM30	VOFFSET	Comparator Offset Voltage	-80	±60	80	mV	
CM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/Fall Time	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp AC Characteristics							
CM20	SR	Slew Rate	—	9	—	V/µs	10 pF load
CM21	PM	Phase Margin	—	35	—	°C	G = 100V/V, 10 pF load
CM22	GM	Gain Margin	—	20	—	db	G = 100V/V, 10 pF load
CM23	GBW	Gain Bandwidth	—	10	—	MHz	10 pF load
Op Amp DC Characteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio	—	45	—	db	VCM = AVDD/2
CM42	VOFFSET	Op Amp Offset Voltage	-50	±6	50	mV	
CM43	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM44	IOS	Input Offset Current	—	—	—	—	See pad leakage currents in Table 30-10
CM45	IB	Input Bias Current	—	—	—	—	See pad leakage currents in Table 30-10
CM46	IOUT	Output Current	—	—	420	µA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	—	—	kΩ	**Note 2**
CM49a	VOUT	Output Voltage	AVSS + 0.075	—	AVDD – 0.075	V	IOUT = 420 µA

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

33.0 CHARACTERISTICS FOR HIGH-TEMPERATURE DEVICES (+150°C)

33.1 IDD

FIGURE 33-1: TYPICAL/MAXIMUM IDD vs. FOSC (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)

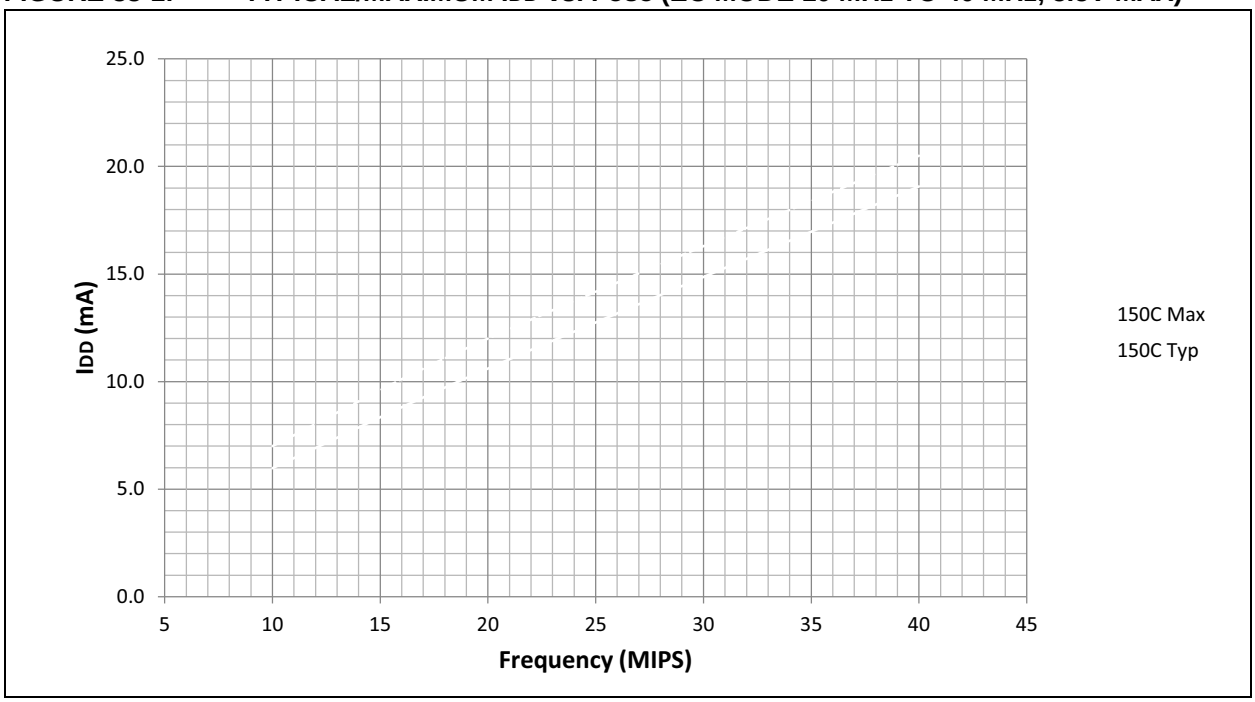


FIGURE 33-2: TYPICAL IDD vs. VDD (EC MODE, 10 MIPS)

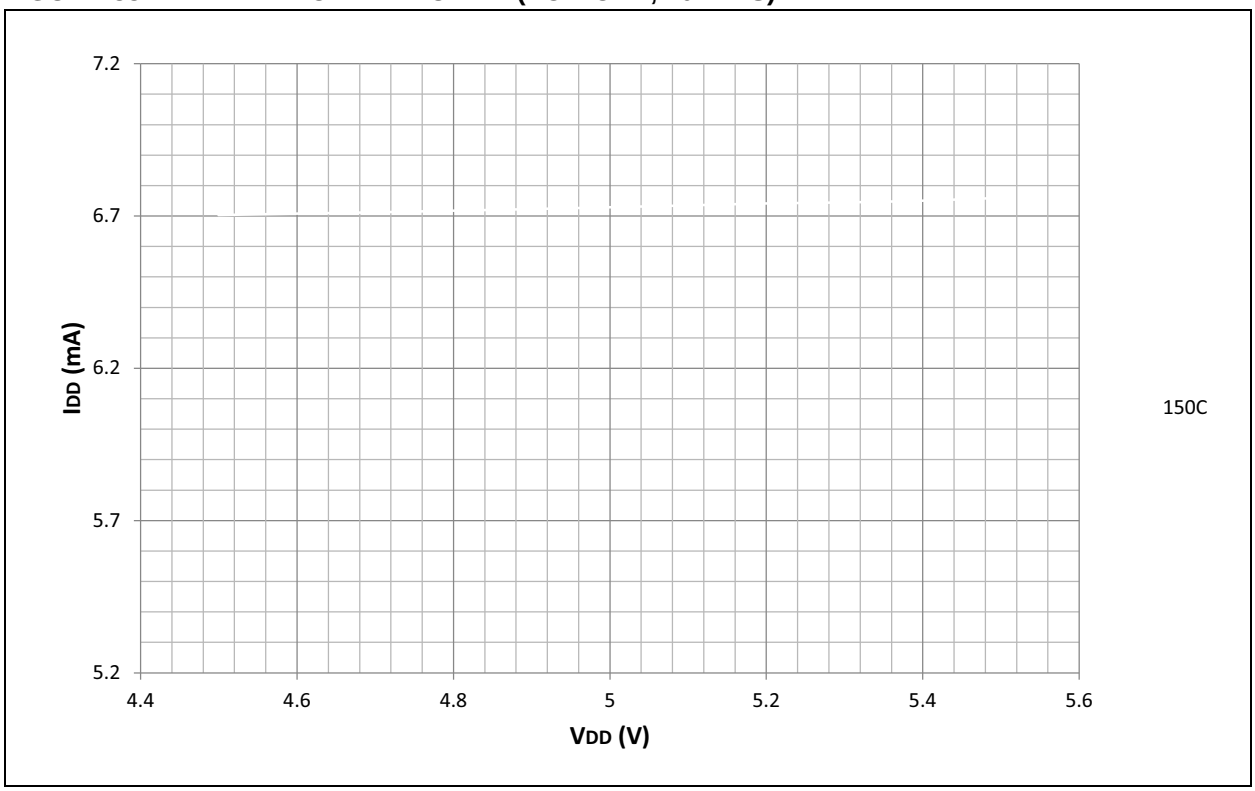


FIGURE 33-3: TYPICAL IDD vs. VDD (EC MODE, 20 MIPS)

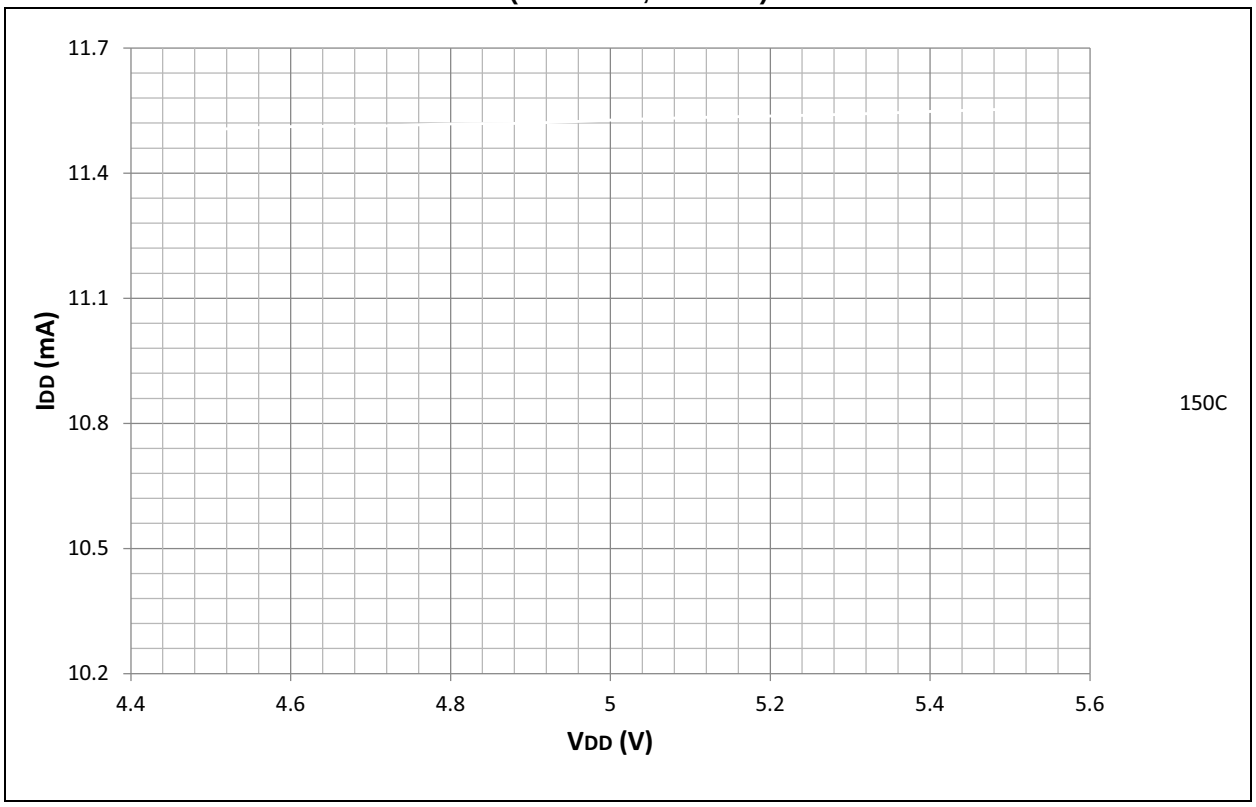
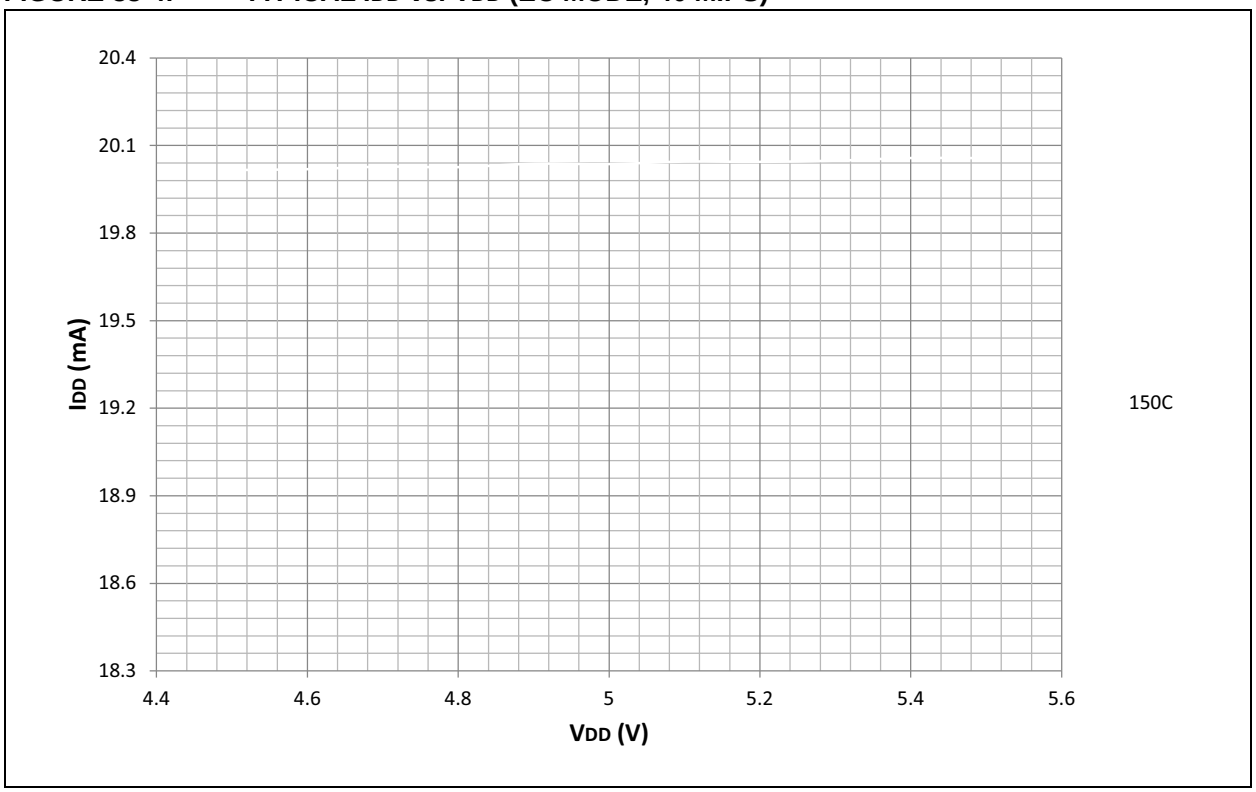
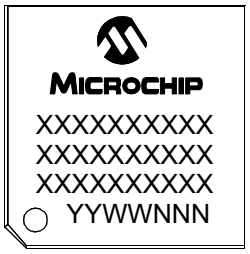


FIGURE 33-4: TYPICAL IDD vs. VDD (EC MODE, 40 MIPS)



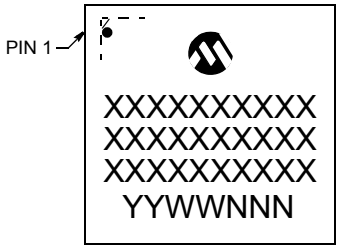
34.1 Package Marking Information (Continued)

44-Lead TQFP (10x10x1 mm)

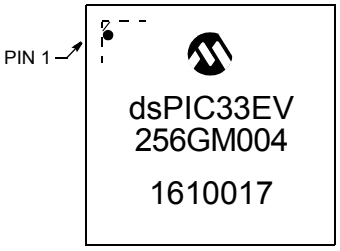


Example

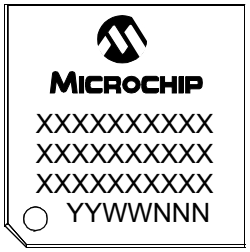
44-Lead QFN (8x8 mm)



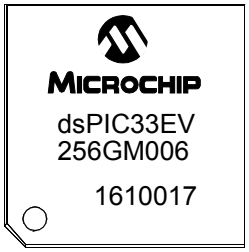
Example



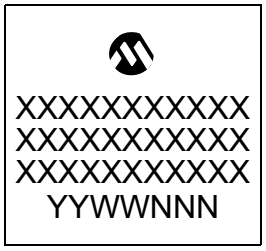
64-Lead TQFP (10x10x1 mm)



Example



64-Lead QFN (9x9x0.9 mm)



Example

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