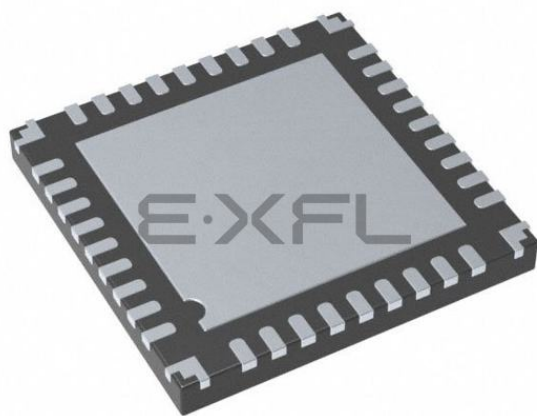




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

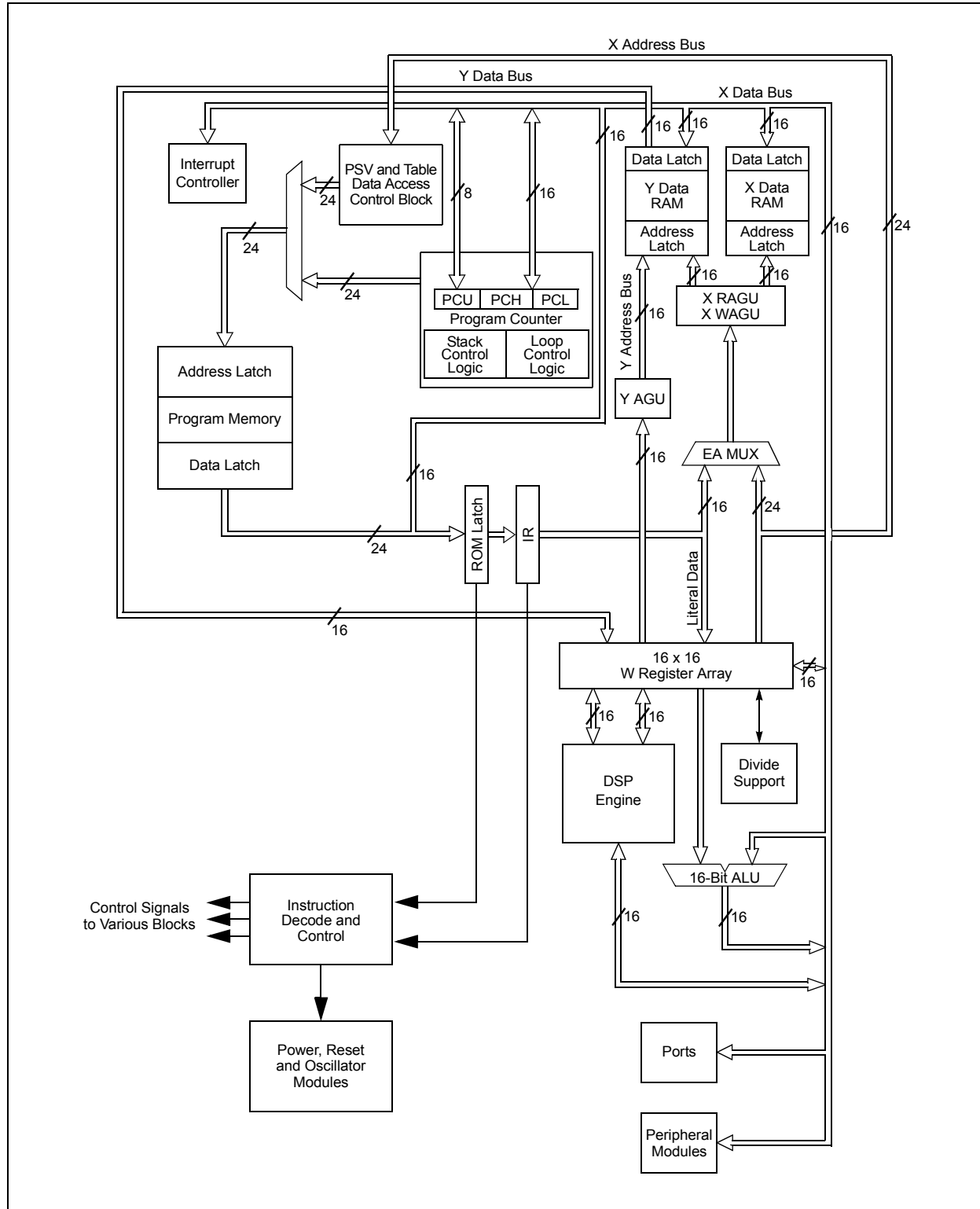
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm103-i-m5

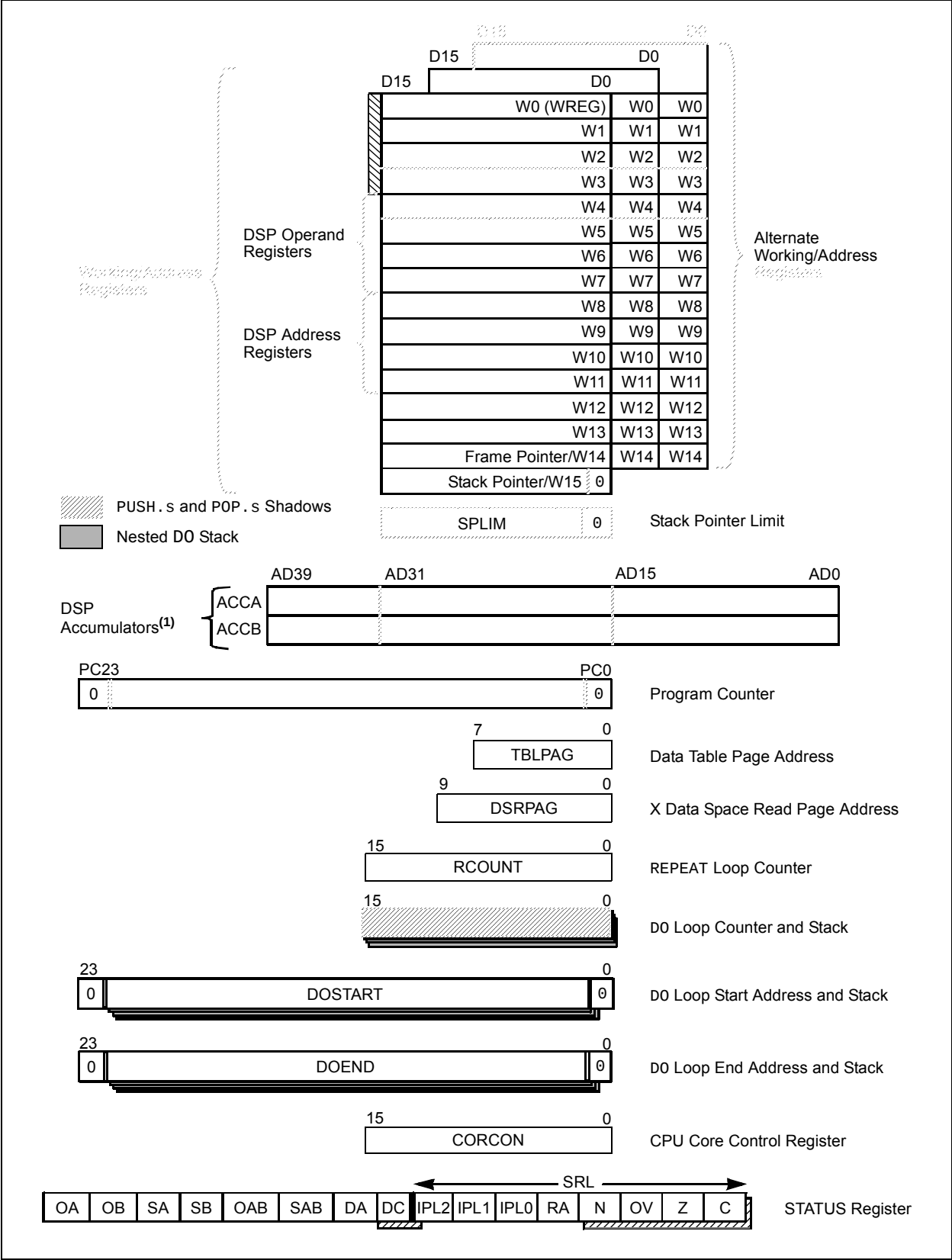
dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 3-1: dsPIC33EVXXXGM00X/10X FAMILY CPU BLOCK DIAGRAM



dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 3-2: PROGRAMMER'S MODEL



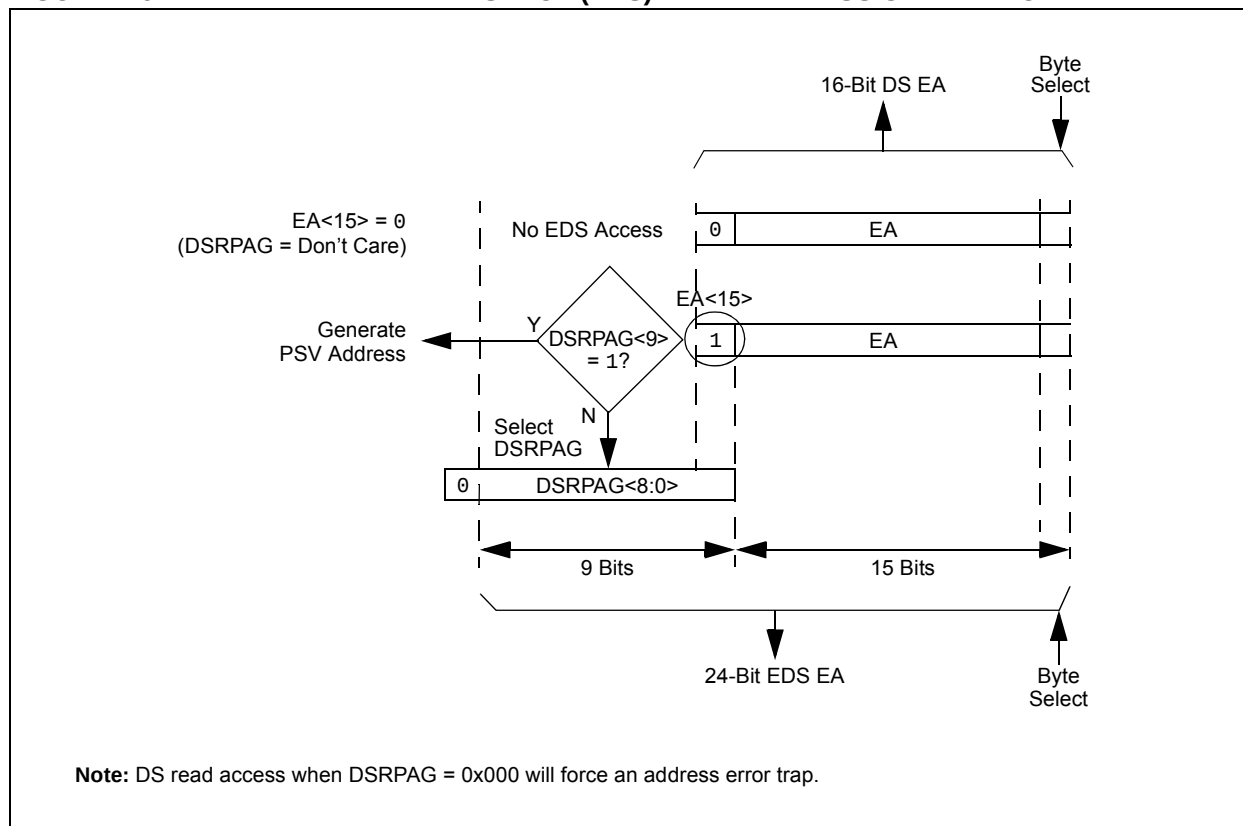
dsPIC33EVXXGM00X/10X FAMILY

4.3.1 PAGED MEMORY SCHEME

The dsPIC33EVXXGM00X/10X family architecture extends the available DS through a paging scheme, which allows the available DS to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the Base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Data Space Read Page register (DSRPAG) or the 9-bit Data Space Write Page register (DSWPAG), to form an EDS address, or Program Space Visibility (PSV) address.

The Data Space Page registers are located in the SFR space. Construction of the EDS address is shown in Figure 4-9 and Figure 4-10. When $DSRPAG<9> = 0$ and the base address bit, $EA<15> = 1$, the $DSRPAG<8:0>$ bits are concatenated onto $EA<14:0>$ to form the 24-bit EDS read address. Similarly, when the base address bit, $EA<15> = 1$, the $DSWPAG<8:0>$ bits are concatenated onto $EA<14:0>$ to form the 24-bit EDS write address.

FIGURE 4-9: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Direct Memory Access (DMA)**” (DS70348) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM. For the simplified DMA block diagram, refer to Figure 8-1.

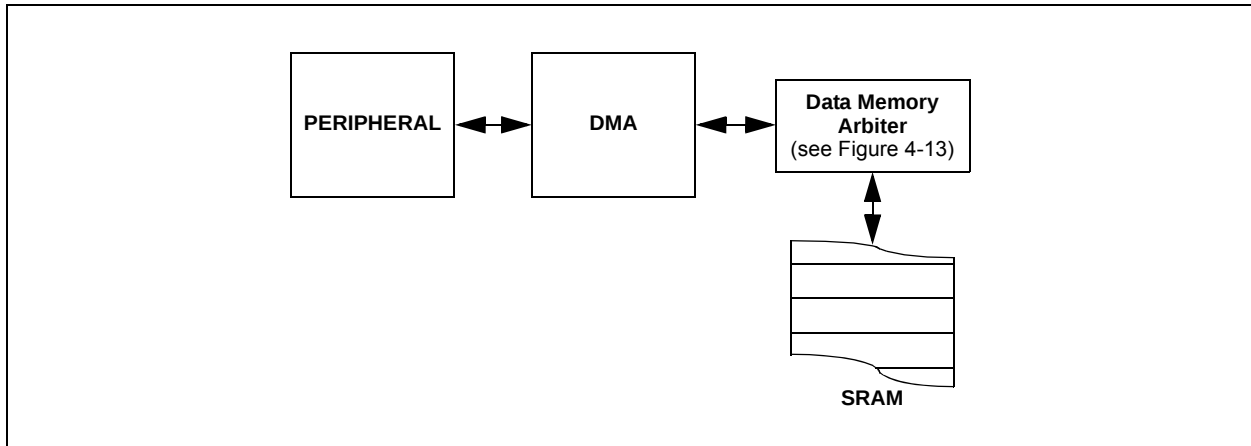
In addition, DMA can access the entire data memory space. The data memory bus arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. The peripherals supported by the DMA Controller include:

- CAN
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: PERIPHERAL TO DMA CONTROLLER



dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator x bits
11111 = Fault 32 (**default**)
11110 = Reserved
.
.
.
01100 = Op Amp/Comparator 5
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Fault 8
00110 = Fault 7
00101 = Fault 6
00100 = Fault 5
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator x bit⁽²⁾
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator x bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT<1:0> values (cycle)
00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT<1:0> values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FDEVOP<0>) is a '1', the FCLCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>**: Secondary Prescale bits (Master mode)⁽³⁾

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>**: Primary Prescale bits (Master mode)⁽³⁾

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to the value of 1:1.

dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

FIGURE 20-1: SENTx MODULE BLOCK DIAGRAM

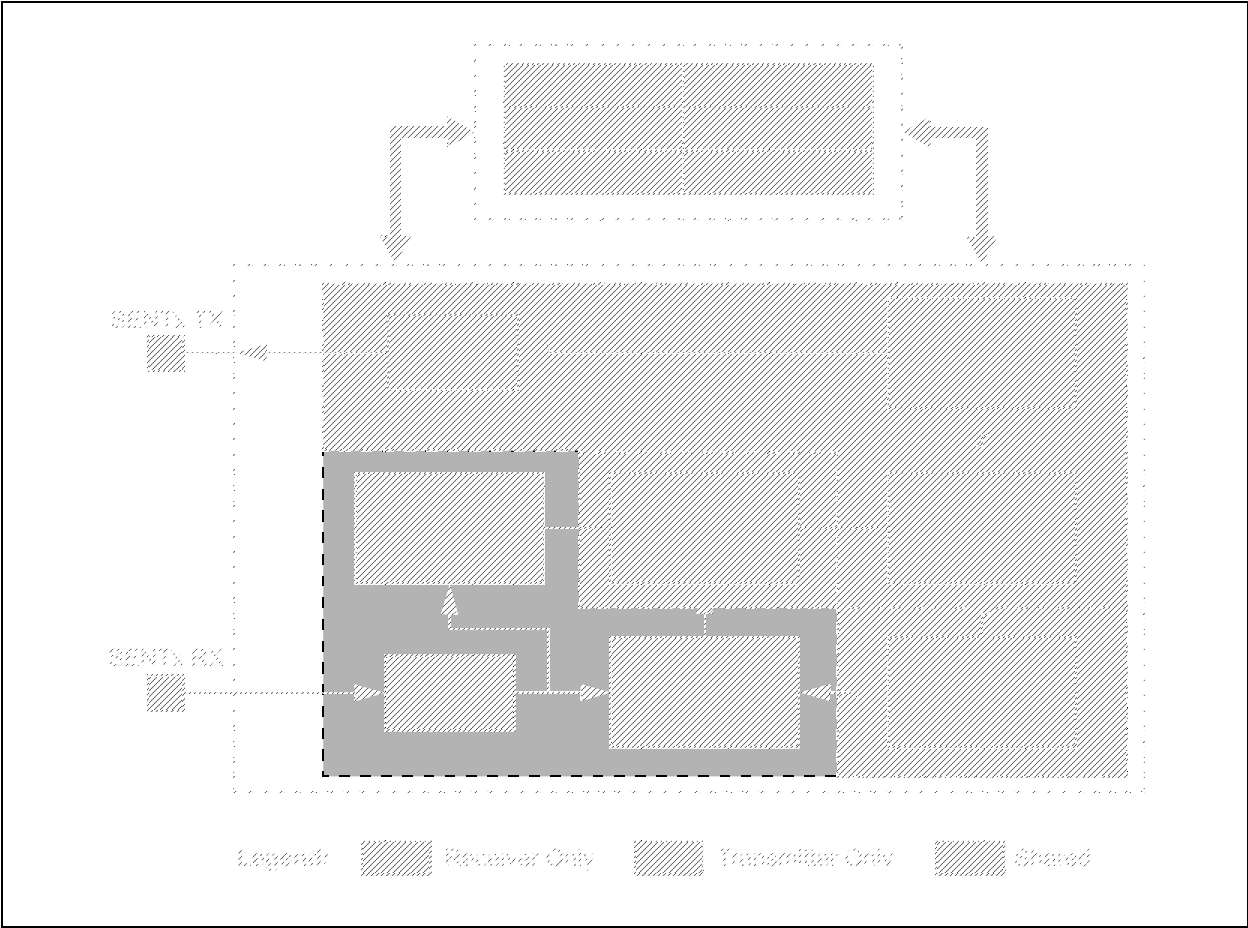
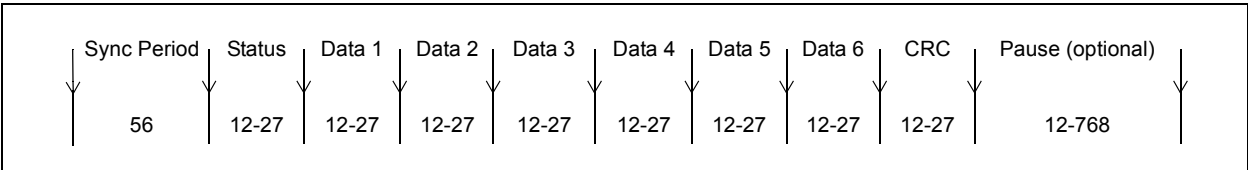


FIGURE 20-2: SENTx PROTOCOL DATA FRAMES



dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 22-2: CxCTRL2: CANx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT<4:0>				
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5

Unimplemented: Read as '0'

bit 4-0

DNCNT<4:0>: DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection

10001 = Compare up to Data Byte 3, bit 6 with EID<17>

•

•

•

00001 = Compare up to Data Byte 1, bit 7 with EID<0>

00000 = Do not compare data bytes

dsPIC33EVXXXGM00X/10X FAMILY

**FIGURE 30-21: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1)
TIMING CHARACTERISTICS**

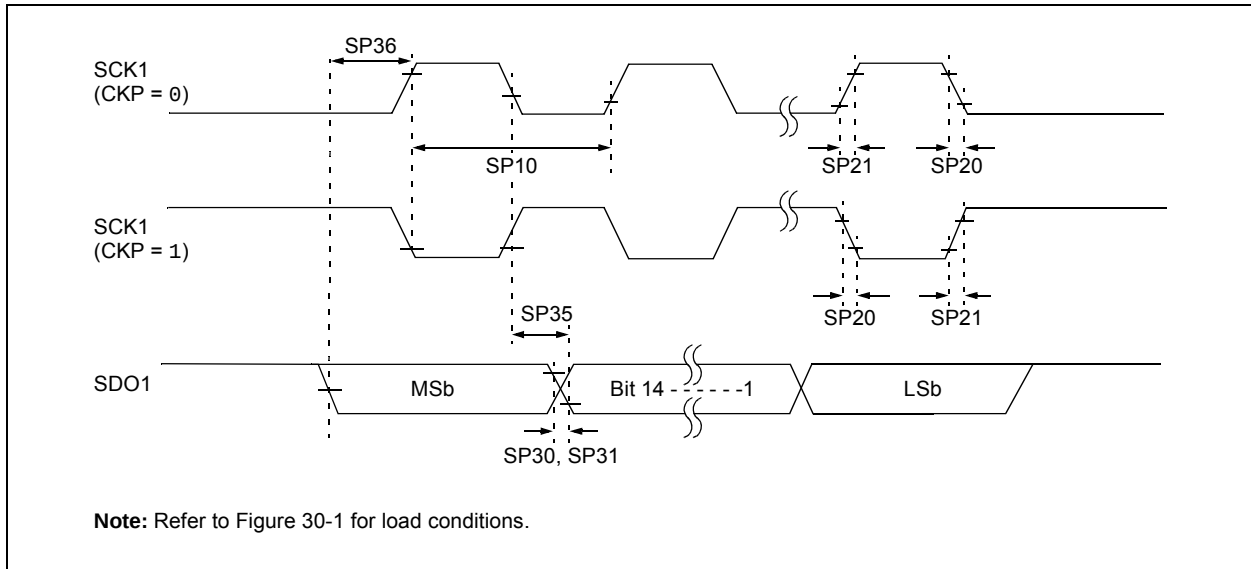


TABLE 30-39: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See Note 3
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2sch, TdiV2scl	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

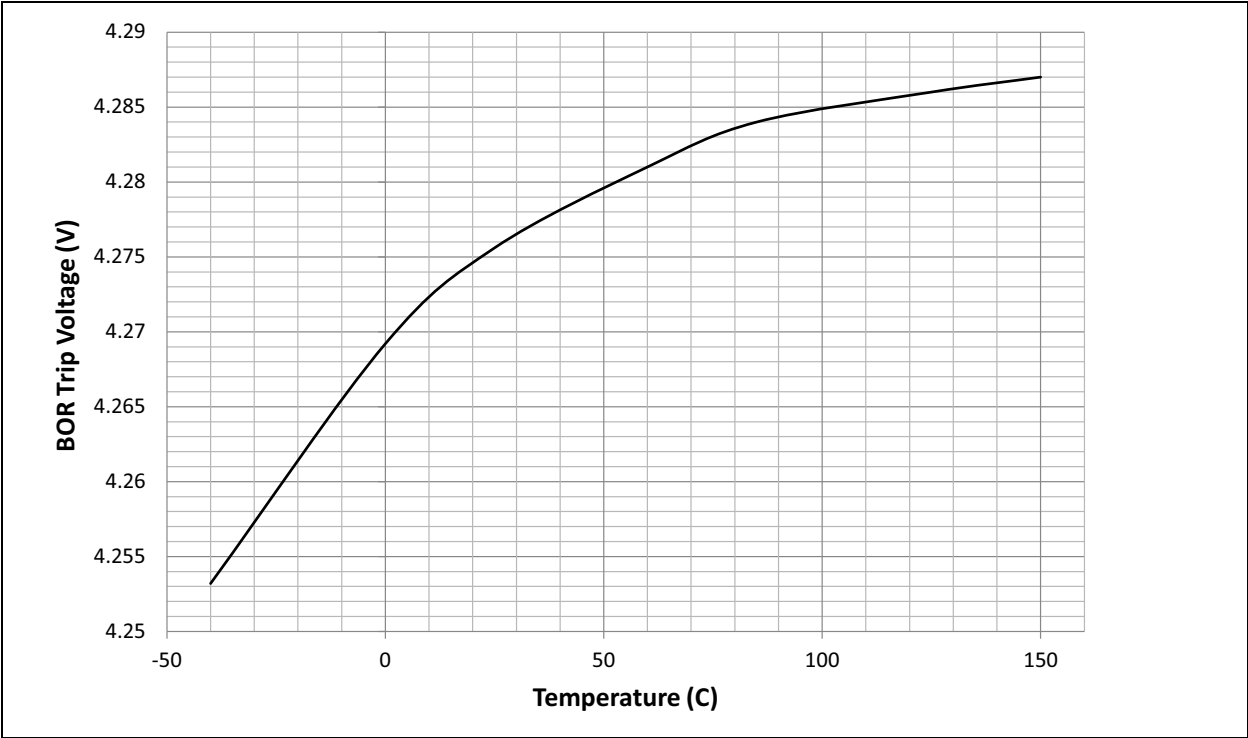
2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

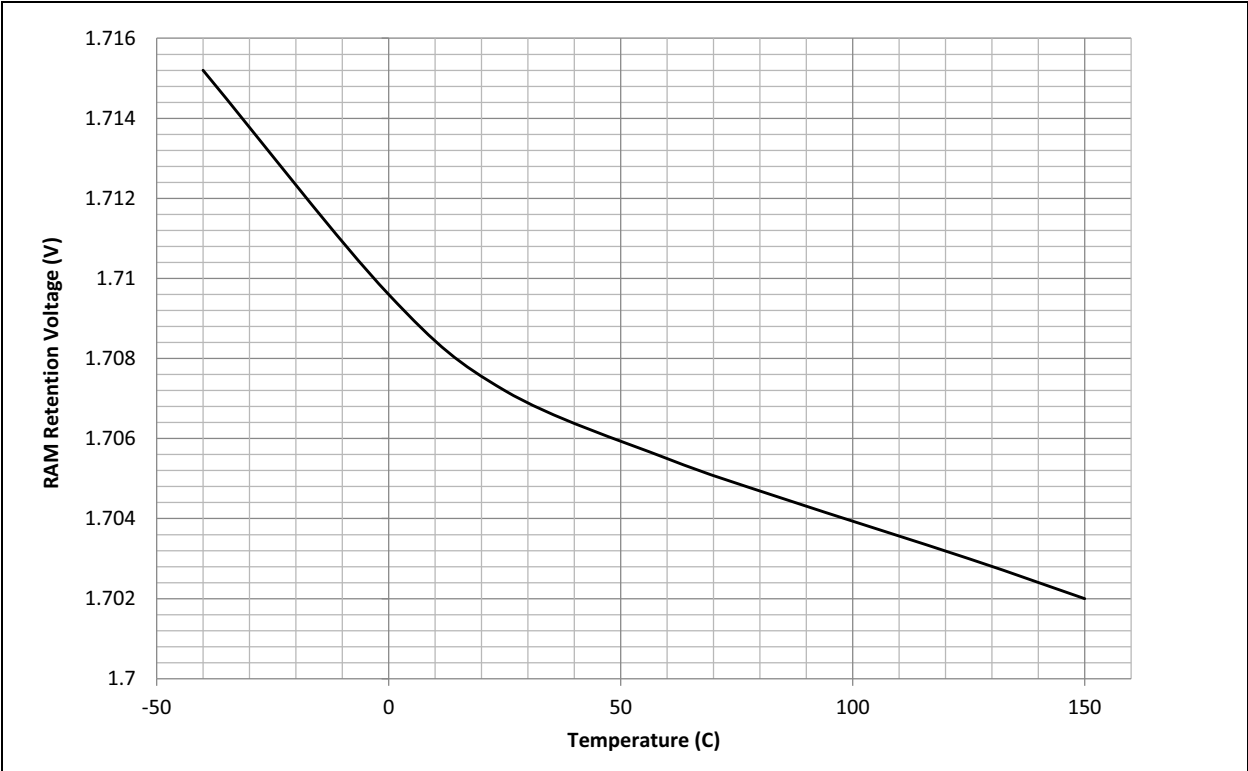
32.12 V_{BOR}

FIGURE 32-35: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



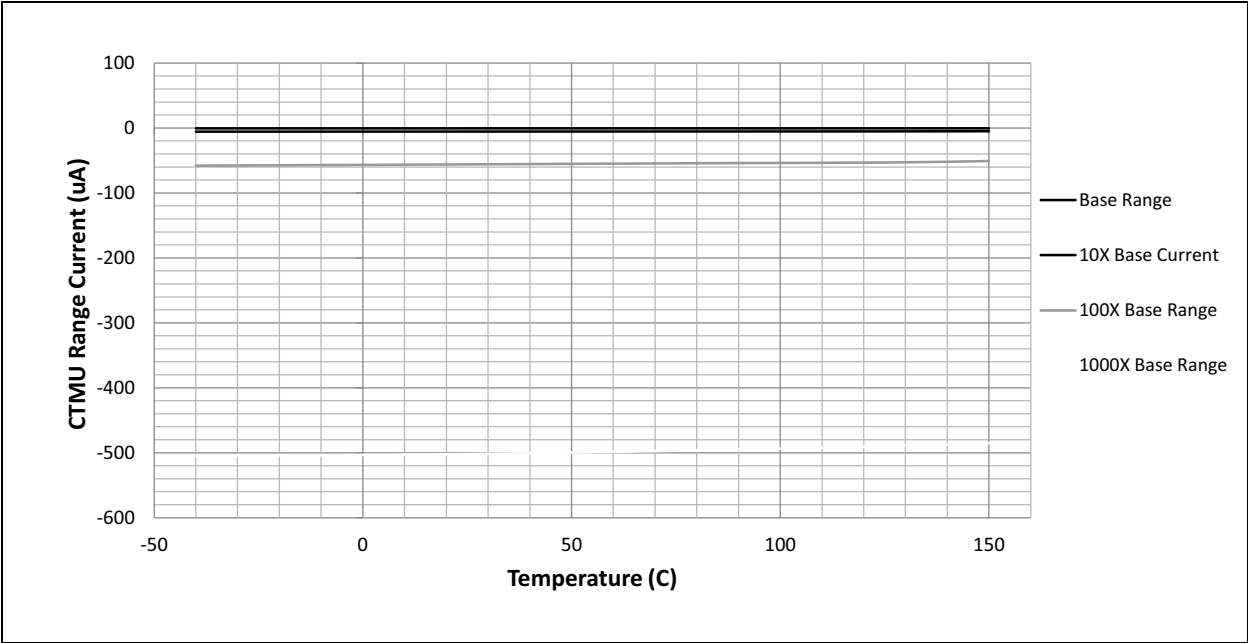
32.13 RAM Retention

FIGURE 32-36: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE



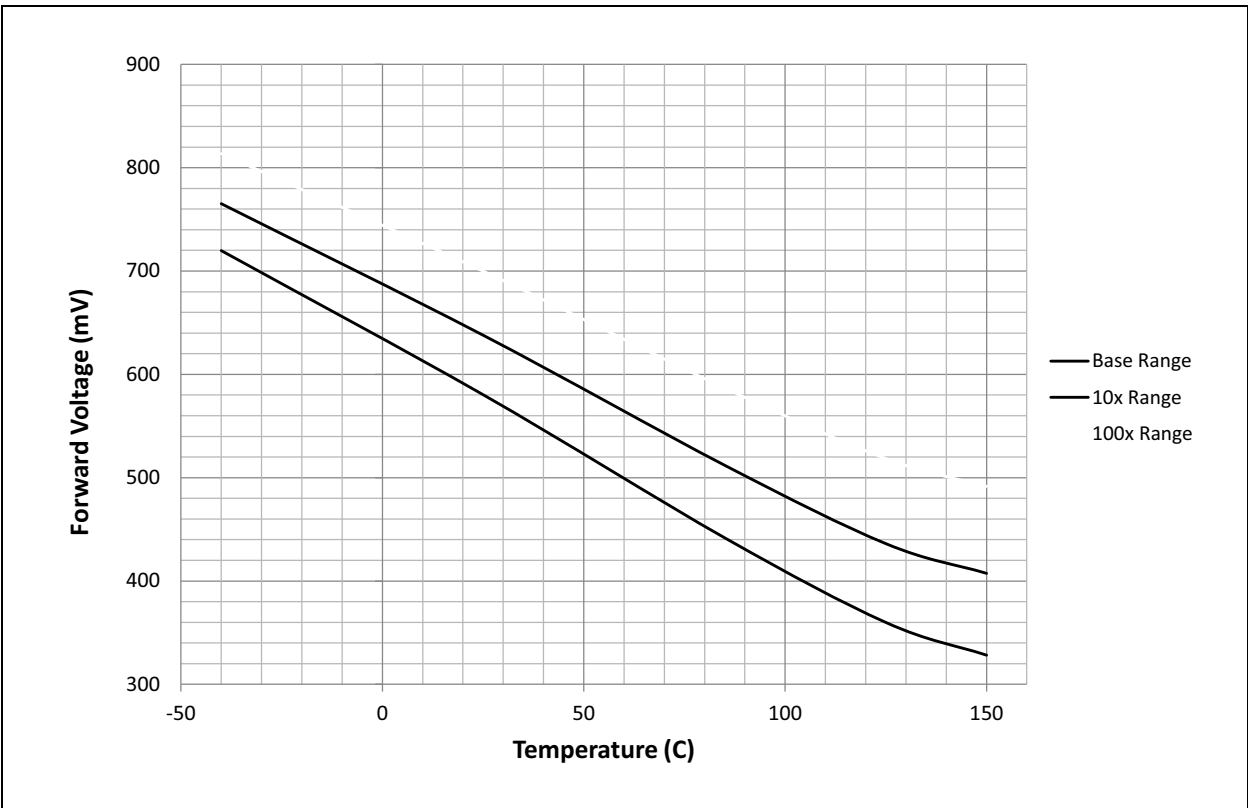
32.15 CTMU Current vs. Temperature

FIGURE 32-39: TYPICAL CTMU CURRENT (IRNG) vs. TEMPERATURE



32.16 CTMU Temperature Forward Diode

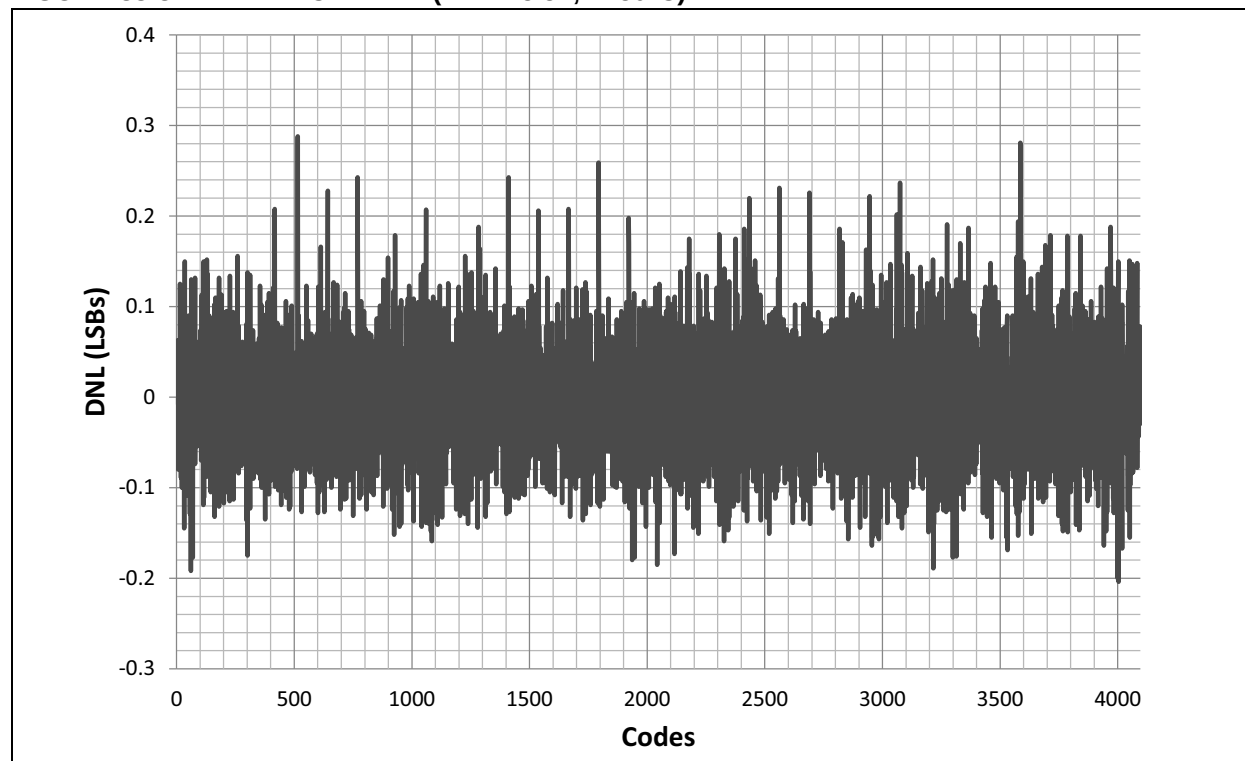
FIGURE 32-40: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE vs. TEMPERATURE



dsPIC33EVXXXGM00X/10X FAMILY

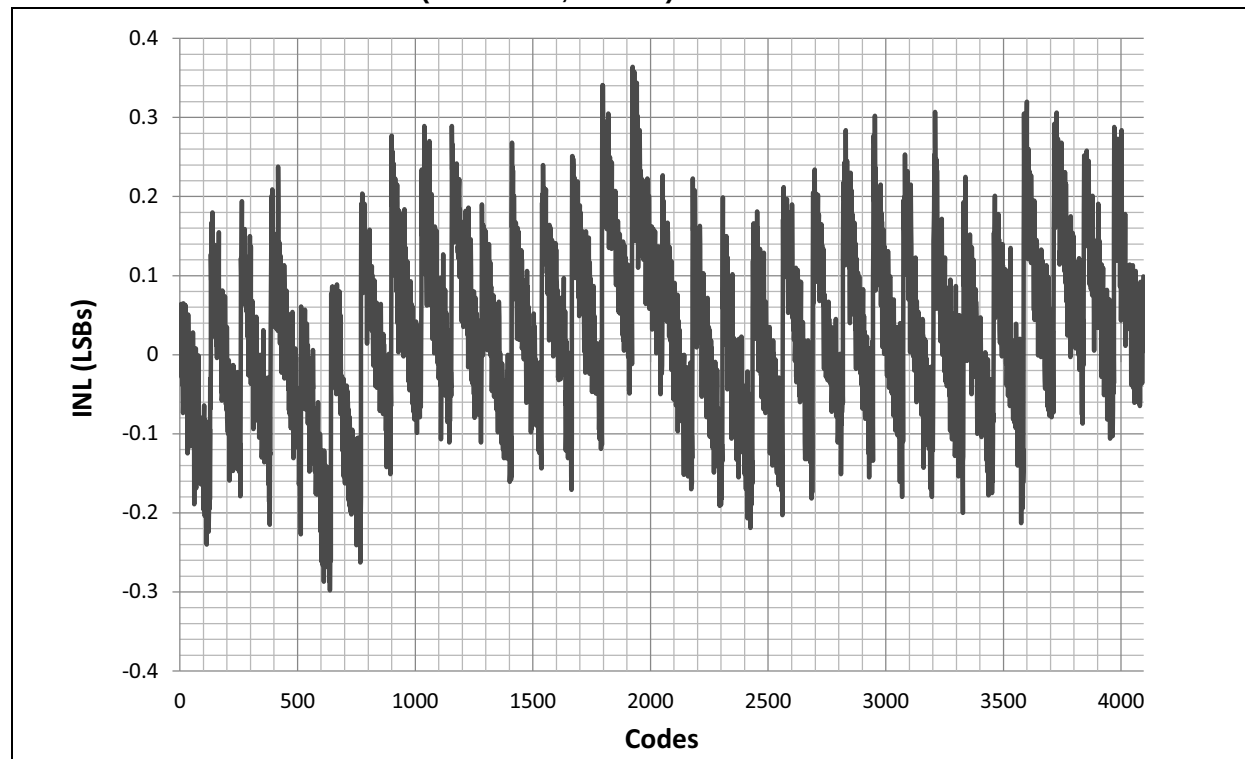
33.17 ADC DNL

FIGURE 33-37: TYPICAL DNL ($V_{DD} = 5.5V$, $+150^{\circ}C$)



33.18 ADC INL

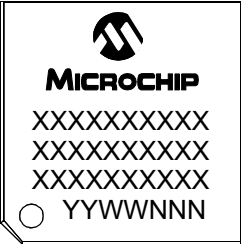
FIGURE 33-38: TYPICAL INL ($V_{DD} = 5.5V$, $+150^{\circ}C$)



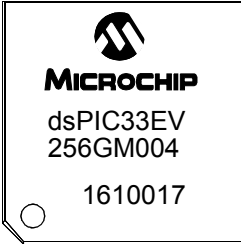
dsPIC33EVXXXGM00X/10X FAMILY

34.1 Package Marking Information (Continued)

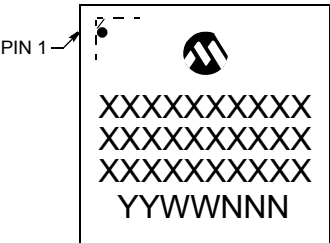
44-Lead TQFP (10x10x1 mm)



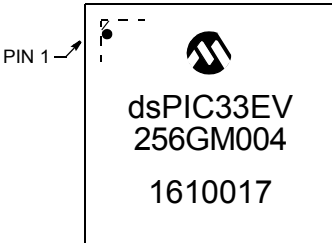
Example



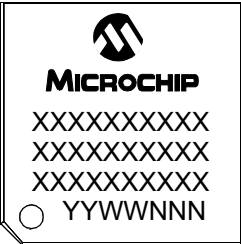
44-Lead QFN (8x8 mm)



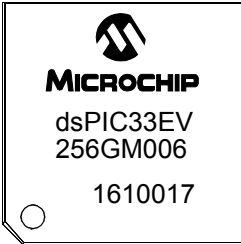
Example



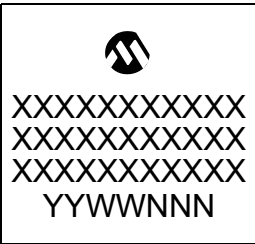
64-Lead TQFP (10x10x1 mm)



Example



64-Lead QFN (9x9x0.9 mm)



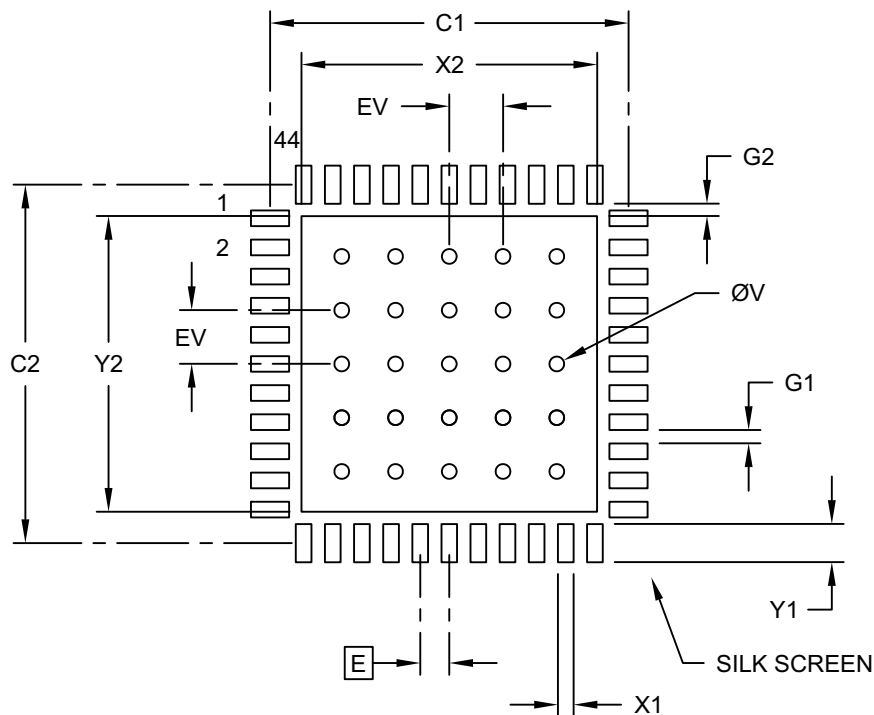
Example



dsPIC33EVXXXGM00X/10X FAMILY

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

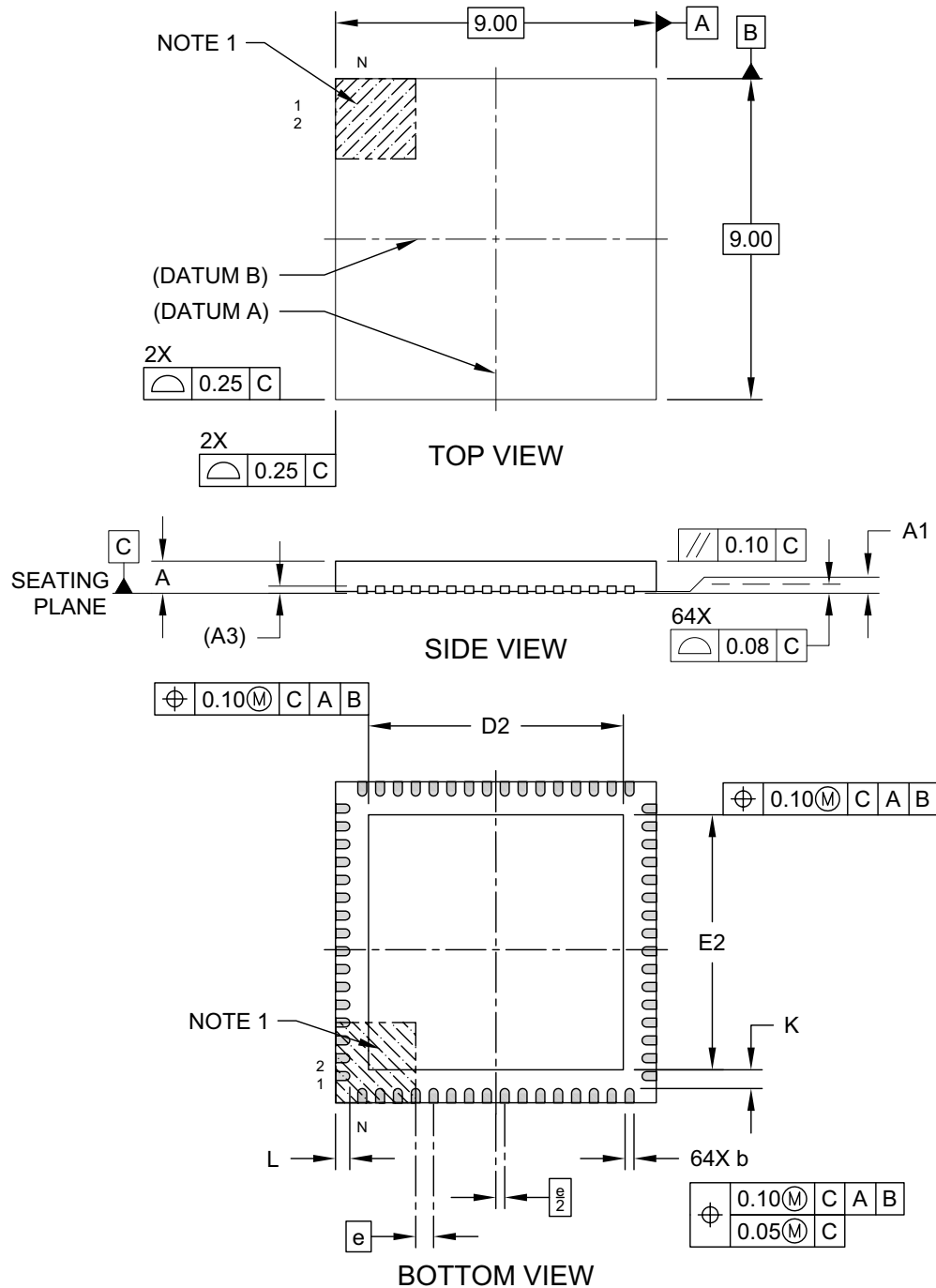
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C

dsPIC33EVXXXGM00X/10X FAMILY

**64-Lead Very Thin Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-149D [MR] Sheet 1 of 2

dsPIC33EVXXXGM00X/10X FAMILY

Revision E (September 2016)

This revision incorporates the following updates:

- Sections:
 - Added new **Section 32.0 “Characteristics for Industrial/Extended Temperature Devices (-40°C to +125°C)”** and **Section 33.0 “Characteristics for High-Temperature Devices (+150°C)”**.
 - Updated the **Qualification and Class B Support** section.
 - Updated **Section 27.6 “In-Circuit Serial Programming”**.
 - Updated **Section 34.0 “Packaging Information”** with the addition of the 28-Lead SSOP package information and new packaging diagram revisions.
 - Updated the **“Product Identification System”** section with the addition of the 28-Lead SSOP package.
- Figures:
 - Updated Figure 4-6.
- Registers:
 - Updated Register 25-2, Register 25-3, Register 27-1 and Register 27-2.
- Tables:
 - Updated Table 30-7, Table 30-9, Table 30-39, Table 30-40, Table 30-41, Table 30-42, Table 30-43, Table 30-44 and Table 30-45.

dsPIC33EVXXXGM00X/10X FAMILY

CxFMSKSEL1 (CANx Filters 7-0 Mask Selection 1).....	269	I2CxMSK (I2Cx Slave Mode Address Mask).....	235
CxFMSKSEL2 (CANx Filters 15-8 Mask Selection 2).....	270	I2CxSTAT (I2Cx Status).....	234
CxINTE (CANx Interrupt Enable).....	261	ICxCON1 (Input Capture x Control 1).....	190
CxINTF (CANx Interrupt Flag).....	260	ICxCON2 (Input Capture x Control 2).....	191
CxRXFnEID (CANx Acceptance Filter n Extended Identifier).....	268	INTCON1 (Interrupt Control 1).....	103
CxRXFnSID (CANx Acceptance Filter n Standard Identifier).....	268	INTCON2 (Interrupt Control 2).....	105
CxRXFUL1 (CANx Receive Buffer Full 1).....	272	INTCON3 (Interrupt Control 3).....	106
CxRXFUL2 (CANx Receive Buffer Full 2).....	272	INTCON4 (Interrupt Control 4).....	107
CxRXMnEID (CANx Acceptance Filter Mask n Extended Identifier).....	271	INTTREG (Interrupt Control and Status).....	108
CxRXMnSID (CANx Acceptance Filter Mask n Standard Identifier).....	271	IOCONx (PWMx I/O Control).....	213
CxRXOVF1 (CANx Receive Buffer Overflow 1).....	273	LEBCONx (PWMx Leading-Edge Blanking Control).....	217
CxRXOVF2 (CANx Receive Buffer Overflow 2).....	273	LEBDLYx (PWMx Leading-Edge Blanking Delay).....	218
CxTRmnCON (CANx TX/RX Buffer mn Control).....	274	MDC (PWMx Master Duty Cycle).....	207
CxVEC (CANx Interrupt Code).....	257	NVMADR (NVM Lower Address).....	88
DEVID (Device ID).....	323	NVMADRU (NVM Upper Address).....	88
DEVREV (Device Revision).....	323	NVMCON (NVM Control).....	86
DMALCA (DMA Last Channel Active Status).....	120	NVMKEY (NVM Key).....	89
DMA PPS (DMA Ping-Pong Status).....	121	NVMSRCADRH (NVM Data Memory Upper Address).....	90
DMA PWC (DMA Peripheral Write Collision Status).....	118	NVMSRCADRL (NVM Data Memory Lower Address).....	90
DMA RQC (DMA Request Collision Status).....	119	OCxCON1 (Output Compare x Control 1).....	194
DMAxCNT (DMA Channel x Transfer Count).....	116	OCxCON2 (Output Compare x Control 2).....	196
DMAxCON (DMA Channel x Control).....	112	OSCCON (Oscillator Control).....	126
DMAxPAD (DMA Channel x Peripheral Address).....	116	OSCTUN (FRC Oscillator Tuning).....	131
DMAxREQ (DMA Channel x IRQ Select).....	113	PDCx (PWMx Generator Duty Cycle).....	210
DMAxSTAH (DMA Channel x Start Address A, High).....	114	PHASEx (PWMx Primary Phase-Shift).....	210
DMAxSTAL (DMA Channel x Start Address A, Low).....	114	PLLFBF (PLL Feedback Divisor).....	130
DMAxSTBH (DMA Channel x Start Address B, High).....	115	PMD1 (Peripheral Module Disable Control 1).....	136
DMAxSTBL (DMA Channel x Start Address B, Low).....	115	PMD2 (Peripheral Module Disable Control 2).....	137
DMTCLR (Deadman Timer Clear).....	183	PMD3 (Peripheral Module Disable Control 3).....	138
DMTCNTH (Deadman Timer Count High).....	185	PMD4 (Peripheral Module Disable Control 4).....	138
DMTCNTL (Deadman Timer Count Low).....	185	PMD6 (Peripheral Module Disable Control 6).....	139
DMTCON (Deadman Timer Control).....	182	PMD7 (Peripheral Module Disable Control 7).....	140
DMTHOLDREG (DMT Hold).....	188	PMD8 (Peripheral Module Disable Control 8).....	141
DMTPRECLR (Deadman Timer Preclear).....	182	PTCON (PWMx Time Base Control).....	204
DMTPSCNTH (DMT Post Configure Count Status High).....	186	PTCON2 (PWMx Primary Master Clock Divider Select).....	205
DMTPSCNTL (DMT Post Configure Count Status Low).....	186	PTPER (PWMx Primary Master Time Base Period).....	206
DMTPSINTVH (DMT Post Configure Interval Status High).....	187	PWMCONx (PWMx Control).....	208
DMTPSINTVL (DMT Post Configure Interval Status Low).....	187	RCON (Reset Control).....	93
DMTSTAT (Deadman Timer Status).....	184	REFOCON (Reference Oscillator Control).....	132
DSADRH (DMA Most Recent RAM High Address).....	117	RPINR0 (Peripheral Pin Select Input 0).....	153
DSADRL (DMA Most Recent RAM Low Address).....	117	RPINR1 (Peripheral Pin Select Input 1).....	153
DTRx (PWMx Dead-Time).....	211	RPINR11 (Peripheral Pin Select Input 11).....	157
FCLCONx (PWMx Fault Current-Limit Control).....	215	RPINR12 (Peripheral Pin Select Input 12).....	158
I2CxCON1 (I2Cx Control 1).....	231	RPINR18 (Peripheral Pin Select Input 18).....	159
I2CxCON2 (I2Cx Control 2).....	233	RPINR19 (Peripheral Pin Select Input 19).....	159
		RPINR22 (Peripheral Pin Select Input 22).....	160
		RPINR23 (Peripheral Pin Select Input 23).....	161
		RPINR26 (Peripheral Pin Select Input 26).....	161
		RPINR3 (Peripheral Pin Select Input 3).....	154
		RPINR37 (Peripheral Pin Select Input 37).....	162
		RPINR38 (Peripheral Pin Select Input 38).....	162
		RPINR39 (Peripheral Pin Select Input 39).....	163
		RPINR44 (Peripheral Pin Select Input 44).....	164
		RPINR45 (Peripheral Pin Select Input 45).....	164
		RPINR7 (Peripheral Pin Select Input 7).....	155
		RPINR8 (Peripheral Pin Select Input 8).....	156
		RPOR0 (Peripheral Pin Select Output 0).....	165
		RPOR1 (Peripheral Pin Select Output 1).....	165
		RPOR10 (Peripheral Pin Select Output 10).....	170