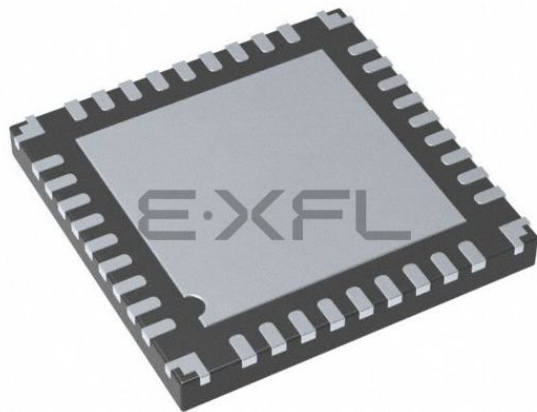




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm103t-i-m5

TABLE 4-7: ADC1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
ADC1BUF0	0300	ADC1 Data Buffer 0																	xxxx	
ADC1BUF1	0302	ADC1 Data Buffer 1																	xxxx	
ADC1BUF2	0304	ADC1 Data Buffer 2																	xxxx	
ADC1BUF3	0306	ADC1 Data Buffer 3																	xxxx	
ADC1BUF4	0308	ADC1 Data Buffer 4																	xxxx	
ADC1BUF5	030A	ADC1 Data Buffer 5																	xxxx	
ADC1BUF6	030C	ADC1 Data Buffer 6																	xxxx	
ADC1BUF7	030E	ADC1 Data Buffer 7																	xxxx	
ADC1BUF8	0310	ADC1 Data Buffer 8																	xxxx	
ADC1BUF9	0312	ADC1 Data Buffer 9																	xxxx	
ADC1BUFA	0314	ADC1 Data Buffer 10																	xxxx	
ADC1BUFB	0316	ADC1 Data Buffer 11																	xxxx	
ADC1BUFC	0318	ADC1 Data Buffer 12																	xxxx	
ADC1BUFD	031A	ADC1 Data Buffer 13																	xxxx	
ADC1BUFE	031C	ADC1 Data Buffer 14																	xxxx	
ADC1BUFF	031E	ADC1 Data Buffer 15																	xxxx	
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000		
AD1CON2	0322	VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0	BUFS	SMP14	SMP13	SMP12	SMP11	SMP10	BUFM	ALTS	0000		
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000		
AD1CHS123	0326	—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000		
AD1CHS0	0328	CH0NB	—	CH0SB5	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000		
AD1CSSH	032E	CSS<31:24>									—	—	—	—	CSS<19:16>					0000
AD1CSSL	0330	CSS<15:0>																	0000	
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	—	DMABL2	DMABL1	DMABL0	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: CTMU REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUICON	033E	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM002/102 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR10	0684	—	—	RP176R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM004/104 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR5	067A	—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0	0000
RPOR6	067C	—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0	0000
RPOR7	067E	—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0	0000
RPOR10	0684	—	—	RP176R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit
1 = An Illegal Opcode detection or an Illegal Address mode, or Uninitialized W register used as an Address Pointer caused a Reset
0 = An Illegal Opcode Reset or Uninitialized W Register Reset has not occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep mode
0 = Flash voltage regulator goes into Standby mode during Sleep mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred
- bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
1 = WDT is enabled
0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	NSTDIS: Interrupt Nesting Disable bit 1 = Interrupt nesting is disabled 0 = Interrupt nesting is enabled
bit 14	OVAERR: Accumulator A Overflow Trap Flag bit 1 = Trap was caused by overflow of Accumulator A 0 = Trap was not caused by overflow of Accumulator A
bit 13	OVBERR: Accumulator B Overflow Trap Flag bit 1 = Trap was caused by overflow of Accumulator B 0 = Trap was not caused by overflow of Accumulator B
bit 12	COVAERR: Accumulator A Catastrophic Overflow Trap Flag bit 1 = Trap was caused by catastrophic overflow of Accumulator A 0 = Trap was not caused by catastrophic overflow of Accumulator A
bit 11	COVBERR: Accumulator B Catastrophic Overflow Trap Flag bit 1 = Trap was caused by catastrophic overflow of Accumulator B 0 = Trap was not caused by catastrophic overflow of Accumulator B
bit 10	OVATE: Accumulator A Overflow Trap Enable bit 1 = Trap overflow of Accumulator A 0 = Trap is disabled
bit 9	OVBTE: Accumulator B Overflow Trap Enable bit 1 = Trap overflow of Accumulator B 0 = Trap is disabled
bit 8	COVTE: Catastrophic Overflow Trap Enable bit 1 = Trap on catastrophic overflow of Accumulator A or B is enabled 0 = Trap is disabled
bit 7	SFTACERR: Shift Accumulator Error Status bit 1 = Math error trap was caused by an invalid accumulator shift 0 = Math error trap was caused by an invalid accumulator shift
bit 6	DIV0ERR: Divide-by-Zero Error Status bit 1 = Math error trap was caused by a divide-by-zero 0 = Math error trap was not caused by a divide-by-zero
bit 5	DMACERR: DMAC Trap Flag bit 1 = DMAC trap has occurred 0 = DMAC trap has not occurred
bit 4	MATHERR: Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred

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REGISTER 14-9: DMTPSINTVL: DMT POST CONFIGURE INTERVAL STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

PSINTV<15:0>: Lower DMT Window Interval Configuration Status bits

This is always the value of the FDMTINTVL Configuration register.

REGISTER 14-10: DMTPSINTVH: DMT POST CONFIGURE INTERVAL STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

PSINTV<31:16>: Higher DMT Window Interval Configuration Status bits

This is always the value of the FDMTINTVH Configuration register.

dsPIC33EVXXXGM00X/10X FAMILY

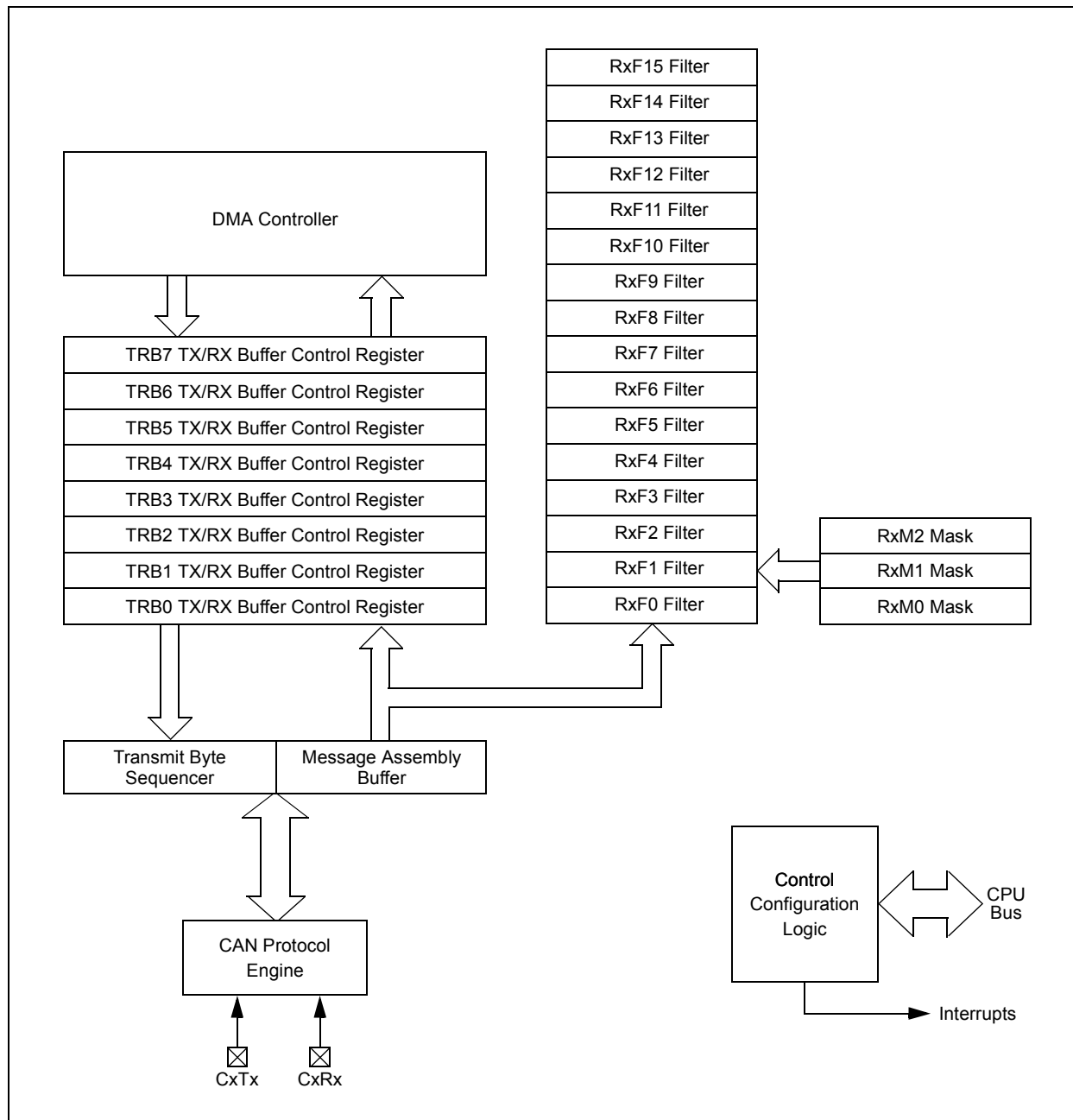
REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator x bits
- 11111 = Fault 32 (**default**)
 - 11110 = Reserved
 -
 -
 -
 - 01100 = Op Amp/Comparator 5
 - 01011 = Comparator 4
 - 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Fault 8
 - 00110 = Fault 7
 - 00101 = Fault 6
 - 00100 = Fault 5
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2
 - 00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator x bit⁽²⁾
- 1 = The selected Fault source is active-low
 - 0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator x bits
- 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT<1:0> values (cycle)
 - 00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT<1:0> values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FDEVOP<0>) is a '1', the FCLCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 22-1: CANx MODULE BLOCK DIAGRAM



22.2 Modes of Operation

The CANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit 1 = Transmitter is in Bus Off state 0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit 1 = Transmitter is in Bus Passive state 0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit 1 = Receiver is in Bus Passive state 0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit 1 = Transmitter is in Error Warning state 0 = Transmitter is not in Error Warning state
bit 9	RXWAR: Receiver in Error State Warning bit 1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit 1 = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIF: Invalid Message Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8> register) 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

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REGISTER 22-8: CxEC: CANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15							
bit 8							

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>**: Receive Error Count bits

REGISTER 22-9: CxCFG1: CANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

11 1111 = T_Q = 2 x 64 x 1/FCAN

•

•

•

00 0010 = T_Q = 2 x 3 x 1/FCAN

00 0001 = T_Q = 2 x 2 x 1/FCAN

00 0000 = T_Q = 2 x 1 x 1/FCAN

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator x Filter Input Clock Select bits

111 = T5CLK⁽¹⁾

110 = T4CLK⁽²⁾

101 = T3CLK⁽¹⁾

100 = T2CLK⁽²⁾

011 = Reserved

010 = SYNCO1⁽³⁾

001 = Fosc⁽⁴⁾

000 = Fp⁽⁴⁾

bit 3 **CFLTREN:** Comparator x Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator x Filter Clock Divide Select bits

111 = Clock divide 1:128

110 = Clock divide 1:64

101 = Clock divide 1:32

100 = Clock divide 1:16

011 = Clock divide 1:8

010 = Clock divide 1:4

001 = Clock divide 1:2

000 = Clock divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).

2: See the Type B Timer Block Diagram (Figure 13-1).

3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 17-2).

4: See the Oscillator System Diagram (Figure 9-1).

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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
46	MAC	MAC $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd, AWB$	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd$	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
47	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV $f, WREG$	Move f to WREG	1	1	None
		MOV $\#lit16, Wn$	Move 16-bit literal to Wn	1	1	None
		MOV.b $\#lit8, Wn$	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV $WREG, f$	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from $W(ns):W(ns + 1)$ to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to $W(nd + 1):W(nd)$	1	2	None
48	MOVPG	MOVPG $\#lit10, DSRPAG$	Move 10-bit literal to DSRPAG	1	1	None
		MOVPG $\#lit9, DSWPAG$	Move 9-bit literal to DSWPAG	1	1	None
		MOVPG $\#lit8, TBLPAG$	Move 8-bit literal to TBLPAG	1	1	None
		MOVPGW $Ws, DSRPAG$	Move $Ws<9:0>$ to DSRPAG	1	1	None
		MOVPGW $Ws, DSWPAG$	Move $Ws<8:0>$ to DSWPAG	1	1	None
		MOVPGW $Ws, TBLPAG$	Move $Ws<7:0>$ to TBLPAG	1	1	None
49	MOVSAC	MOVSAC $Acc, Wx, Wxd, Wy, Wyd, AWB$	Prefetch and store accumulator	1	1	None
50	MPY	MPY $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd$	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
51	MPY.N	MPY.N $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	-(Multiply Wm by Wn) to Accumulator	1	1	None
52	MSC	MSC $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd, AWB$	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 30-9: DC CHARACTERISTICS: DOZE CURRENT (IDOE)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	Typ. ⁽²⁾	Max.	Doze Ratio	Units	Conditions		
Doze Current (IDOE) ⁽¹⁾							
DC73a	16.0	18.25	1:2	mA	-40°C	5.0V	70 MIPS
DC73g	7.1	8.0	1:128	mA			
DC70a	16.25	18.5	1:2	mA	+25°C	5.0V	70 MIPS
DC70g	7.3	8.2	1:128	mA			
DC71a	17.0	19.0	1:2	mA	+85°C	5.0V	70 MIPS
DC71g	7.5	8.9	1:128	mA			
DC72a	17.75	19.95	1:2	mA	+125°C	5.0V	60 MIPS
DC72g	8.25	9.32	1:128	mA			

Note 1: IDOE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLK0 is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
  NOP();
}
```

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

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TABLE 30-50: OP AMP/COMPARATOR x SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Comparator AC Characteristics							
CM10	TRESP	Response Time	—	19	80	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	
Comparator DC Characteristics							
CM30	VOFFSET	Comparator Offset Voltage	-80	±60	80	mV	
CM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/Fall Time	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp AC Characteristics							
CM20	SR	Slew Rate	—	9	—	V/μs	10 pF load
CM21	PM	Phase Margin	—	35	—	°C	G = 100V/V, 10 pF load
CM22	GM	Gain Margin	—	20	—	db	G = 100V/V, 10 pF load
CM23	GBW	Gain Bandwidth	—	10	—	MHz	10 pF load
Op Amp DC Characteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio	—	45	—	db	VCM = AVDD/2
CM42	VOFFSET	Op Amp Offset Voltage	-50	±6	50	mV	
CM43	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM44	IOS	Input Offset Current	—	—	—	—	See pad leakage currents in Table 30-10
CM45	IB	Input Bias Current	—	—	—	—	See pad leakage currents in Table 30-10
CM46	IOUT	Output Current	—	—	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	—	—	kΩ	Note 2
CM49a	VOUT	Output Voltage	AVSS + 0.075	—	AVDD – 0.075	V	IOUT = 420 μA

Note 1: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

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TABLE 30-53: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
CTMU Current Source							
CTMUI1	IOUT1	Base Range	—	550	—	nA	CTMUICON<9:8> = 01
CTMUI2	IOUT2	10x Range	—	5.5	—	μA	CTMUICON<9:8> = 10
CTMUI3	IOUT3	100x Range	—	55	—	μA	CTMUICON<9:8> = 11
CTMUI4	IOUT4	1000x Range	—	550	—	μA	CTMUICON<9:8> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	—	0.525	—	V	TA = +25°C, CTMUICON<9:8> = 01
			—	0.585	—	V	TA = +25°C, CTMUICON<9:8> = 10
			—	0.645	—	V	TA = +25°C, CTMUICON<9:8> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change ^(1,2)	—	-1.92	—	mV/°C	CTMUICON<9:8> = 01
			—	-1.74	—	mV/°C	CTMUICON<9:8> = 10
			—	-1.56	—	mV/°C	CTMUICON<9:8> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

Note 2: Parameters are characterized but not tested in manufacturing. Measurements are taken with the following conditions:

- VREF = AVDD = 5.0V
- ADC configured for 10-bit mode
- ADC configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- CPU executing
while(1)
{
NOP();
}
- Device operating from the FRC with no PLL

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FIGURE 33-3: TYPICAL I_{DD} vs. V_{DD} (EC MODE, 20 MIPS)

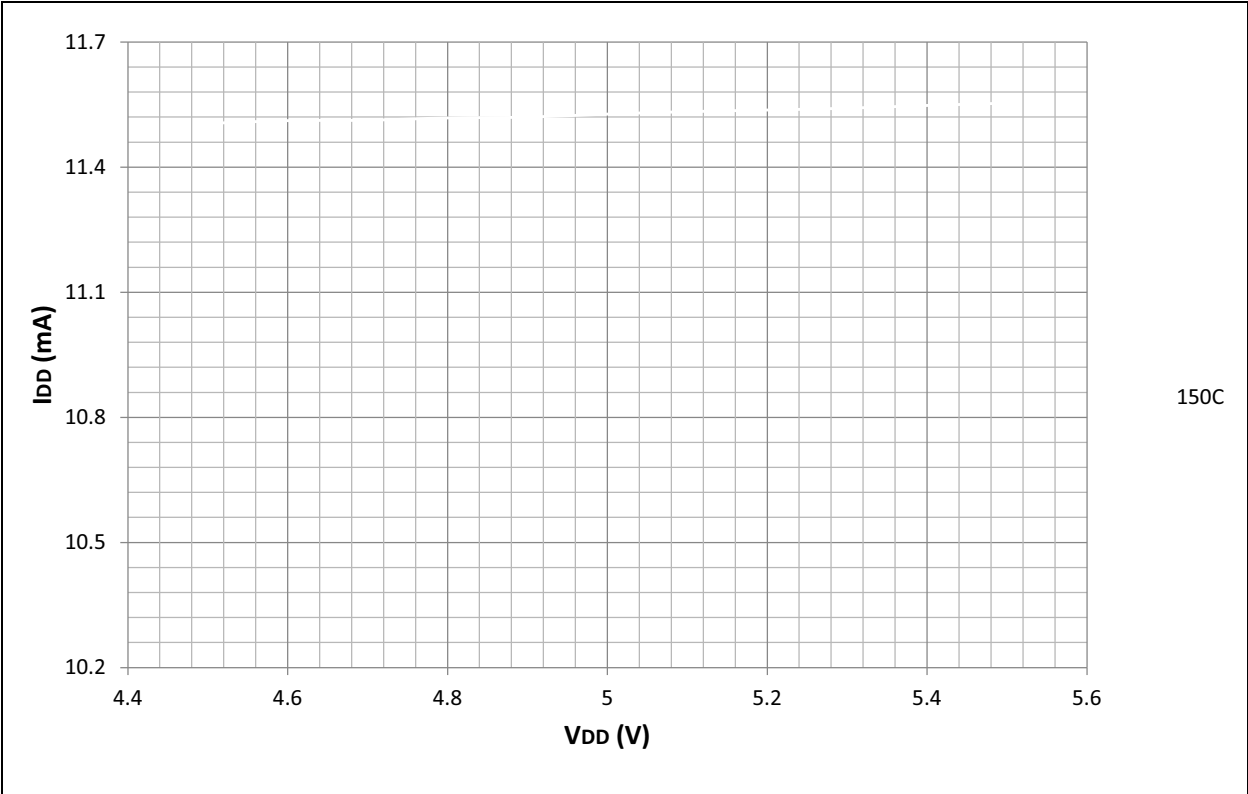
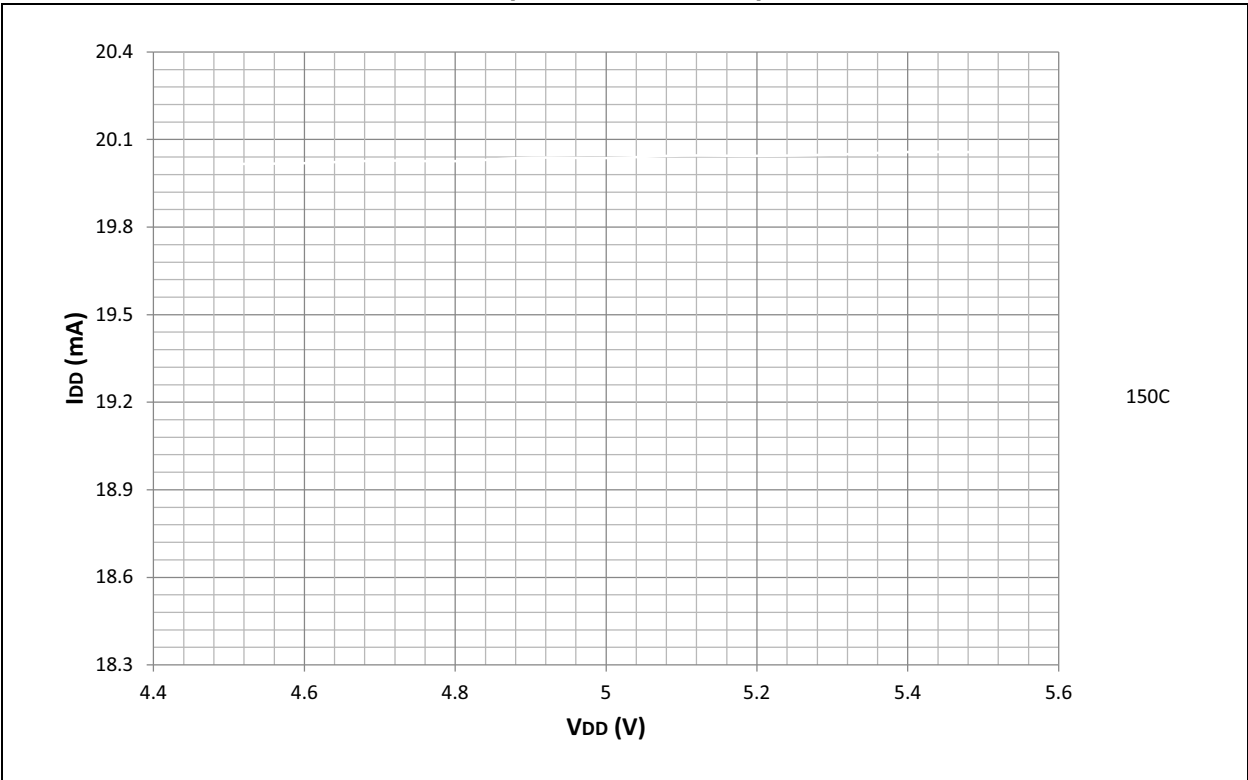


FIGURE 33-4: TYPICAL I_{DD} vs. V_{DD} (EC MODE, 40 MIPS)



33.14 Comparator Op Amp Offset

FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. V_{CM}

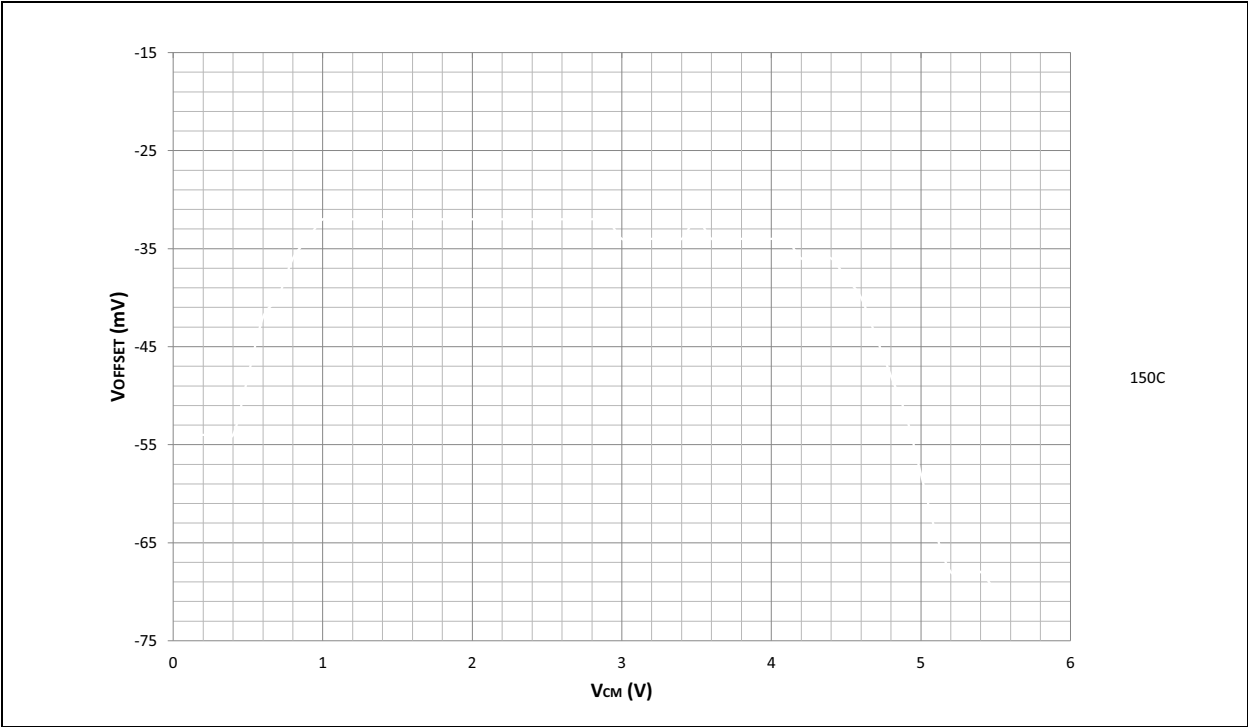
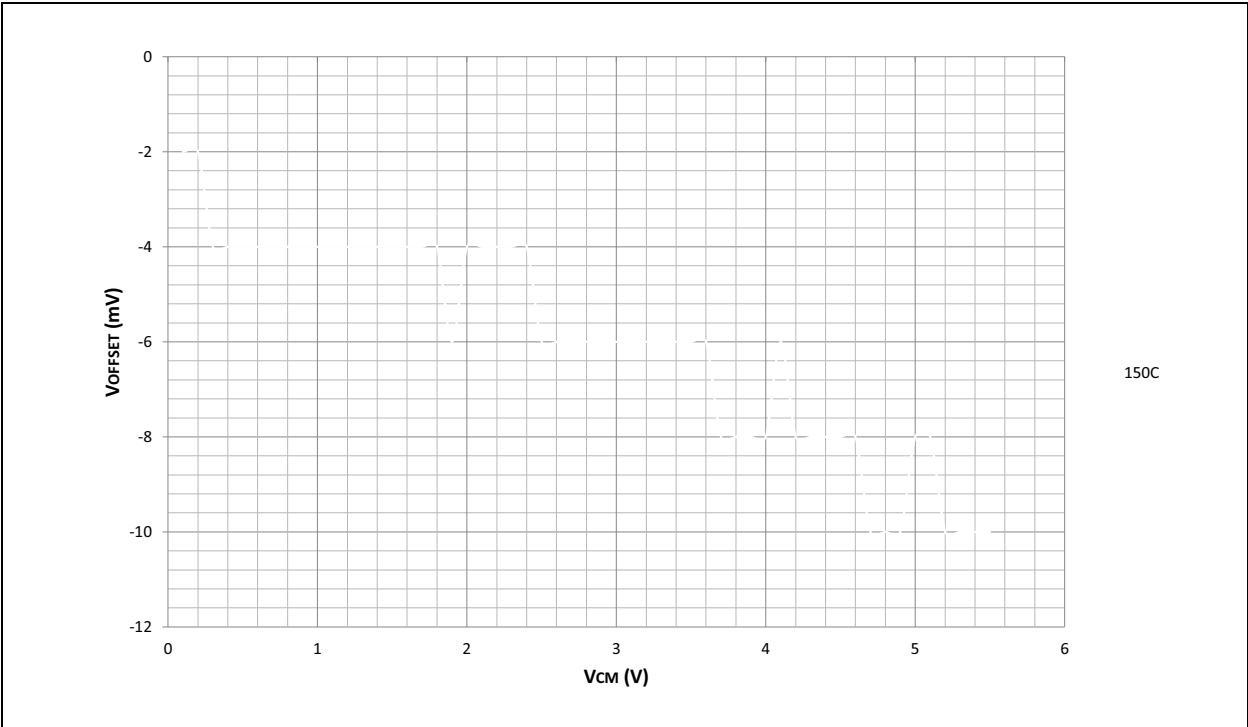


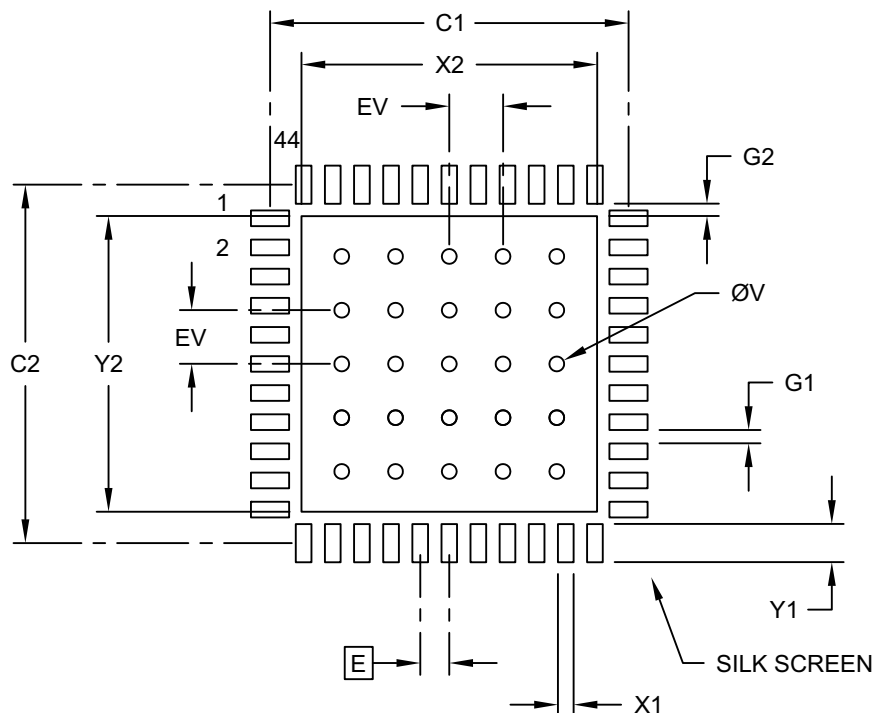
FIGURE 33-34: TYPICAL OP AMP OFFSET vs. V_{CM}



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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

dsPIC 33 EV XXX GM0 0X T PT - XXX Microchip Trademark Architecture Core Family Program Memory Size (Kbytes) Product Group Pin Count Tape and Reel Flag (if applicable) Package Pattern		Example: dsPIC33EV256GM006-I/PT: dsPIC33, Enhanced Voltage, 256-Kbyte Program Memory, 64-Pin, Industrial Temperature, TQFP Package.
Architecture: 33 = 16-Bit Digital Signal Controller Family: EV = Enhanced Voltage Product Group: GM = General Purpose plus Motor Control Family Pin Count: 02 = 28-Pin 04 = 44-Pin 06 = 64-Pin Temperature Range I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) H = -40°C to +150°C (High) Package: MM = Plastic Quad Flat, No Lead Package – (28-pin) 6x6x0.9 mm body (QFN-S) SO = Plastic Small Outline – (28-pin) 7.50 mm body (SOIC) SS = Plastic Shrink Small Outline – (28-pin) 5.30 mm body (SSOP) SP = Skinny Plastic Dual In-Line – (28-pin) 300 mil body (SPDIP) ML = Plastic Quad Flat, No Lead Package – (44-pin) 8x8 mm body (QFN) MR = Plastic Quad Flat, No Lead Package – (64-pin) 9x9x0.9 mm body (QFN) PT = Plastic Thin Quad Flatpack – (44-pin) 10x10x1 mm body (TQFP) PT = Plastic Thin Quad Flatpack – (64-pin) 10x10x1 mm body (TQFP)		