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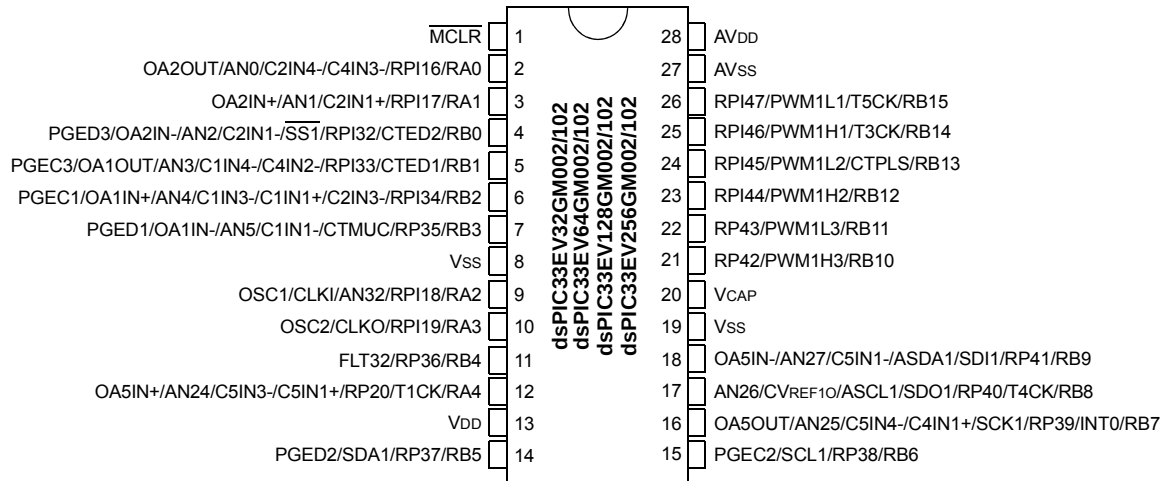
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev128gm104-i-ml

dsPIC33EVXXXGM00X/10X FAMILY

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP^(1,2,3)



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.5 “Peripheral Pin Select (PPS)”** for available peripherals and information on limitations.
- 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- 3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAX input is used; otherwise, the ANx input is used.

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REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	CCTXI2	CCTXI1	CCTXI0
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0	R/W-0
—	—	—	—	—	MCTXI2	MCTXI1	MCTXI0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCTXI<2:0>:** Current (W Register) Context Identifier bits

111 = Reserved

•
•
•

011 = Reserved

010 = Alternate Working Register Set 2 is currently in use

001 = Alternate Working Register Set 1 is currently in use

000 = Default register set is currently in use

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **MCTXI<2:0>:** Manual (W Register) Context Identifier bits

111 = Reserved

•
•
•

011 = Reserved

010 = Alternate Working Register Set 2 was most recently manually selected

001 = Alternate Working Register Set 1 was most recently manually selected

000 = Default register set was most recently manually selected

TABLE 4-7: ADC1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC1BUF0	0300	ADC1 Data Buffer 0																	xxxx
ADC1BUF1	0302	ADC1 Data Buffer 1																	xxxx
ADC1BUF2	0304	ADC1 Data Buffer 2																	xxxx
ADC1BUF3	0306	ADC1 Data Buffer 3																	xxxx
ADC1BUF4	0308	ADC1 Data Buffer 4																	xxxx
ADC1BUF5	030A	ADC1 Data Buffer 5																	xxxx
ADC1BUF6	030C	ADC1 Data Buffer 6																	xxxx
ADC1BUF7	030E	ADC1 Data Buffer 7																	xxxx
ADC1BUF8	0310	ADC1 Data Buffer 8																	xxxx
ADC1BUF9	0312	ADC1 Data Buffer 9																	xxxx
ADC1BUFA	0314	ADC1 Data Buffer 10																	xxxx
ADC1BUFB	0316	ADC1 Data Buffer 11																	xxxx
ADC1BUFC	0318	ADC1 Data Buffer 12																	xxxx
ADC1BUFD	031A	ADC1 Data Buffer 13																	xxxx
ADC1BUFE	031C	ADC1 Data Buffer 14																	xxxx
ADC1BUFF	031E	ADC1 Data Buffer 15																	xxxx
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD1CON2	0322	VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0	BUFS	SMPI4	SMPI3	SMPI2	SMP11	SMP10	BUFM	ALTS	0000	
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000	
AD1CHS123	0326	—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000	
AD1CHS0	0328	CH0NB	—	CH0SB5	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000	
AD1CSSH	032E	CSS<31:24>									—	—	—	—	CSS<19:16>				0000
AD1CSSL	0330	CSS<15:0>																	0000
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL2	DMABL1	DMABL0	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: CTMU REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUICON	033E	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: DMAC REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA0REQ	0B02	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA0STAL	0B04	STA<15:0>																0000
DMA0STAH	0B06	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA0STBL	0B08	STB<15:0>																0000
DMA0STBH	0B0A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA0PAD	0B0C	PAD<15:0>																0000
DMA0CNT	0B0E	—	—	CNT<13:0>														0000
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA1REQ	0B12	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA1STAL	0B14	STA<15:0>																0000
DMA1STAH	0B16	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA1STBL	0B18	STB<15:0>																0000
DMA1STBH	0B1A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA1PAD	0B1C	PAD<15:0>																0000
DMA1CNT	0B1E	—	—	CNT<13:0>														0000
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA2REQ	0B22	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA2STAL	0B24	STA<15:0>																0000
DMA2STAH	0B26	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA2STBL	0B28	STB<15:0>																0000
DMA2STBH	0B2A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA2PAD	0B2C	PAD<15:0>																0000
DMA2CNT	0B2E	—	—	CNT<13:0>														0000
DMA3CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA3REQ	0B32	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA3STAL	0B34	STA<15:0>																0000
DMA3STAH	0B36	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA3STBL	0B38	STB<15:0>																0000
DMA3STBH	0B3A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA3PAD	0B3C	PAD<15:0>																0000
DMA3CNT	0B3E	—	—	CNT<13:0>														0000
DMA3PWC	0BF0	—	—	—	—	—	—	—	—	—	—	—	—	PWCOL<3:0>				0000
DMA3RQC	0BF2	—	—	—	—	—	—	—	—	—	—	—	—	RQCOL<3:0>				0000
DMA3PPS	0BF4	—	—	—	—	—	—	—	—	—	—	—	—	PPST<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXGM00X/10X FAMILY

4.3.1 PAGED MEMORY SCHEME

The dsPIC33EVXXGM00X/10X family architecture extends the available DS through a paging scheme, which allows the available DS to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the Base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Data Space Read Page register (DSRPAG) or the 9-bit Data Space Write Page register (DSWPAG), to form an EDS address, or Program Space Visibility (PSV) address.

The Data Space Page registers are located in the SFR space. Construction of the EDS address is shown in Figure 4-9 and Figure 4-10. When $DSRPAG<9> = 0$ and the base address bit, $EA<15> = 1$, the $DSRPAG<8:0>$ bits are concatenated onto $EA<14:0>$ to form the 24-bit EDS read address. Similarly, when the base address bit, $EA<15> = 1$, the $DSWPAG<8:0>$ bits are concatenated onto $EA<14:0>$ to form the 24-bit EDS write address.

FIGURE 4-9: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION

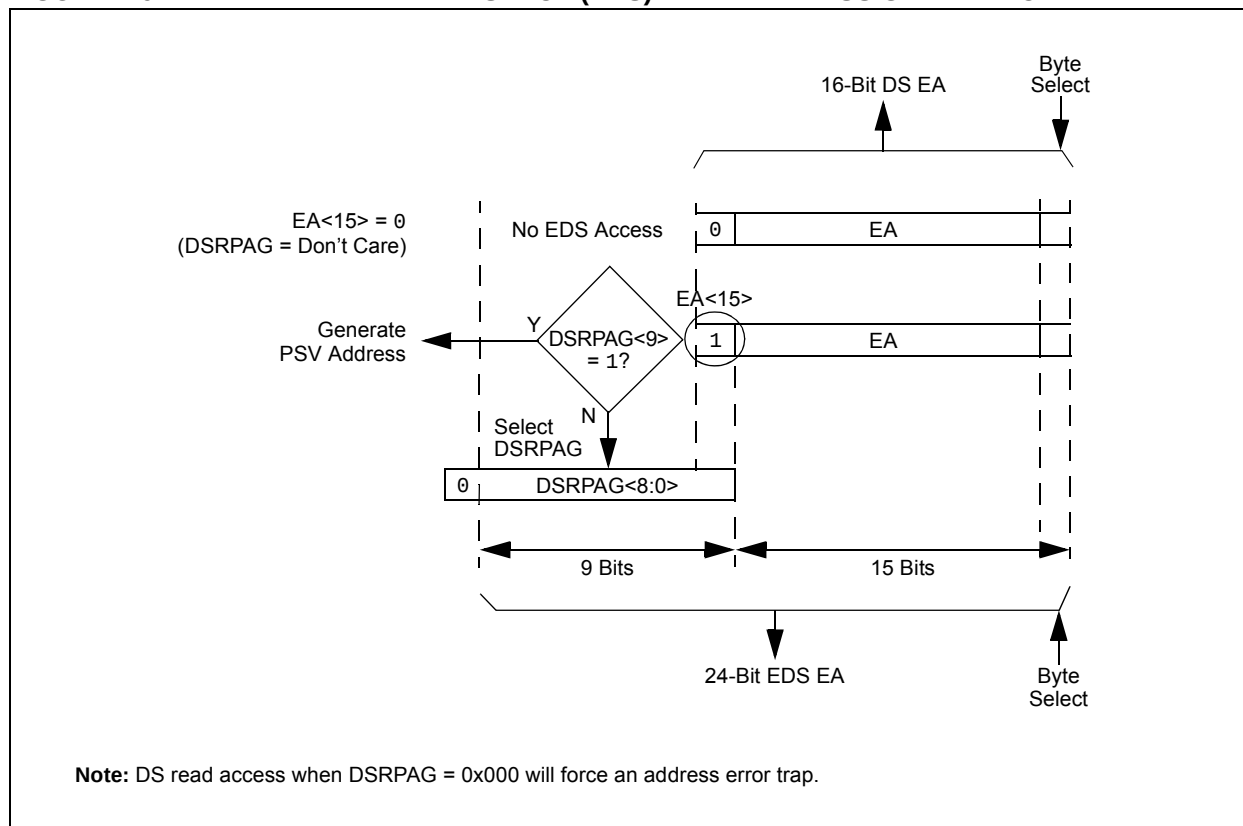
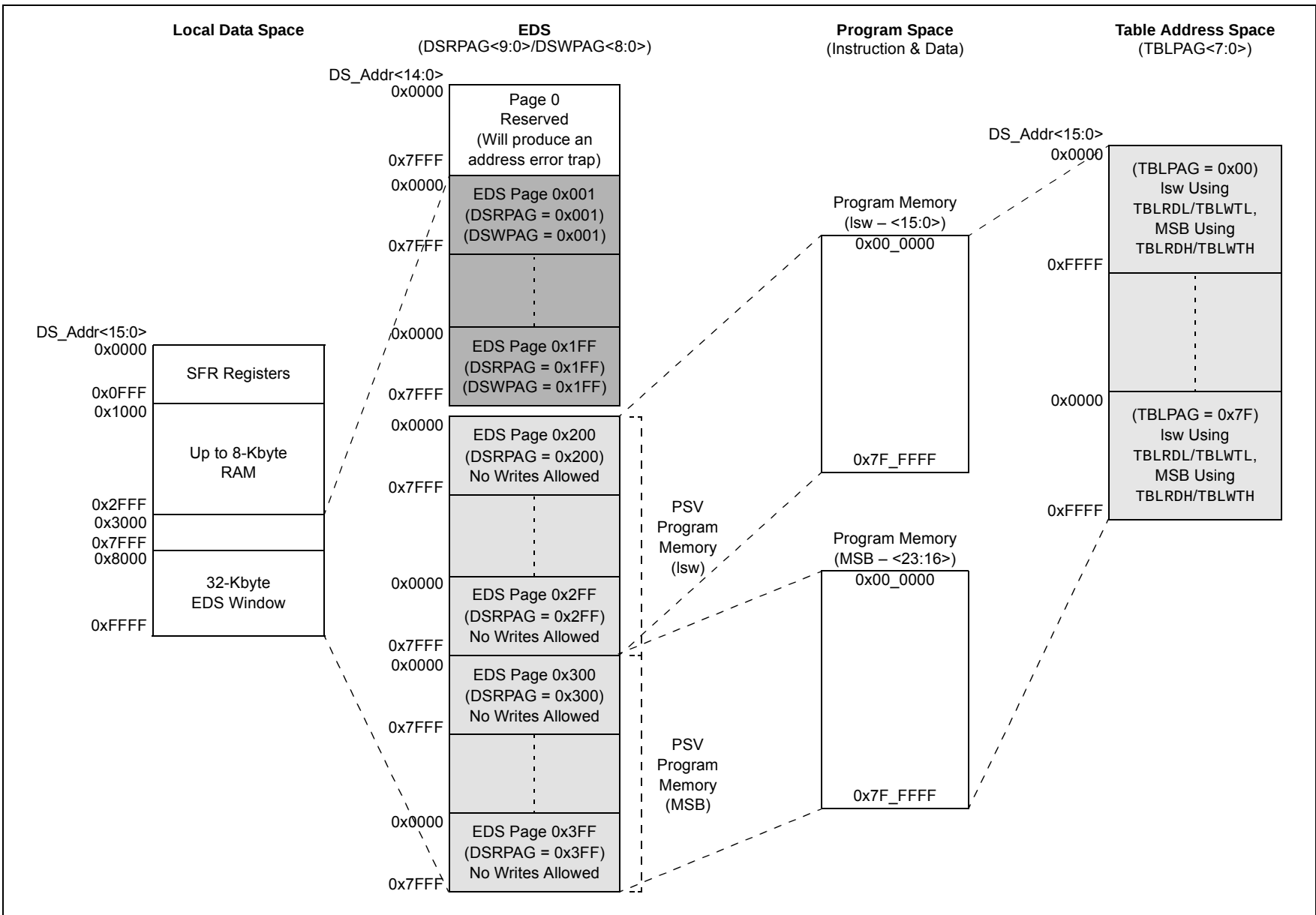


FIGURE 4-11: PAGED DATA MEMORY SPACE



dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

10.2.1 SLEEP MODE

The following events occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared before entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby mode when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following events occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

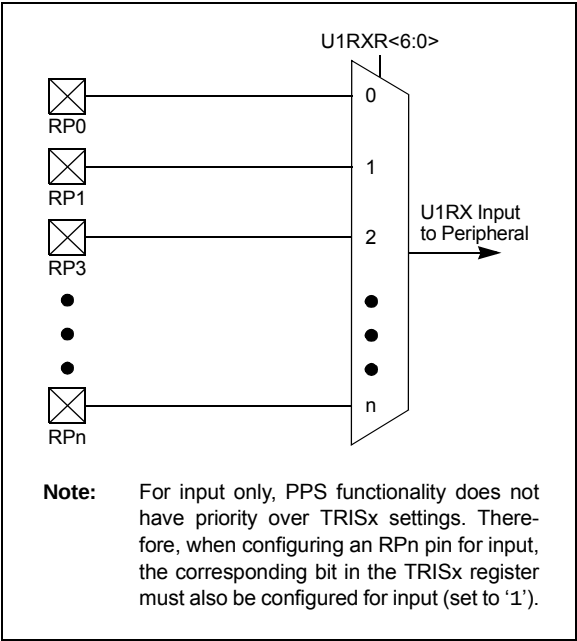
10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up either from Sleep mode or Idle mode.

dsPIC33EVXXXGM00X/10X FAMILY

For example, Figure 11-2 shows the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.5.4.1 Virtual Connections

dsPIC33EVXXXGM00X/10X family devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in Section 25.0 “Op Amp/Comparator Module”).

These devices provide six virtual output pins (RPV0-RPV5) that correspond to the outputs of six peripheral pin output remapper blocks (RP176-RP181). The six virtual remapper outputs (RP176-RP181) are not connected to actual pins. The six virtual pins may be read by any of the input remappers as inputs, RPI176-RPI181. These virtual pins can be used to connect the internal peripherals, whose signals are of significant use to the other peripherals, but these output signals are not present on the device pin.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<7:0> bits of the RPINR12 register to the value of 'b00000001', the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP57R<5:0>:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP56R<5:0>:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

- bit 6-4 **SYNCSRC<2:0>**: Synchronous Source Selection bits⁽¹⁾
 111 = Reserved
 •
 •
 •
 100 = Reserved
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = SYNC11 input from PPS
- bit 3-0 **SEVTPS<3:0>**: Special Event Trigger Output Postscaler Select bits⁽¹⁾
 1111 = 1:16 postscaler generates a Special Event Trigger on every sixteenth compare match event
 •
 •
 •
 0001 = 1:2 postscaler generates a Special Event Trigger on every second compare match event
 0000 = 1:1 postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNC11 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 17-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0> ⁽¹⁾		
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-3 **Unimplemented:** Read as '0'
- bit 2-0 **PCLKDIV<2:0>**: PWMx Input Clock Prescaler (Divider) Select bits⁽¹⁾
 111 = Reserved
 110 = Divide-by-64
 101 = Divide-by-32
 100 = Divide-by-16
 011 = Divide-by-8
 010 = Divide-by-4
 001 = Divide-by-2
 000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<15:8>							
bit 15				bit 8			

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<7:0>							
bit 7				bit 0			

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>**: Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<31:24>							
bit 15				bit 8			

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<23:16>							
bit 7				bit 0			

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>**: Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

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TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typ. ⁽²⁾	Max.	Units	Conditions		
Idle Current (I _{IDLE}) ⁽¹⁾						
DC40d	1.25	2	mA	-40°C	5.0V	10 MIPS
DC40a	1.25	2	mA	+25°C		
DC40b	1.5	2.6	mA	+85°C		
DC40c	1.5	2.6	mA	+125°C		
DC42d	2.3	3	mA	-40°C	5.0V	20 MIPS
DC42a	2.3	3	mA	+25°C		
DC42b	2.6	3.45	mA	+85°C		
DC42c	2.6	3.85	mA	+125°C		
DC44d	6.9	8	mA	-40°C	5.0V	70 MIPS
DC44a	6.9	8	mA	+25°C		
DC44b	7.25	8.6	mA	+85°C		

Note 1: Base Idle current (I_{IDLE}) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = V_{DD}, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

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FIGURE 30-6: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS

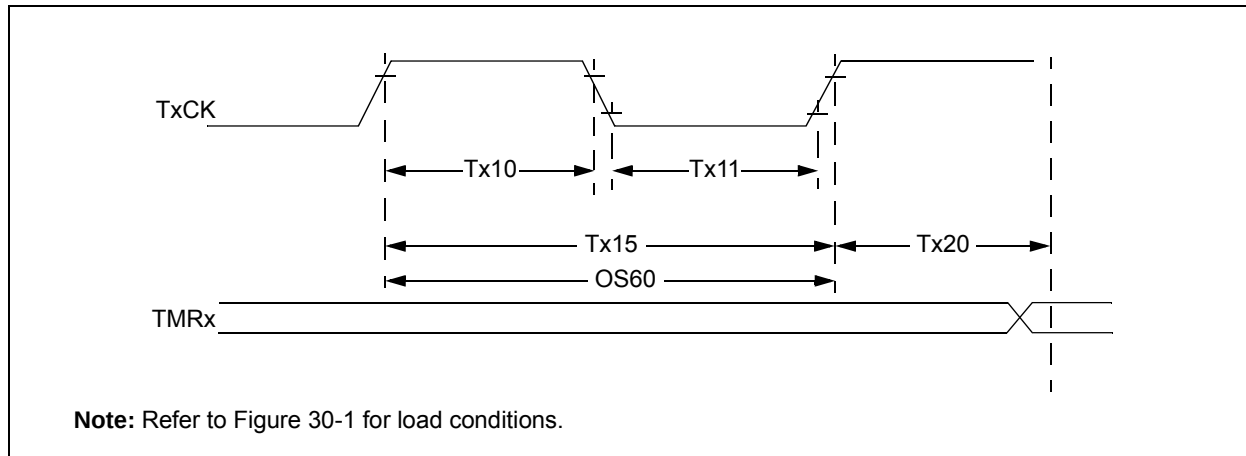


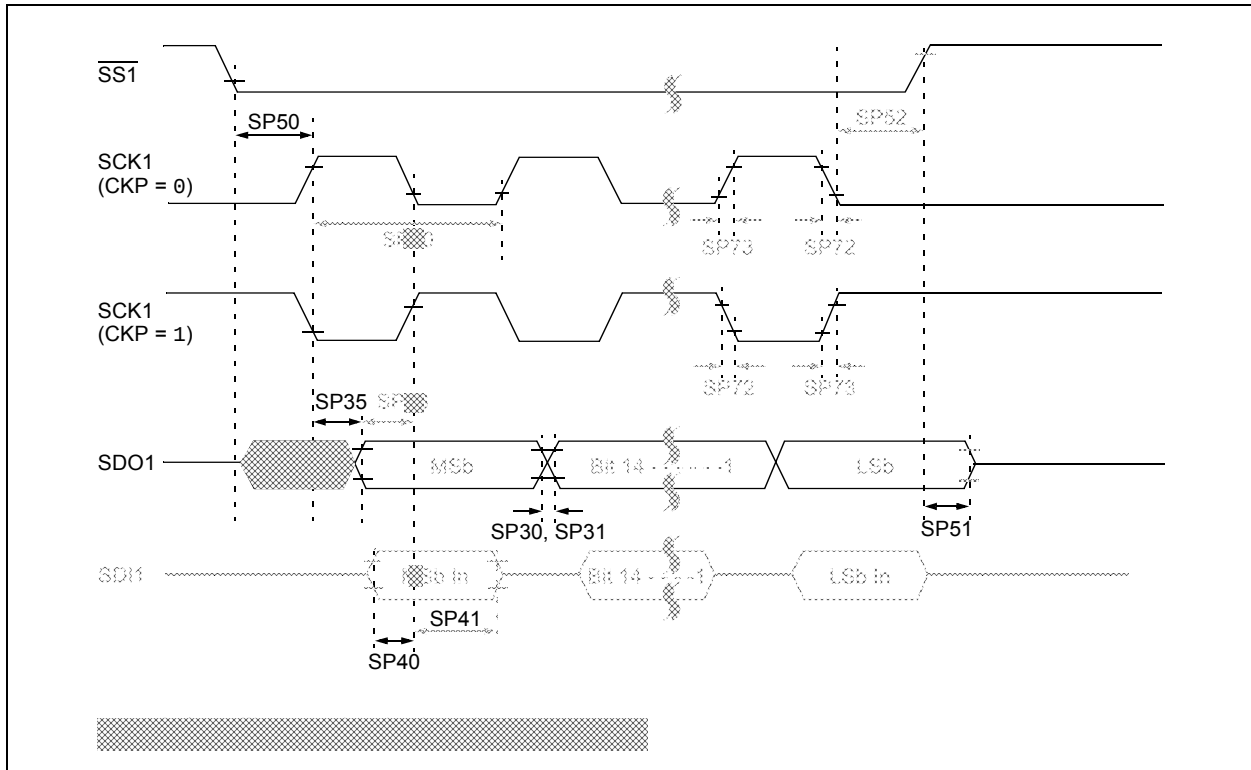
TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽²⁾		Min.	Typ.	Max.	Units	Conditions
TA10	TtxH	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256)
			Asynchronous mode	35	—	—	ns	
TA11	TtxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256)
			Asynchronous mode	10	—	—	ns	
TA15	TtxP	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS (T1CON<1>) bit)		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1: Timer1 is a Type A.

Note 2: These parameters are characterized but not tested in manufacturing.

FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



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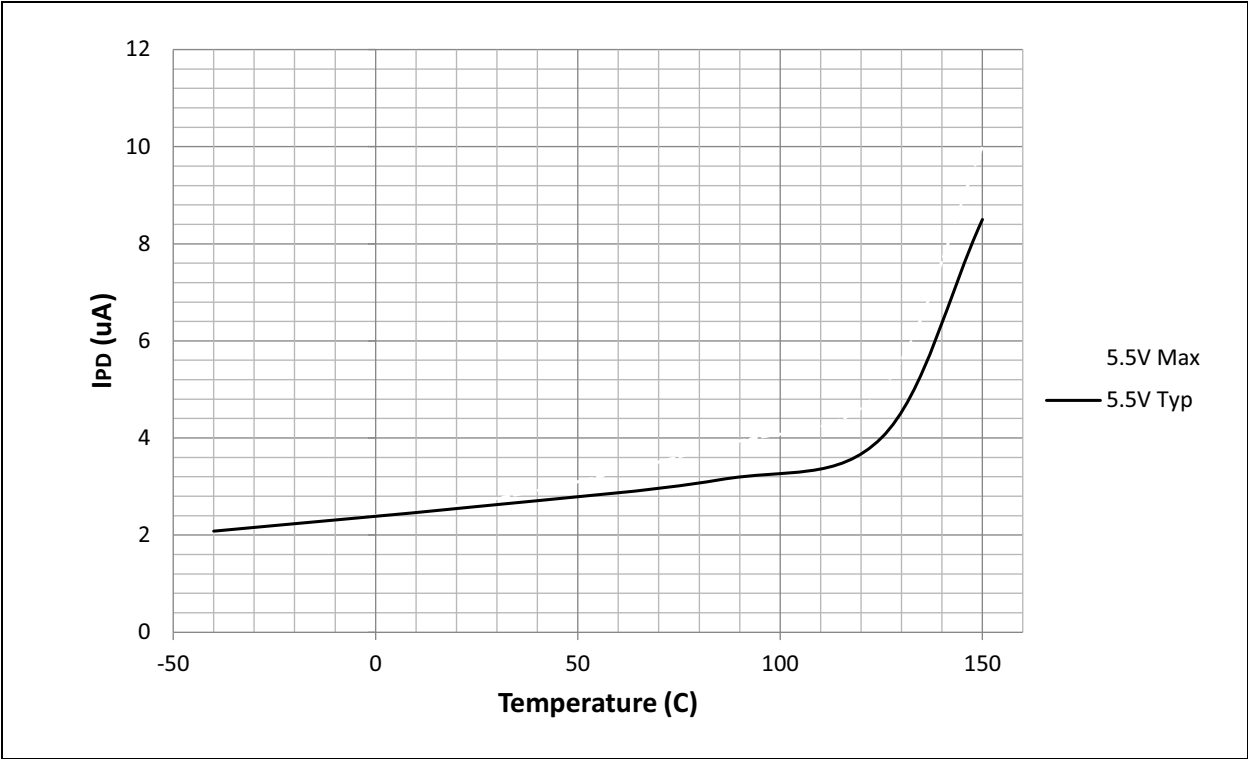
TABLE 30-57: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽⁴⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	117.6	—	—	ns	
AD51	trc	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14	—	TAD	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time when Sampling Any ANx Input	3	—	—	TAD	
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs	3	—	—	TAD	
Timing Parameters							
AD60	tpCS	Conversion Start from Sample Trigger ⁽¹⁾	2	—	3	TAD	Auto-convert trigger is not selected
AD61	tpSS	Sample Start from Setting Sample (SAMP) bit ⁽¹⁾	2	—	3	TAD	
AD62	tcSS	Conversion Completion to Sample Start (ASAM = 1) ⁽¹⁾	—	0.5	—	TAD	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽¹⁾	—	—	20	μs	See Note 3

- Note 1:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 2:** Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
- 3:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.
- 4:** These parameters are characterized but not tested in manufacturing.

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FIGURE 33-15: TYPICAL/MAXIMUM ΔI_{WDT} vs. TEMPERATURE



33.5 FRC

FIGURE 33-16: TYPICAL FRC ACCURACY vs. V_{DD}

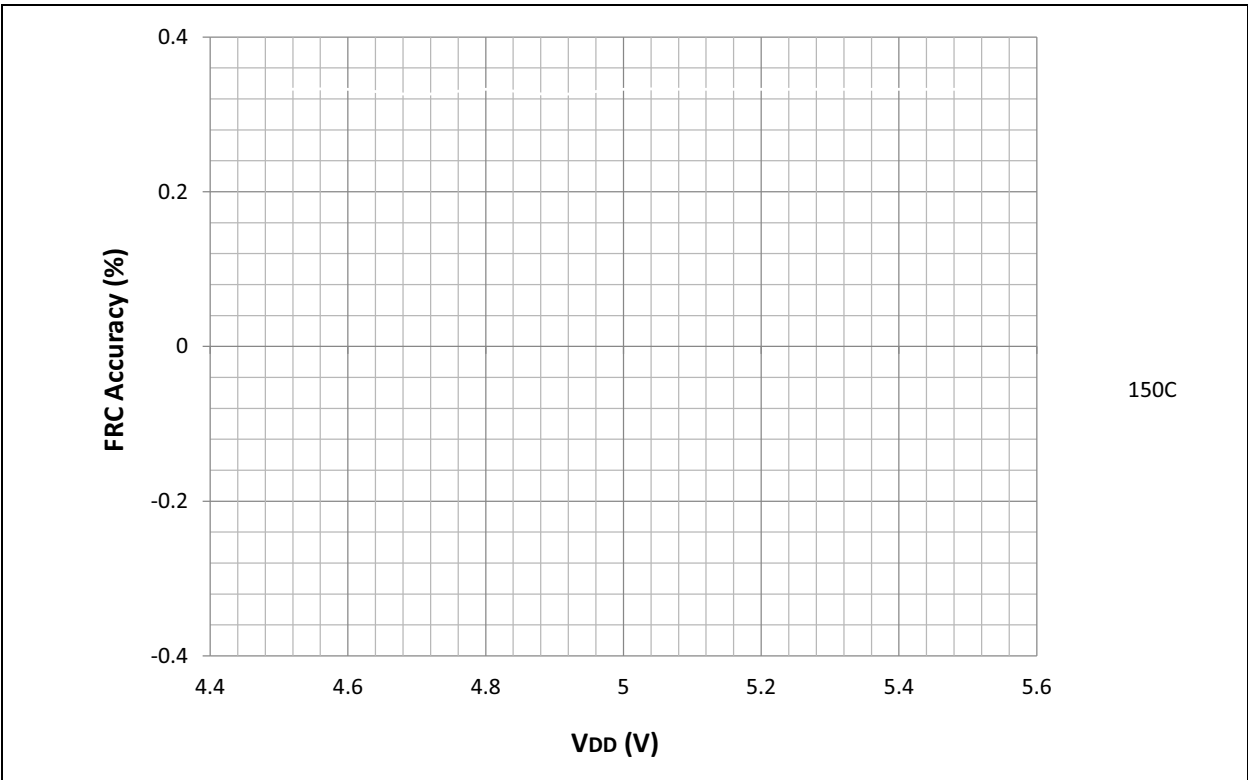
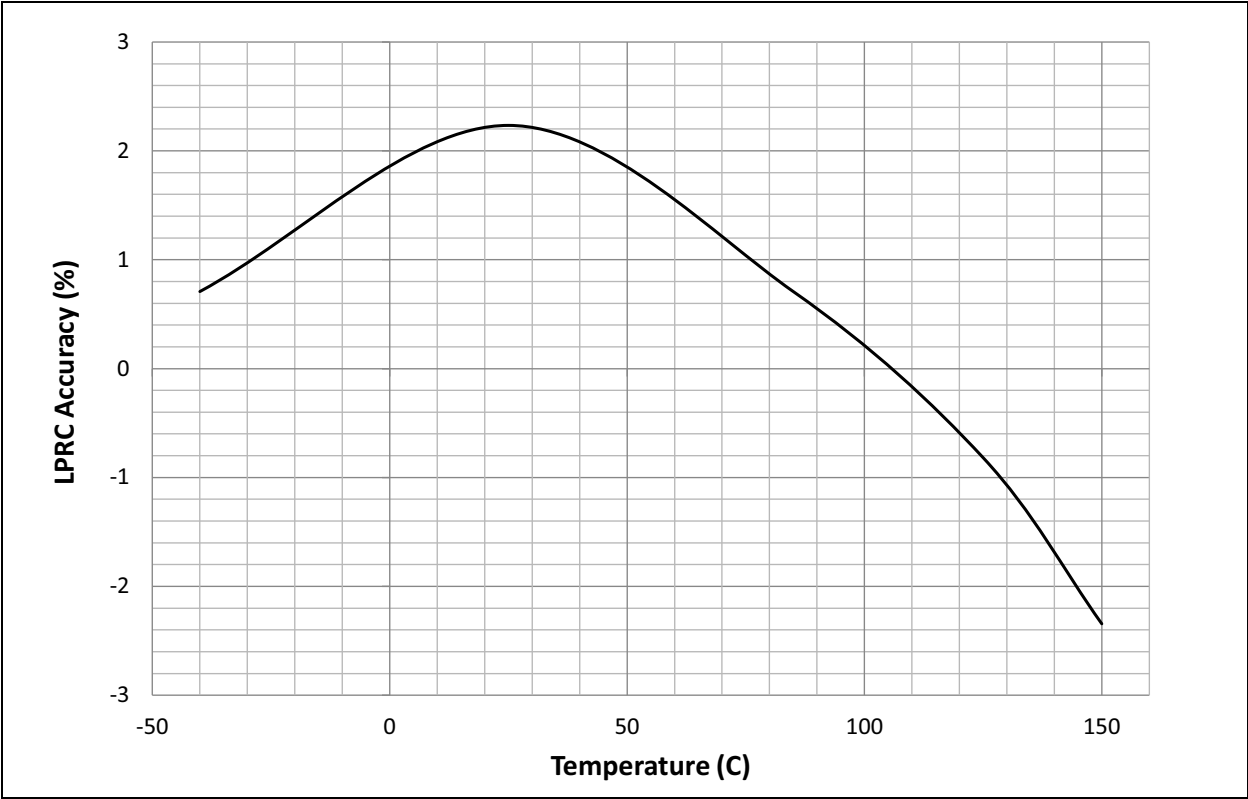
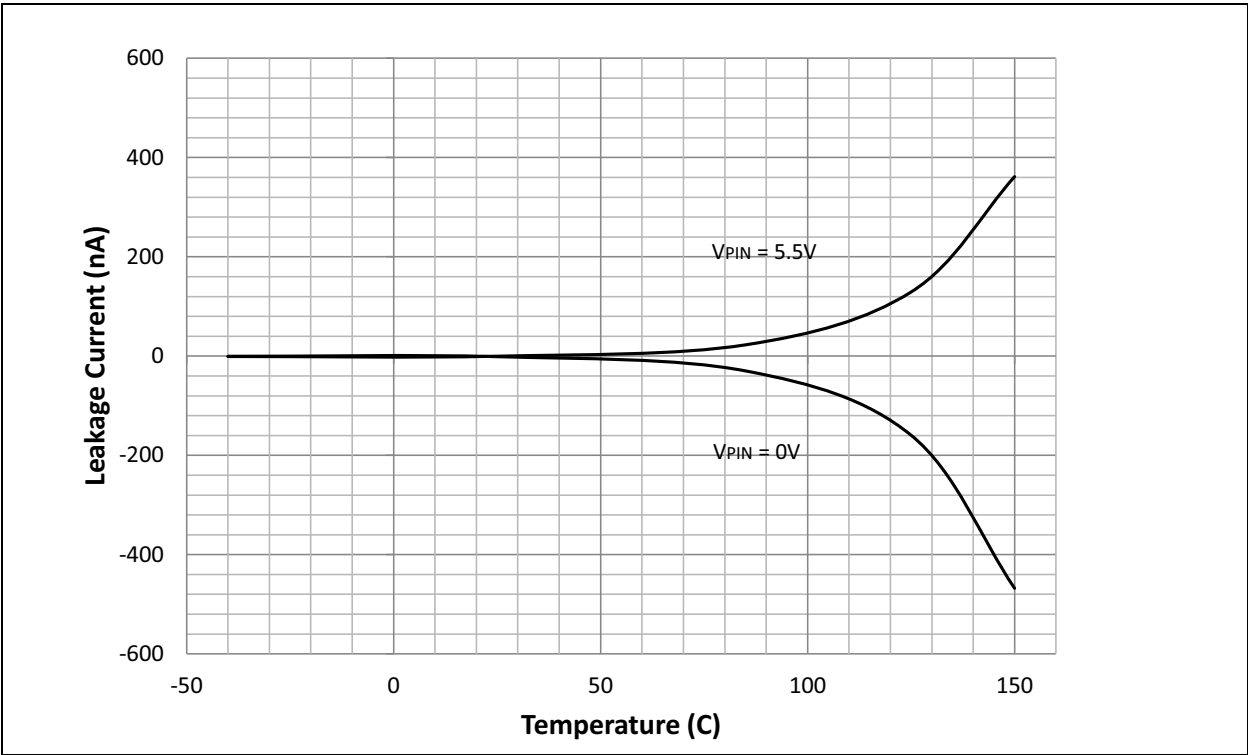


FIGURE 33-19: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V VDD)



33.7 Leakage Current

FIGURE 33-20: TYPICAL I_{IL} vs. TEMPERATURE ($\overline{\text{MCLR}}$)



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