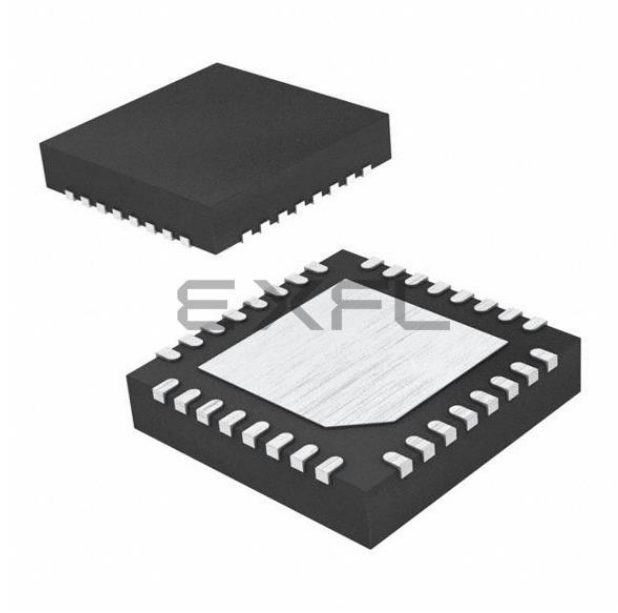
# Microchip Technology - DSPIC33EV256GM002-E/MM Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 11x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm002-e-mm |

## dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES

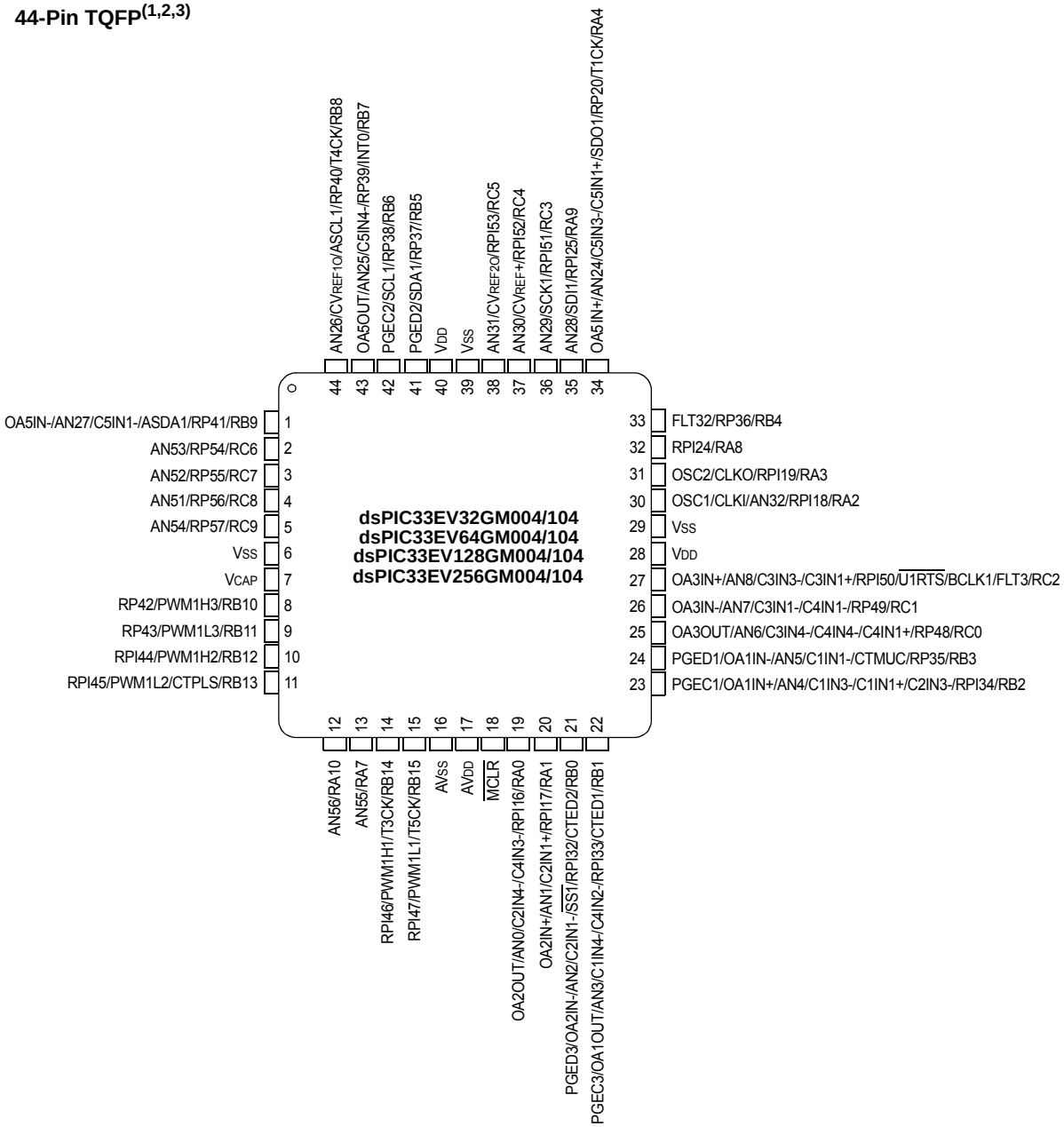
The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.

**TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES**

| Device | Program Memory Bytes | SRAM Bytes | CAN | DMA Channels | 16-Bit Timers (T1) | 32-Bit Timers | Input Capture | Output Compare | PWM | UART | SPI | $I^2C$ | SENT | 10/12-Bit ADC | ADC Inputs | Op Amp/Comparators | CTMU | Security | Peripheral Pin Select (PPS) | General Purpose I/O (GPIO) | External Interrupts | Pins | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| dsPIC33EV32GM002 | 32K | 4K | 0 | 4 | 5 | 2 | 4 | 4 | 3x2 | 2 | 2 | 1 | 2 | 1 | 11 | 3/4 | 1 | Intermediate | Y | 21 | 3 | 28 | SPDIP, SOIC, SSOP, QFN-S |
| dsPIC33EV32GM102 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM002 | 64K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM102 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM002 | 128K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM102 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM002 | 256K | 16K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM102 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV32GM004 | 32K | 4K | 0 | 4 | 5 | 2 | 4 | 4 | 3x2 | 2 | 2 | 1 | 2 | 1 | 24 | 4/5 | 1 | Intermediate | Y | 35 | 3 | 44 | TQFP, QFN |
| dsPIC33EV32GM104 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM004 | 64K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM104 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM004 | 128K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM104 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM004 | 256K | 16K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM104 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV32GM006 | 32K | 4K | 0 | 4 | 5 | 2 | 4 | 4 | 3x2 | 2 | 2 | 1 | 2 | 1 | 36 | 4/5 | 1 | Intermediate | Y | 53 | 3 | 64 | TQFP, QFN |
| dsPIC33EV32GM106 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM006 | 64K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV64GM106 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM006 | 128K | 8K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV128GM106 | | | 1 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM006 | 256K | 16K | 0 | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EV256GM106 | | | 1 | | | | | | | | | | | | | | | | | | | | |

## Pin Diagrams (Continued)

**44-Pin TQFP(1,2,3)**




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

**TABLE 4-26: DMAC REGISTER MAP**

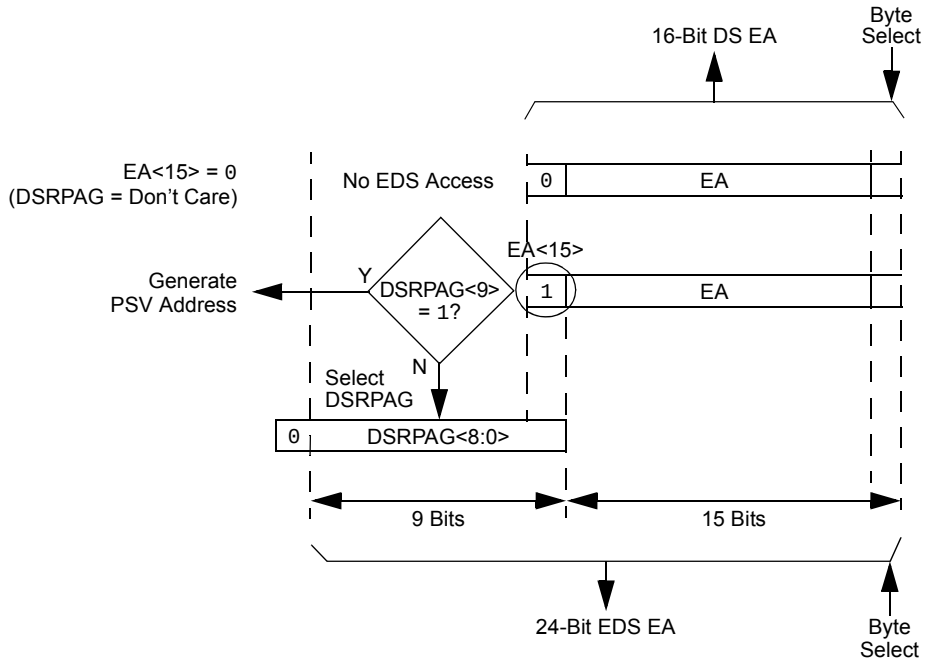
| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA0CON | 0B00 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 | 0000 |
| DMA0REQ | 0B02 | FORCE | — | — | — | — | — | — | — | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 | 00FF |
| DMA0STAL | 0B04 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STAH | 0B06 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA0STBL | 0B08 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STBH | 0B0A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA0PAD | 0B0C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0CNT | 0B0E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA1CON | 0B10 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 | 0000 |
| DMA1REQ | 0B12 | FORCE | — | — | — | — | — | — | — | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 | 00FF |
| DMA1STAL | 0B14 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STAH | 0B16 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA1STBL | 0B18 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STBH | 0B1A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA1PAD | 0B1C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1CNT | 0B1E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA2CON | 0B20 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 | 0000 |
| DMA2REQ | 0B22 | FORCE | — | — | — | — | — | — | — | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 | 00FF |
| DMA2STAL | 0B24 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STAH | 0B26 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA2STBL | 0B28 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STBH | 0B2A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA2PAD | 0B2C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2CNT | 0B2E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA3CON | 0B30 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 | 0000 |
| DMA3REQ | 0B32 | FORCE | — | — | — | — | — | — | — | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 | 00FF |
| DMA3STAL | 0B34 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STAH | 0B36 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA3STBL | 0B38 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STBH | 0B3A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA3PAD | 0B3C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3CNT | 0B3E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMAPWC | 0BF0 | — | — | — | — | — | — | — | — | — | — | — | — | PWCOL<3:0> | | | | 0000 |
| DMARQC | 0BF2 | — | — | — | — | — | — | — | — | — | — | — | — | RQCOL<3:0> | | | | 0000 |
| DMAPPS | 0BF4 | — | — | — | — | — | — | — | — | — | — | — | — | PPST<3:0> | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### 4.3.1 PAGED MEMORY SCHEME

The dsPIC33EVXXXGM00X/10X family architecture extends the available DS through a paging scheme, which allows the available DS to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the Base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Data Space Read Page register (DSRPAG) or the 9-bit Data Space Write Page register (DSWPAG), to form an EDS address, or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space. Construction of the EDS address is shown in Figure 4-9 and Figure 4-10. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when the base address bit, EA<15> = 1, the DSWPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS write address.

**FIGURE 4-9: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION**




**Note:** DS read access when DSRPAG = 0x000 will force an address error trap.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)**

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 7-1: SR: CPU STATUS REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA | OB | SA | SB | OAB | SAB | DA | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IPL2(2,3) | IPL1(2,3) | IPL0(2,3) | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

**Note 1:** For complete register details, see Register 3-1.

**2:** The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.

**3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)**

bit 2 **Unimplemented:** Read as '0'

bit 1 **C1MD:** CAN1 Module Disable bit(1)
1 = CAN1 module is disabled
0 = CAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

**Note 1:** This bit is available on dsPIC33EVXXXGM10X devices only.

**REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **IC4MD:IC1MD:** Input Capture x (x = 1-4) Module Disable bits
1 = Input Capture x module is disabled
0 = Input Capture x module is enabled

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **OC4MD:OC1MD:** Output Compare x (x = 1-4) Module Disable bits
1 = Output Compare x module is disabled
0 = Output Compare x module is enabled

**REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CMPMD | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-0 **Unimplemented:** Read as '0'

**REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | REFOMD | CTMUMD | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0 **Unimplemented:** Read as '0'

**REGISTER 17-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PDCx<15:0>:** PWMx Generator Duty Cycle Value bits

**REGISTER 17-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PHASEx<15:0>:** PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

**Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.

**2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL.

**NOTES:**

**REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

**REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

## 24.3 ADC Control Registers

**REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC, HS | R/C-0, HC, HS |
|---|---|---|---|---|---|---|---|
| SSRC2 | SSRC1 | SSRC0 | SSRCG | SIMSAM | ASAM | SAMP | DONE(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** ADCx Operating Mode bit
1 = ADCx module is operating
0 = ADCx is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADCx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ADDMABM:** ADCx DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather mode address to the DMA channel based on the index of the analog input and the size of the DMA buffer

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** ADCx 10-Bit or 12-Bit Operation Mode bit
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer (DOUT = 0000 dddd dddd dddd)

**Note 1:** Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

**REGISTER 26-2: CVR2CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 2**

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CVREN | CVROE(1) | — | — | CVRSS | VREFSEL | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CVR6 | CVR5 | CVR4 | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF2O Pin) bit(1)
1 = Voltage level is output on the CVREF2O pin
0 = Voltage level is disconnected from the CVREF2O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = Comparator Reference Source 2 (CVR2) provides inverting input voltage when VREFSEL (CVR1CON<10>) = 0
0 = Comparator Reference Source 1 (CVR1) provides inverting input voltage when VREFSEL (CVR1CON<10>) = 0

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

**Note 1:** CVROE (CVR2CON<14>) is not available on the 28-pin devices.

**REGISTER 27-1: DEVID: DEVICE ID REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<23:16>(1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<15:8>(1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<7:0>(1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-Only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEVID<23:0>:** Device Identifier bits(1)

**Note 1:** Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of Device ID values.

**REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<23:16>(1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<15:8>(1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<7:0>(1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEVREV<23:0>:** Device Revision bits(1)

**Note 1:** Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of device revision values.

## 30.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**. |

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

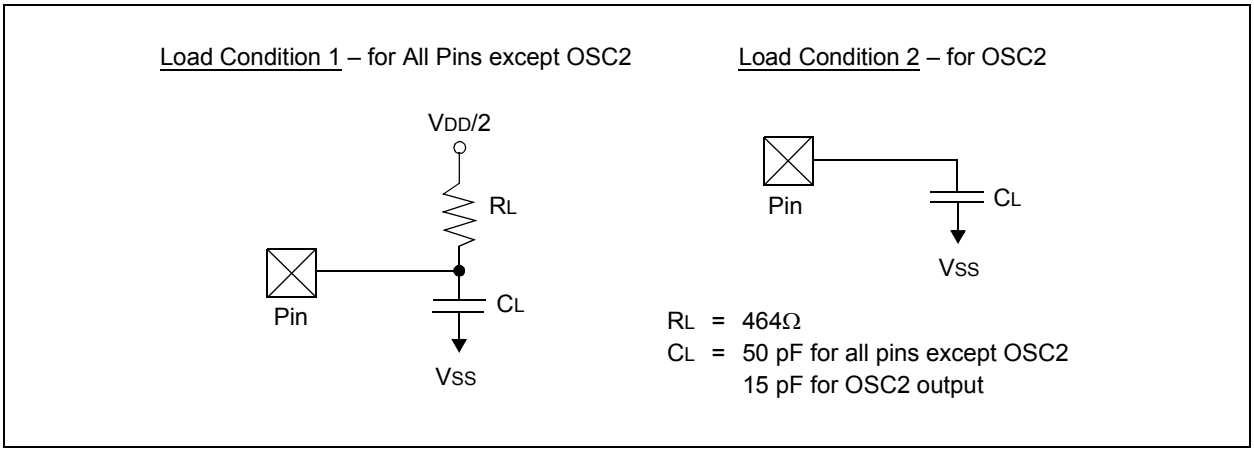



**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO50 | COSCO | OSC2 Pin | — | — | 15 | pF | In XT and HS modes, when external clock is used to drive OSC1 |
| DO56 | CIO | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$ mode |

## 31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EVXXXGM00X/10X family electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 "Electrical Characteristics"** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings(1)

Ambient temperature under bias(2) ..... -40°C to +150°C
Storage temperature ..... -65°C to +160°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +6.0V
Maximum current out of $V_{SS}$ pin ..... 350 mA
Maximum current into $V_{DD}$ pin(3) ..... 350 mA
Maximum junction temperature ..... +155°C
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sunk by all ports combined ..... 200 mA
Maximum current sourced by all ports combined(3) ..... 200 mA

**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

**2:** AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

**3:** Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

## 31.1 High-Temperature DC Characteristics

**TABLE 31-1: OPERATING MIPS vs. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temperature Range (in °C) | Max MIPS |
|---|---|---|---|
| | | | dsPIC33EVXXXGM00X/10X Family |
| HDC5 | 4.5V to 5.5V(1,2) | -40°C to +150°C | 40 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Device functionality is tested but is not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

**2:** When BOR is enabled, the device will work from 4.7V to 5.5V.

**TABLE 31-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| High-Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +155 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +150 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min. | Typ.(1) | Max. | Units | Conditions |
| **Operating Voltage** | | | | | | | |
| HDC10 | VDD | **Supply Voltage(3)** | VBOR | — | 5.5 | V | |
| HDC12 | VDR | **RAM Data Retention Voltage(2)** | 1.8 | — | — | V | |
| HDC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | — | — | VSS | V | |
| HDC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 1.0 | — | — | V/ms | 0V-5.0V in 5 ms |
| HDC18 | VCORE | **VDD Core** Internal Regulator Voltage | 1.62 | 1.8 | 1.98 | V | Voltage is dependent on load, temperature and VDD |

**Note 1:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**2:** This is the limit to which VDD may be lowered without losing RAM data.

**3:** VDD voltage must remain at VSS for a minimum of 200 μs to ensure POR.

**FIGURE 33-3: TYPICAL IDD vs. VDD (EC MODE, 20 MIPS)**

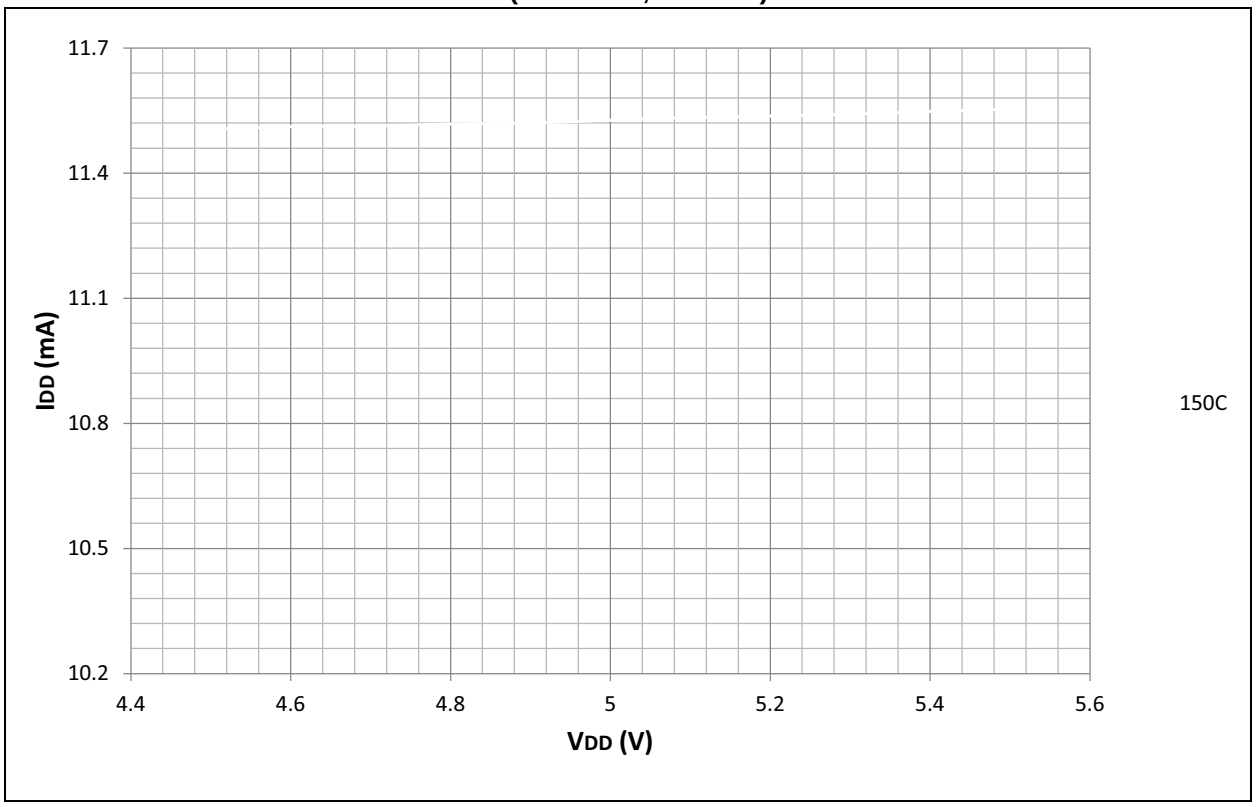
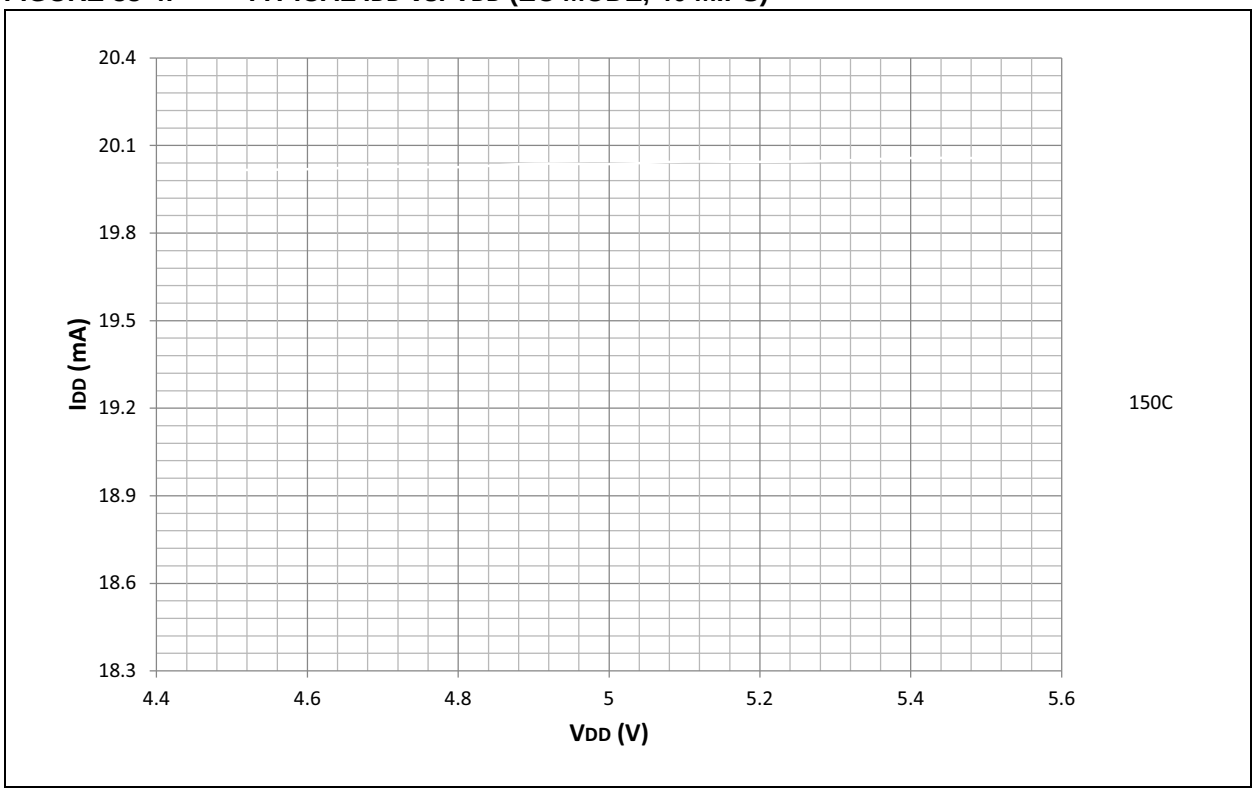



**FIGURE 33-4: TYPICAL IDD vs. VDD (EC MODE, 40 MIPS)**



## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: http://microchip.com/support**

**NOTES:**