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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm006-i-mr">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm006-i-mr</a>

# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER<sup>(1,3)</sup>

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2 <sup>(2)</sup>	NOSC1 <sup>(2)</sup>	NOSC0 <sup>(2)</sup>
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Backup FRC Oscillator (BFRC)<sup>(4)</sup>
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) Divided by N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits<sup>(2)</sup>

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved<sup>(5)</sup>
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) Divided by N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

- 1 = If FCKSM0 = 1, then clock and PLL configurations are locked; if FCKSM0 = 0, then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

**Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*” (available from the Microchip web site) for details.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This register resets only on a Power-on Reset (POR).

**4:** COSC<2:0> bits will be set to '0b100' when FRC fails.

**5:** User cannot write '0b100' to NOSC<2:0>. COSC<2:0> will be set to '0b100' (BFRC) when the FRC fails.

## 14.0 DEADMAN TIMER (DMT)

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Deadman Timer (DMT)**” (DS70005155) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

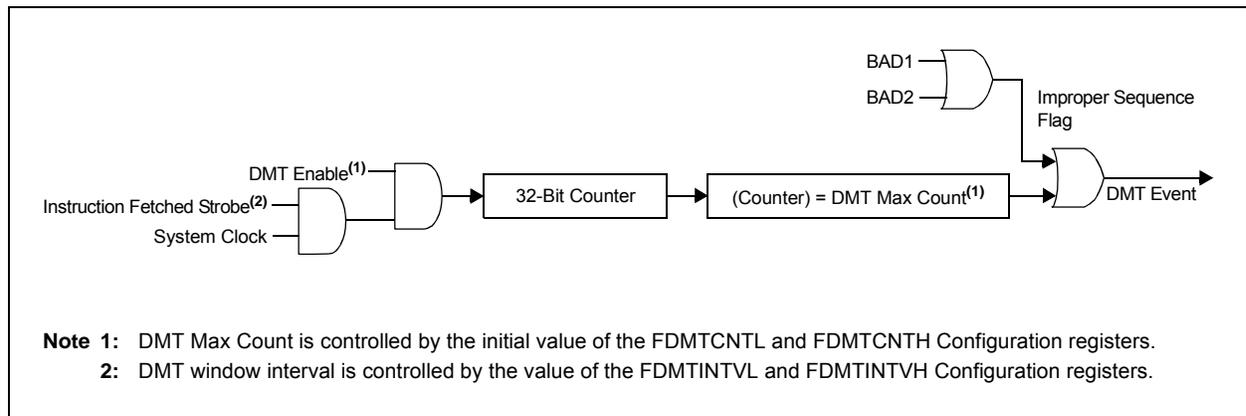
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical, and safety-critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 14-1 shows a block diagram of the Deadman Timer module.

**FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM**



## 16.0 OUTPUT COMPARE

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Output Compare**” (DS70005157) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

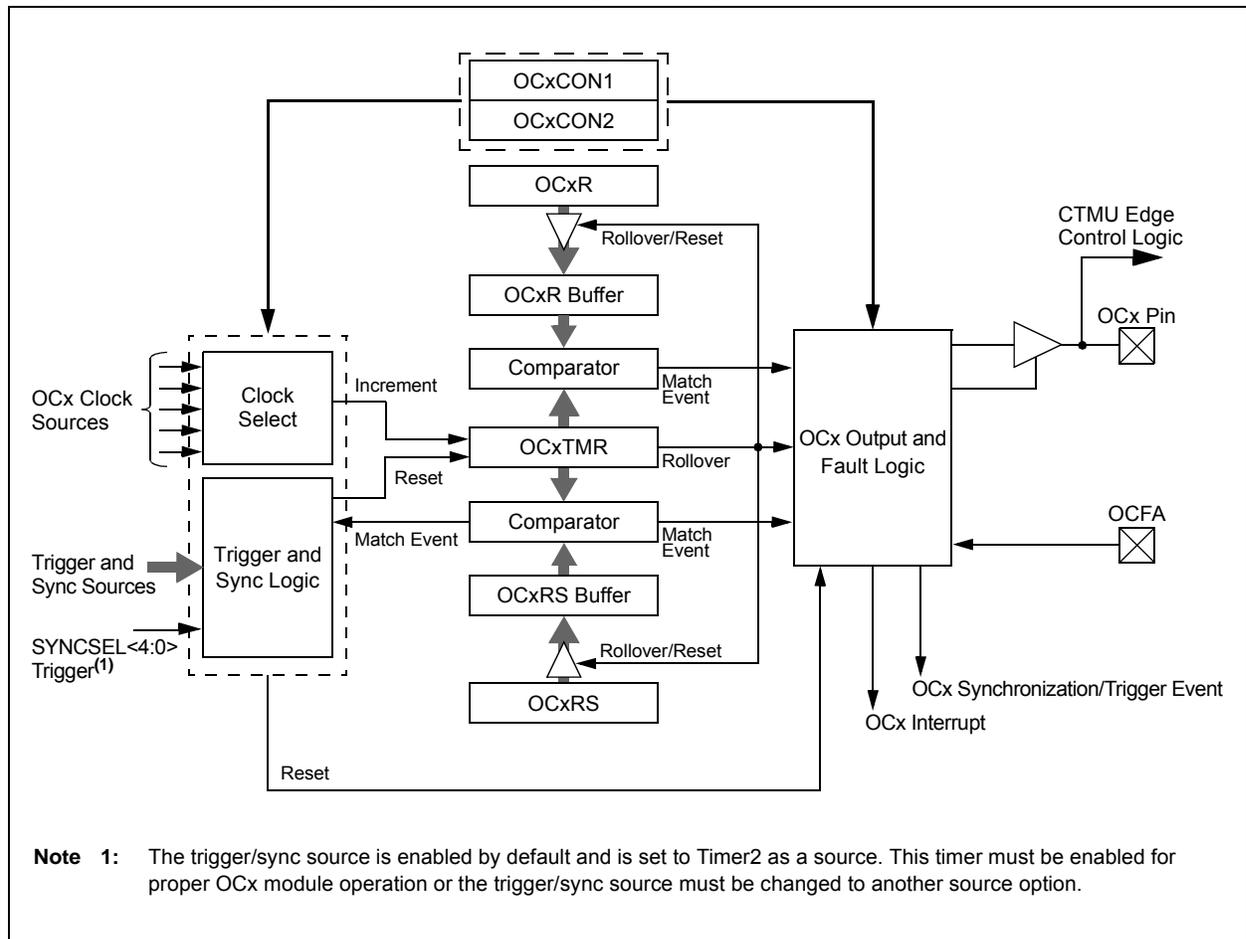
sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Figure 16-1 shows a block diagram of the output compare module.

**Note:** For more information on OCxR and OCxRS register restrictions, refer to the “**Output Compare**” (DS70005157) section in the “*dsPIC33/PIC24 Family Reference Manual*”.

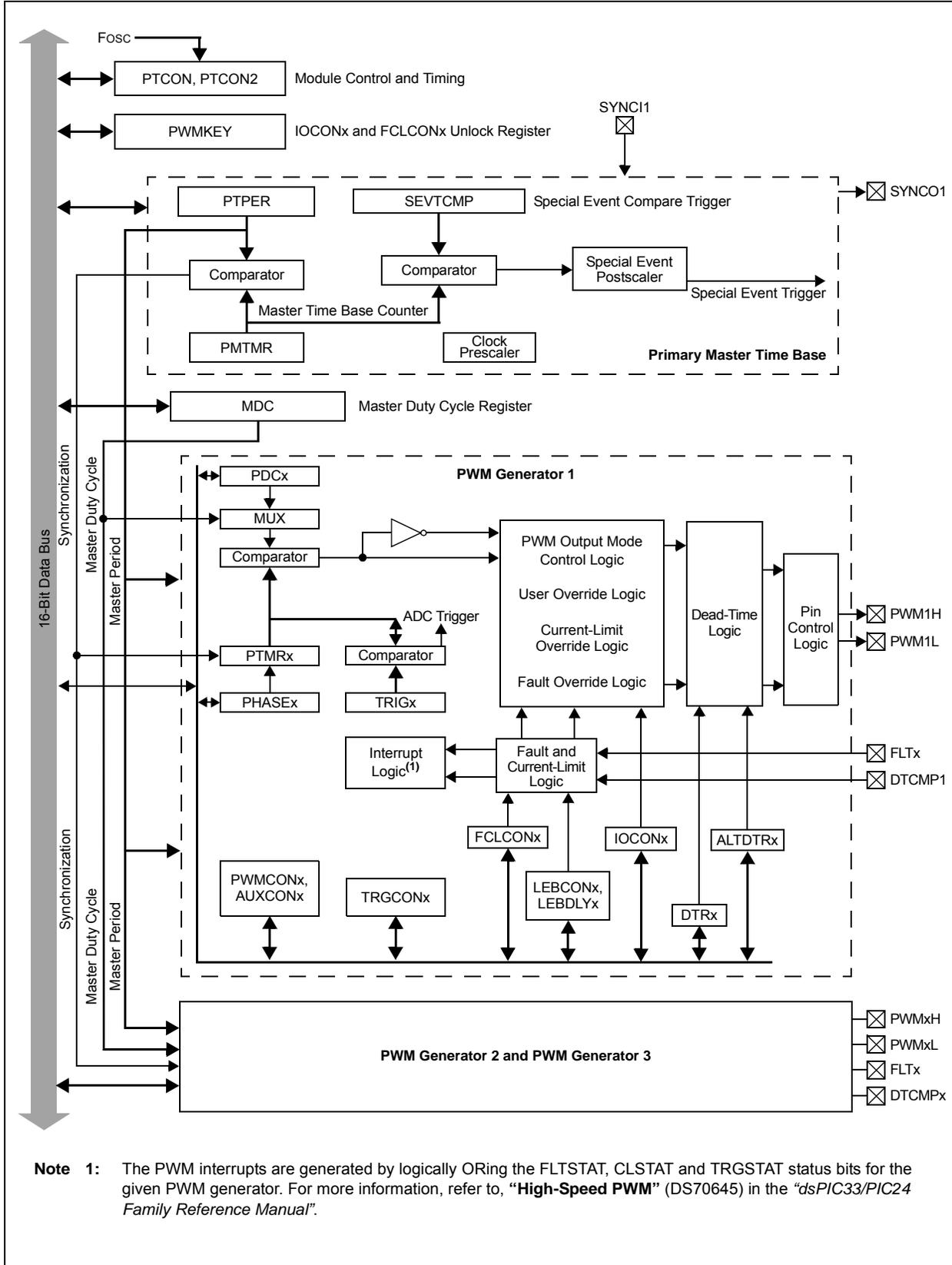
The dsPIC33EVXXGM00X/10X family devices support up to 4 output compare modules. The output compare module can select one of eight available clock

**FIGURE 16-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM**



# dsPIC33EVXXGM00X/10X FAMILY

**FIGURE 17-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM**



# dsPIC33EVXXGM00X/10X FAMILY

## 17.3 PWMx Control Registers

### REGISTER 17-1: PTCN: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU <sup>(1)</sup>	SYNCPOL <sup>(1)</sup>	SYNCOEN <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN <sup>(1)</sup>	SYNCSRC2 <sup>(1)</sup>	SYNCSRC1 <sup>(1)</sup>	SYNCSRC0 <sup>(1)</sup>	SEVTPS3 <sup>(1)</sup>	SEVTPS2 <sup>(1)</sup>	SEVTPS1 <sup>(1)</sup>	SEVTPS0 <sup>(1)</sup>
bit 7							bit 0

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15      **PTEN:** PWMx Module Enable bit  
1 = PWMx module is enabled  
0 = PWMx module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PTSIDL:** PWMx Time Base Stop in Idle Mode bit  
1 = PWMx time base halts in CPU Idle mode  
0 = PWMx time base runs in CPU Idle mode
- bit 12      **SESTAT:** Special Event Interrupt Status bit  
1 = Special event interrupt is pending  
0 = Special event interrupt is not pending
- bit 11      **SEIEN:** Special Event Interrupt Enable bit  
1 = Special event interrupt is enabled  
0 = Special event interrupt is disabled
- bit 10      **EIPU:** Enable Immediate Period Updates bit<sup>(1)</sup>  
1 = Active Period register is updated immediately  
0 = Active Period register updates occur on PWMx cycle boundaries
- bit 9        **SYNCPOL:** Synchronize Input and Output Polarity bit<sup>(1)</sup>  
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)  
0 = SYNCI1/SYNCO1 is active-high
- bit 8        **SYNCOEN:** Primary Time Base Sync Enable bit<sup>(1)</sup>  
1 = SYNCO1 output is enabled  
0 = SYNCO1 output is disabled
- bit 7        **SYNCEN:** External Time Base Synchronization Enable bit<sup>(1)</sup>  
1 = External synchronization of primary time base is enabled  
0 = External synchronization of primary time base is disabled

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'  
 bit 13-0      **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

## REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'  
 bit 13-0      **ALTDTRx<13:0>:** Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

# dsPIC33EVXXGM00X/10X FAMILY

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NOTES:

# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R/C-0	R-0	R/W-0, HC
PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN <sup>(1)</sup>
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 15-8      **Unimplemented:** Read as '0'

bit 7      **PAUSE:** Pause Period Status bit

- 1 = The module is transmitting/receiving a pause period
- 0 = The module is not transmitting/receiving a pause period

bit 6-4      **NIB<2:0>:** Nibble Status bit

Module in Transmit Mode (RCVEN = 0):

- 111 = Module is transmitting a CRC nibble
- 110 = Module is transmitting Data Nibble 6
- 101 = Module is transmitting Data Nibble 5
- 100 = Module is transmitting Data Nibble 4
- 011 = Module is transmitting Data Nibble 3
- 010 = Module is transmitting Data Nibble 2
- 001 = Module is transmitting Data Nibble 1
- 000 = Module is transmitting a status nibble or pause period, or is not transmitting

Module in Receive Mode (RCVEN = 1):

- 111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred
- 110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
- 101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
- 100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
- 011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
- 010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
- 001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
- 000 = Module is receiving a status nibble or waiting for Sync

bit 3      **CRCERR:** CRC Status bit (Receive mode only)

- 1 = A CRC error occurred for the 1-6 data nibbles in SENTxDATH/L
- 0 = A CRC error has not occurred

bit 2      **FRMERR:** Framing Error Status bit (Receive mode only)

- 1 = A data nibble was received with less than 12 tick periods or greater than 27 tick periods
- 0 = Framing error has not occurred

bit 1      **RXIDLE:** SENTx Receiver Idle Status bit (Receive mode only)

- 1 = The SENTx data bus has been Idle (high) for a period of SYNCMAX<15:0> or greater
- 0 = The SENTx data bus is not Idle

**Note 1:** In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 22-2: CxCTRL2: CANx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT<4:0>				
bit 7						bit 0	

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15-5      **Unimplemented:** Read as '0'
- bit 4-0      **DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits
  - 10010-11111 = Invalid selection
  - 10001 = Compare up to Data Byte 3, bit 6 with EID<17>
  - 
  - 
  - 
  - 00001 = Compare up to Data Byte 1, bit 7 with EID<0>
  - 00000 = Do not compare data bytes



# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 22-14: CxBUFPNT3: CANx FILTERS 8-11 BUFFER POINTER REGISTER 3

R/W-0							
F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0
bit 15							bit 8

R/W-0							
F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15-12      **F11BP<3:0>**: RX Buffer Mask for Filter 11 bits  
 1111 = Filter hits received in RX FIFO buffer  
 1110 = Filter hits received in RX Buffer 14  
 •  
 •  
 •  
 0001 = Filter hits received in RX Buffer 1  
 0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F10BP<3:0>**: RX Buffer Mask for Filter 10 bits (same values as bits 15-12)
- bit 7-4      **F9BP<3:0>**: RX Buffer Mask for Filter 9 bits (same values as bits 15-12)
- bit 3-0      **F8BP<3:0>**: RX Buffer Mask for Filter 8 bits (same values as bits 15-12)

# dsPIC33EVXXGM00X/10X FAMILY

## REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15						bit 8	

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm <sup>(1)</sup>	TXLARBm <sup>(1)</sup>	TXERRm <sup>(1)</sup>	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7						bit 0	

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-8            See Definition for bits 7-0, controls Buffer n.
- bit 7              **TXENm**: TX/RX Buffer Selection bit  
                    1 = Buffer, TRBm, is a transmit buffer  
                    0 = Buffer, TRBm, is a receive buffer
- bit 6              **TXABTm**: Message Aborted bit<sup>(1)</sup>  
                    1 = Message was aborted  
                    0 = Message completed transmission successfully
- bit 5              **TXLARBm**: Message Lost Arbitration bit<sup>(1)</sup>  
                    1 = Message lost arbitration while being sent  
                    0 = Message did not lose arbitration while being sent
- bit 4              **TXERRm**: Error Detected During Transmission bit<sup>(1)</sup>  
                    1 = A bus error occurred while the message was being sent  
                    0 = A bus error did not occur while the message was being sent
- bit 3              **TXREQm**: Message Send Request bit  
                    1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent  
                    0 = Clearing the bit to '0' while set requests a message abort
- bit 2              **RTRENm**: Auto-Remote Transmit Enable bit  
                    1 = When a remote transmit is received, TXREQ will be set  
                    0 = When a remote transmit is received, TXREQ will be unaffected
- bit 1-0            **TXmPRI<1:0>**: Message Transmission Priority bits  
                    11 = Highest message priority  
                    10 = High intermediate message priority  
                    01 = Low intermediate message priority  
                    00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQm is set.

**Note:** The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

# dsPIC33EVXXGM00X/10X FAMILY

## BUFFER 22-7: CANx MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
Byte 7<15:8>								
bit 15								bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
Byte 6<7:0>								
bit 7								bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-8                      **Byte 7<15:8>**: CANx Message Byte 7 bits

bit 7-0                      **Byte 6<7:0>**: CANx Message Byte 6 bits

## BUFFER 22-8: CANx MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	—	FILHIT<4:0> <sup>(1)</sup>					
bit 15								bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 7								bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-13                      **Unimplemented:** Read as '0'

bit 12-8                      **FILHIT<4:0>**: Filter Hit Code bits<sup>(1)</sup>  
 Encodes number of filter that resulted in writing this buffer.

bit 7-0                      **Unimplemented:** Read as '0'

**Note 1:** Only written by module for receive buffers, unused for transmit buffers.

# dsPIC33EVXXGM00X/10X FAMILY

## 26.2 Comparator Voltage Reference Registers

**REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1**

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—
bit 15						bit 8	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7						bit 0	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15      **CVREN:** Comparator Voltage Reference Enable bit  
 1 = Comparator voltage reference circuit is powered on  
 0 = Comparator voltage reference circuit is powered down
- bit 14      **CVROE:** Comparator Voltage Reference Output Enable (CVREF10 Pin) bit  
 1 = Voltage level is output on the CVREF10 pin  
 0 = Voltage level is disconnected from the CVREF10 pin
- bit 13-12   **Unimplemented:** Read as '0'
- bit 11      **CVRSS:** Comparator Voltage Reference Source Selection bit  
 1 = Comparator reference source, CVRSRC = CVREF+ – AVSS  
 0 = Comparator reference source, CVRSRC = AVDD – AVSS
- bit 10      **VREFSEL:** Voltage Reference Select bit  
 1 = CVREFIN = CVREF+  
 0 = CVREFIN is generated by the resistor network
- bit 9-7     **Unimplemented:** Read as '0'
- bit 6-0     **CVR<6:0>:** Comparator Voltage Reference Value Selection bits  
 1111111 = 127/128 x VREF input voltage  
 •  
 •  
 •  
 0000000 = 0.0 volts



## 29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

## 29.10 MPLAB PM3 Device Programmer

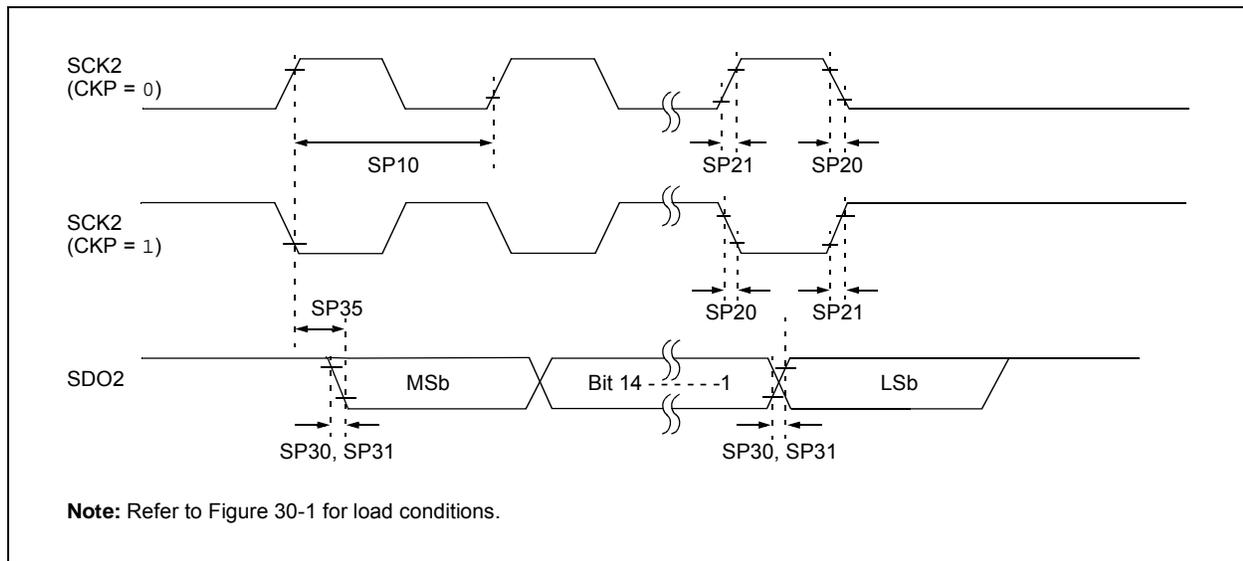
The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

# dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 30-30: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY**

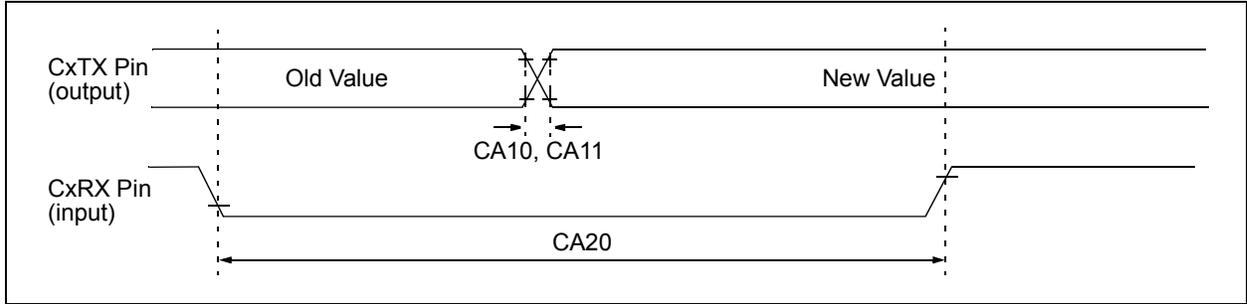
AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 30-31	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-32	—	1	0,1	1
9 MHz	—	Table 30-33	—	0	0,1	1
15 MHz	—	—	Table 30-34	1	0	0
11 MHz	—	—	Table 30-35	1	1	0
15 MHz	—	—	Table 30-36	0	1	0
11 MHz	—	—	Table 30-37	0	0	0

**FIGURE 30-12: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**



# dsPIC33EVXXGM00X/10X FAMILY

**FIGURE 30-32: CANx MODULE I/O TIMING CHARACTERISTICS**



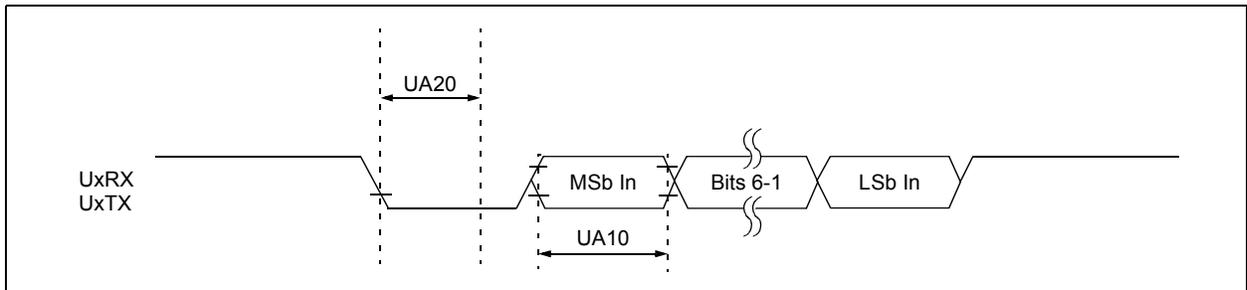
**TABLE 30-48: CANx MODULE I/O TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TcWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 30-33: UARTx MODULE I/O TIMING CHARACTERISTICS**



**TABLE 30-49: UARTx MODULE I/O TIMING REQUIREMENTS**

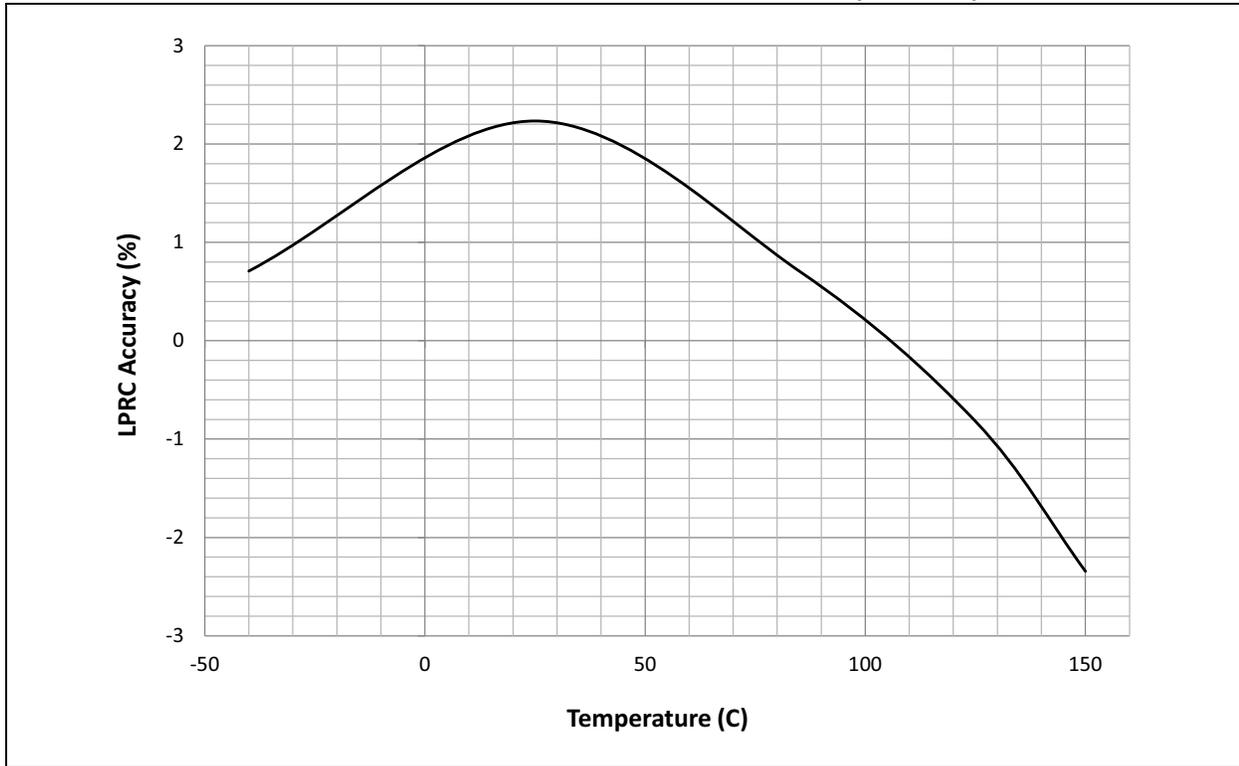
AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TcWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

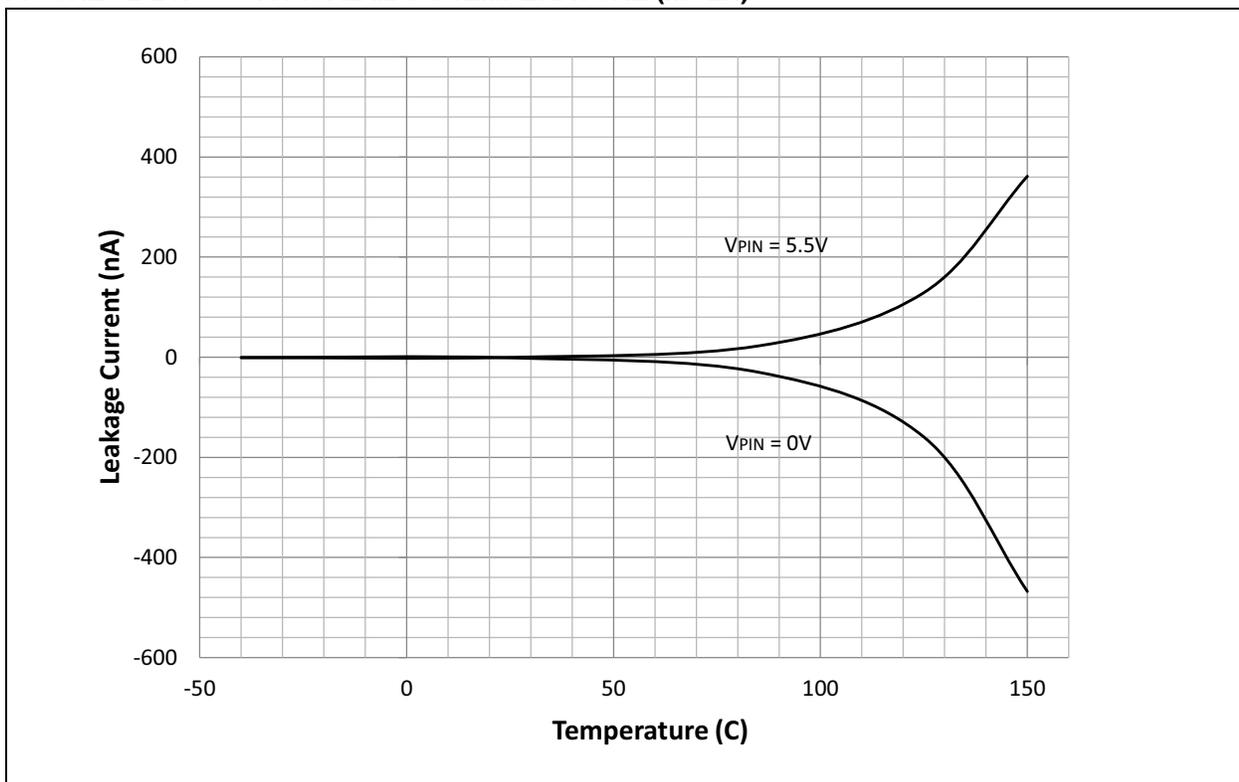
# dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 32-23: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V V<sub>DD</sub>)



## 32.7 Leakage Current

FIGURE 32-24: TYPICAL I<sub>IL</sub> vs. TEMPERATURE ( $\overline{MCLR}$ )



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